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INFOTRACKS

YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Transfer Molding

By Christopher Henderson

In this month's Feature Article, we continue our series on Transfer Molding. Transfer Molding is one of the more common steps in semiconductor packaging, and provides protection for the sensitive semiconductor components and packaging interconnect. In this article, we will continue the discussion of the constituents of mold compounds.

Let's now go into more detail on the individual components of mold compound. The first component we will discuss is the epoxy resin. This is the most important constituent of the mold compound. It serves as the binding material. Epoxy resins are characterized by an epoxide group. We show a general example of an epoxide group in Figure 1. An epoxide group contains two carbon atoms and an oxygen atom. Epoxy resins are typically cured with thermal energy, so they are often referred to as a thermosetting polymer, or thermoset for short hand notation.

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Want to take control of your learning? See page 8

Upcoming Courses:

- Packaging Failure and Yield Analysis
- Defect-Based Testing

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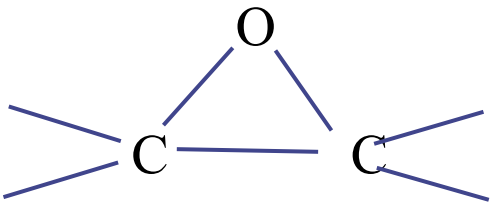

The most generalized structure of the epoxide group

Three member ring with an oxygen atom bonded to two carbon atoms

Figure 1- Chemical structure of an epoxide group

Below we list several common epoxy resins. First is Phenolic or Cresol Novolac. Phenolic epoxy resins are synthetic polymers obtained by the reaction of phenol or substituted phenol with formaldehyde. Cresol Novolac is a variation of this. Novolacs are phenol-formaldehyde epoxy resins with a formaldehyde to phenol molar ratio of less than one. They are often produced from cresols, or methylphenols. Second is Diglycidyl ether of bisphenol A or F. Bisphenol A diglycidyl ether (commonly abbreviated BADGE or DGEBA) is an organic liquid epoxy resin compound. Addition of further Bisphenol A and a catalyst and heat can produce Bisphenol A glycidyl ether epoxy resins of higher molecular weight that are solid. Bisphenol AF (abbreviated as BPAF) is a fluorinated organic compound that is an analogue of bisphenol A in which the two methyl groups are replaced with trifluoromethyl groups. Third are multifunctional epoxy resins. Scientists can address weaknesses in standard epoxy resins by making conventional epoxy resins multifunctional either through chemical modification or manipulation of thermoset formulations to tailored properties. As with all other polymers, epoxy resins, even in some niche applications, still suffer from issues of brittleness, slow cure, non-recyclability, and temperature instability amongst others. Skilled scientists can tune the epoxy polymer in such a way where various groups within the polymer network reactively associate to induce toughness and flexibility. Fourth are the cycloaliphatic epoxides. Cycloaliphatic epoxy resins contain one or more cycloaliphatic rings in the molecule, for example 3,4-epoxycyclohexylmethyl-3,4-epoxycyclohexane carboxylate. This class also displays lower viscosity at room temperature, but offers significantly higher temperature resistance than the aliphatic epoxy resins. However, reactivity is rather low compared to other classes of epoxy resin, and high temperature curing using suitable accelerators is normally required. Fifth are the silicone-based resins. Siliconized epoxy resins can be prepared by the reaction of an amine-terminated silicone resin with a novolac-type epoxy resin.

Let's now discuss a few of the epoxy resin systems in more detail. We begin with one of the most common epoxy resin systems, Ortho Cresol Novolac, or OCN. We show the chemical structure for OCN on the left in Figure 2. In conjunction with this, engineers typically use a Phenol Novolac type hardener. We show the chemical structure of the hardener on the right in Figure 2. The main application for this resin system is for discrete components, and most types of surface-mount packages where the Moisture Sensitivity Level, or MSL, values are lower. The advantages of the OCN-PN system are that it is easy to handle for molding purposes, has a high glass transition temperature, and is low cost. The disadvantages of the OCN-PN system include poor adhesion, high water absorption, and poor flow properties during the molding process.

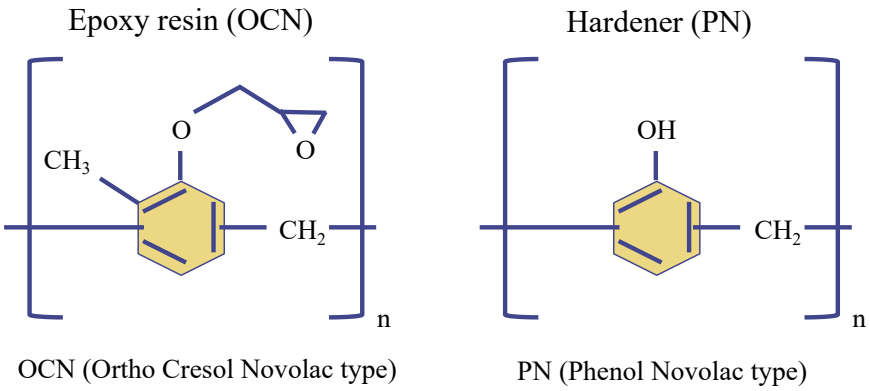

Figure 2- Example chemical structure of a common resin and hardener system.

Other common epoxy resin systems include the Low Molecular Weight, or LMW, systems. There are many types of LMW systems available. Biphenyl-type epoxy resins are a class of LMW system, and are popular for use in mold compounds. In Figure 3, we show the Biphenyl epoxy resin, xylylene hardener system, with their associated chemical structures. LMW systems exhibit excellent adhesion properties, and low water absorption. However, they suffer from poor handling properties due to their tackiness, moisture sensitivity, and low glass transition temperatures. These resin systems work well for typical surface mount devices, including Ball Grid Array devices.

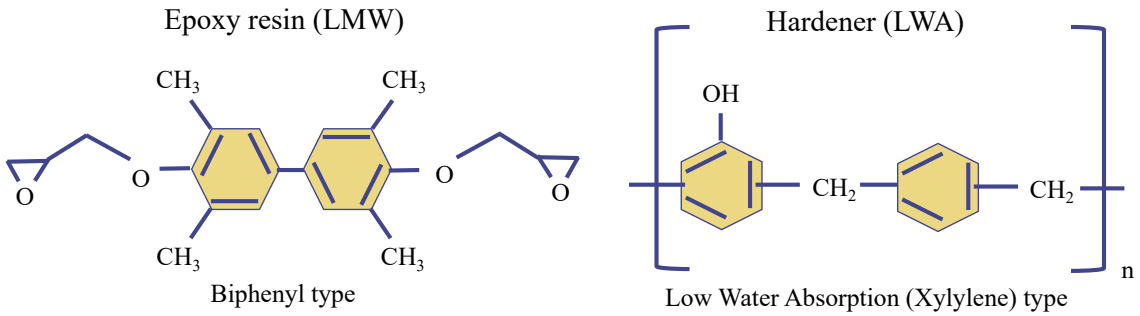

Figure 3- Chemical structures for LMW and Low Water Absorption (LWA) epoxy resin systems.

Other types of common epoxy resin systems include the Multifunctional type, or MF, systems. There are many types of MF systems available. In Figure 4, we show a generic MF epoxy resin hardener system, with their associated chemical structures. MF systems exhibit high glass transition temperatures and superior warpage properties. MF systems suffer from poor adhesion, high water absorption, and poor flame retardancy. These epoxy resin systems work well for Ball Grid Array devices, and other devices that operate with high junction temperatures.

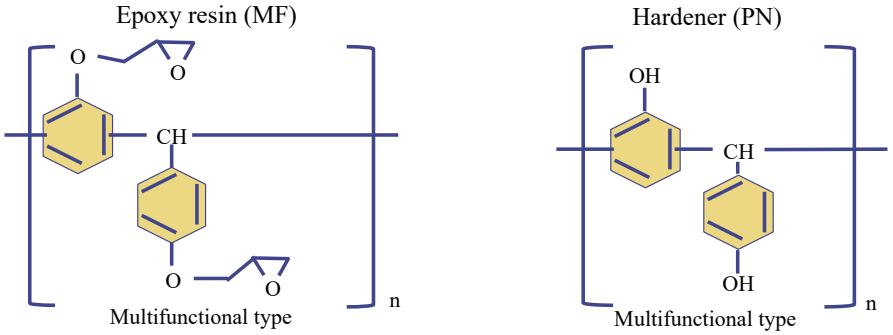

Figure 4- Chemical structures for MF epoxy resin systems.

The final types of epoxy resin systems we will discuss are the Multi-Aromatic Ring epoxy resin systems. These are newer materials that are relatively versatile. One important advantage about them is that they are self-extinguishing, so a flame-retardant chemical is not needed in conjunction with these systems. They have excellent mechanical properties, good thermal stability for use in applications where the semiconductor die might operate as high as 175ºC, and good flow properties. The main disadvantage is the cost of these materials.

Since biphenyl epoxy resins have a few disadvantages, a recent trend is to use more multifunctional epoxy resins in IC packaging. They are used mainly in thin outline packages. There are two resin types in use. One is tetraglycidyl ether of tetraphenol ethane, and the other is the type based on the biphenyl group, like we show in the chemical diagram in Figure 5. CEL9200NT and MC606 from Hitachi, and KMC240 from Shin-Etsu are examples of this type of resin.

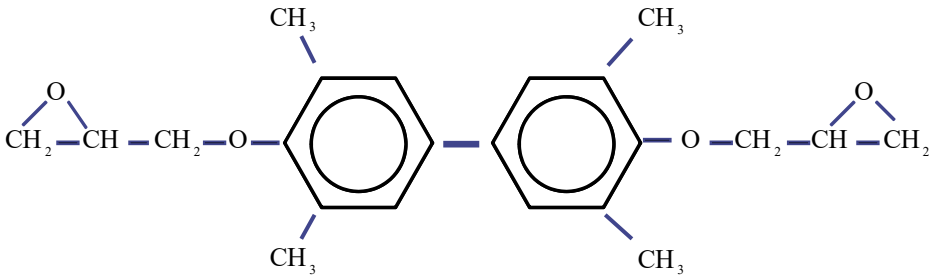

Figure 5- Chemical structure of a multifunction epoxy resin based on a biphenyl group.

In next month's Feature Article, we will continue our discussion of the mold compound constituents by covering curing agents in more detail.

Technical Tidbit: Under or Oversized Mask Features

This month's Technical Tidbit covers mask features that are incorrectly sized. This can be an issue in a local region on a mask; a repetitive structure on a mask; or a global sizing problem on the mask. The absolute size of a minimum feature, including line width, spacing, or contact dimensions is referred to as a Critical Dimension or CD. Variations in CDs can result from variability in photo resist thickness, exposure time, resist development time, temperature and etch time. Variations in CDs affect transistor values, resistor values, and can create potential for shorts or leakage between adjacent features. This failure mechanism addresses only defects associated with doped regions, i.e. lithographic defects at either diffusion or implant. Figure 1 shows an example of CD variation across a wafer.

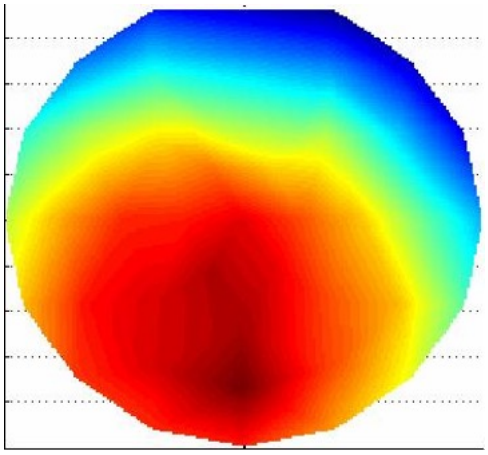

Figure 1- Map showing changes in CDs across a wafer (courtesy Zhang, Spanos, and Kameshwar).

Figure 2 shows an example of the effect of lithography dose on feature sizes.

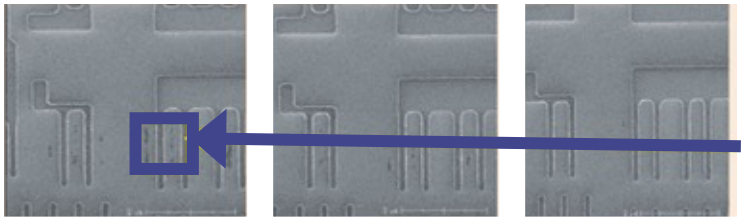

Figure 2- Images showing effects of lower exposure times in the lithography system.

Incorrect feature sizes are difficult to analyze because the electrical problems are usually quite subtle; the critical dimensions may be too small to see or obscured by metal; and the electrical failure symptoms may have a wide range of possible causes. For example, Figure 3 shows an example of a Shallow Trench Isolation (STI) structure that would not be visible once the chip fabrication is complete. Even after a problem is narrowed down to a potential issue like high or low resistor values, there is still the matter of sorting out whether the problem is caused by dimensional factors or by doping. At the wafer level, more evidence can be brought to bear. Engineers can examine both electrical and physical test patterns. Resistor values can be accurately measured. Sheet resistance can be determined from a Van der Pauw pattern which is independent of masking. If the sheet resistance is acceptable, but the resistor values are incorrect, then the problem may be from dimensional effects or contact resistance. Multiple sites can be tested to increase accuracy, and the results of multiple parameters scrutinized for relationships between them and spatially across a wafer.

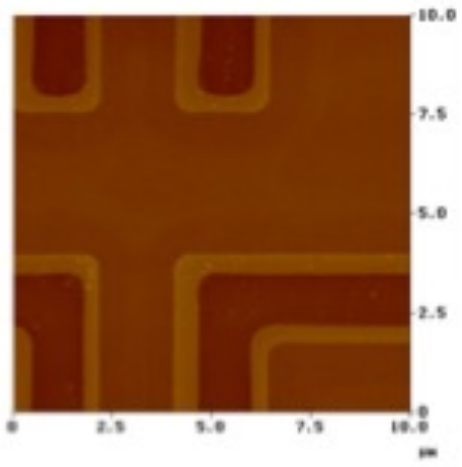

Figure 3- STI Structure examined with an Atomic Force Microscope (AFM). This type of examination is normally not possible after subsequent processing, but only afterwards through destructive failure analysis work.

Circuit simulation can be also used to determine if a CD problem can explain the observed symptoms. Good circuit design strives to immunize designs from CD variation by having performance set by transistor ratios and using transistors with the same width and bias. Note that narrow transistors show more resistance variation than do wider resistors. Figure 4 shows data from a simulation where the x- and y-dimensions of a transistor are varied slightly. Note the red regions show large changes in transistor drive current.

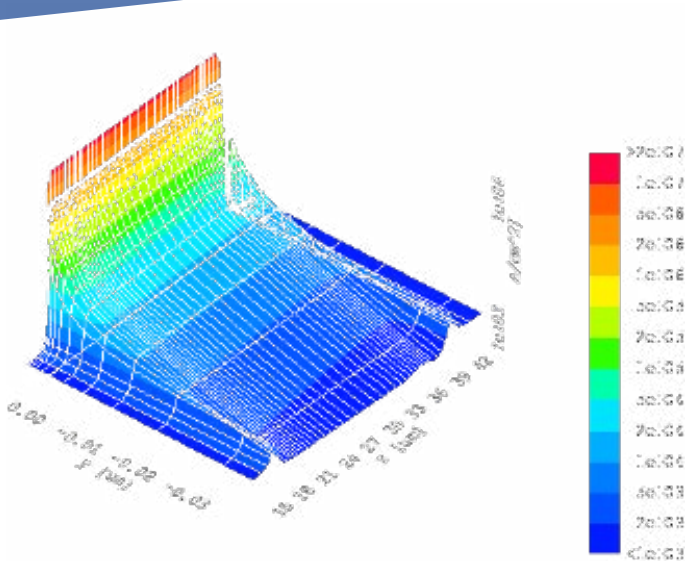

Figure 4- Transistor drive current as a function of transistor channel x- and y-dimensions.

If CDs have an effect on device parameters or performance, it will show up at e-sort or final test, and it is not likely to become a reliability issue. The CD for an ion implanted layer may not be visually measurable on the finished product, but may be inferred from electrical measurements. The two most important factors in determining the resistance of a thin film resistor are its width and the sheet resistance of its diffusion. Sheet resistance is measured using a Van der Pauw or 4-point probe test pattern. A Van der Pauw pattern is a clover-leaf pattern with electrical contacts at the four corners. We show examples of Van der Pauw patterns in Figure 5. By forcing current between two adjacent corners and measuring voltage across the opposite two corners, a kelvin- type sheet resistance can be calculated which in insensitive to the masking dimensions of the diffusions. With a known sheet resistance and resistor length, the width (a critical dimension) can be calculated. Resistor variation, after normalizing out sheet resistance differences, can serve as an electrical monitor of critical dimensions. The mathematics is somewhat more complicated than it first seems because the resistor width is comprised of the width of the diffusion opening plus the width of the two out-diffusions on either side. Since narrow resistors are needed for these test structures, the sidewall components to resistance can be significant.

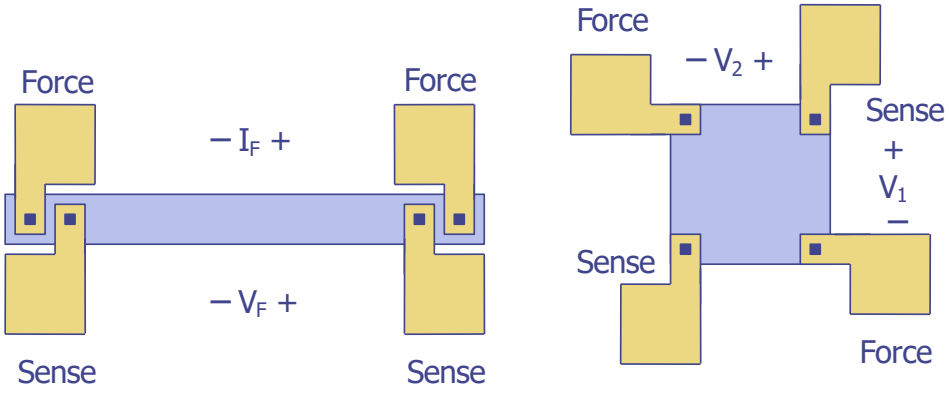

Figure 5- Examples of van der Pauw test patterns to accurately measure resistance.

Ask The Experts

Q: What is a dambar cut?

A: The dambar is a section of the packaging leadframe that serves as part of the seal during the transfer molding process. Because of its function, it shorts the leads together, so after the transfer molding process, the sections of the dambar between the leads need to be cut away to isolate the leads electrically from each other. This process is referred to as the dambar cutting process. We show this graphically in Figure 1.

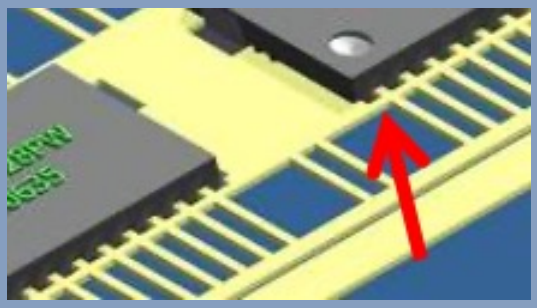

Figure 1- Dambar structure visible on an IC package leadframe strip.

Course Spotlight: SEMICONDUCTOR RELIABILITY AND PRODUCT QUALIFICATION

OVERVIEW

Package reliability and qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms, and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability; assessing the impact of new materials; dealing with limited margins, and other factors. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. While customers expect high reliability levels, incorrect testing, calculations, and qualification procedures can severely impact reliability. ***Semiconductor Reliability and Product Qualification*** is a 4-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability and qualification. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

Participants will learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product. This skill building series is divided into four segments:

1. **Overview of Reliability and Statistics.** Participants will learn the fundamentals of statistics, sample sizes, distributions and their parameters.

2. **Failure Mechanisms.** Participants will learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die and at the package level. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, and others.

3. **Qualification Principles.** Participants will learn how test structures can be designed to help test for a particular failure mechanism.

4. **Test Strategies.** Participants will learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. This course will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.

2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.

3. This course will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.

4. This course will offer a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.

5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.

6. Participants will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.

7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

COURSE OUTLINE

DAY 1

1. Introduction to Reliability
    a. Basic Concepts
    b. Definitions
    c. Historical Information

2. Statistics and Distributions
    a. Basic Statistics
    b. Distributions (Normal, Lognormal, Exponent, Weibull)
    c. Which Distribution Should I Use?
    d. Acceleration
    e. Number of Failures

DAY 2

3. Overview of Die-Level Failure Mechanisms
    a. Time Dependent Dielectric Breakdown
    b. Hot Carrier Damage
    c. Bias Temperature Instability
    d. Electromigration
    e. Stress Induced Voiding
    f. BEOL Dielectric Reliability

4. Package Level Mechanisms
    a. Moisture/Corrosion
        i. Failure Mechanisms
        ii. Models for Humidity
        iii. Tja Considerations
        iv. Static and Periodic stresses
        v. Exercises
    b. Thermo-Mechanical Stress
        i. Models
        ii. Failure Mechanisms
    c. Chip-Package Interactions
        i. Low-K fracture
    d. Through Silicon Via Reliability
    e. Thermal Degradation/Oxidation

DAY 3

5. Board Level
    a. Package Attach (Solder) Reliability
        i. Creep/Sheer/Strain
        ii. Lead-Free Issues
        iii. Electromigration/Thermomigration
        iv. MSL Testing
    b. Board Level Reliability Mechanisms
        i. Interposer
        ii. Substrate

6. Use Condition Failure Mechanisms
    a. Electrical Overstress/ESD
    b. Radiation Effects

7. Test Structures and Test Equipment

8. Developing Screens, Stress Tests, and Life Tests
    a. Burn-In
    b. Life Testing
    c. HAST
    d. JEDEC-based Tests
    e. Exercises

DAY 4

9. Calculating Chip and System Level Reliability

10. Developing a Qualification Program
    a. Process
    b. Standards-Based Qualification
    c. Knowledge-Based Qualification
    d. MIL-STD Qualification
    e. JEDEC Documents (JESD47H, JESD94, JEP148)
    f. AEC-Q100 Qualification

11. JEDEC Tests

12. Exercises and Discussion

Upcoming Courses:

Public Course Schedule:

Packaging Failure and Yield Analysis - September 23-24, 2024 (Mon.-Tues.) | Manila, Philippines -$1,195 until Mon. Sept. 2

Defect-Based Testing - November 18-19, 2024 (Mon.-Tues.) | Munich, Germany - $1,195 until Mon. Oct. 28

Wafer Fab Processing - November 25-28, 2024 (Mon.-Thurs.) | Munich, Germany -$2,095 until Mon. Nov. 4

Failure and Yield Analysis - December 2-5, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Nov. 11

Semiconductor Reliability and Product Qualification - December 9-12, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Nov. 18

Have an idea for a course? If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please email us at info@semitracks.com

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!