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YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Transfer Molding

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In this month's Feature Article, we continue our series on Transfer Molding. Transfer Molding is one of the more common steps in semiconductor packaging, and provides protection for the sensitive semiconductor components and packaging interconnect. In this article, we will start a discussion of the constituents of mold compounds.

Next, let's go into more detail on curing agents. Curing agents harden the resin material, so they are often referred to as hardeners. These agents help to create additional cross-links in the epoxy resin. The degree of hardening, reaction rate, cure time, and storage life depend heavily on the type of curing agent. Curing agents are polymers that contain functional groups that react with epoxide groups. Some common hardening agents contain amines, anhydride groups, phenolics, or cresol novolacs, with novolac curing agents being the most common ones.

Table 1 shows the advantages and disadvantages of the three groups of curing agents. Amine-based curing agents have rapid cure times, good shelf life, and good resistance to alkaline environments, but do not provide a good moisture barrier. Anhydrides provide good electrical performance, resistance to acidic environments, and low reaction rates, but do not provide a good moisture barrier. Phenolic and cresol novolacs provide a good moisture barrier, but suffer from thermal stability issues and low reaction rates.

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- Failure and Yield Analysis

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Curing Agent	Mold Compound Characteristics
Amine	Rapid cure
	Superior shelf life
	Maximum resistance to alkaline environment
	Poor moisture barrier
Anhydride	Good electrical performance
	Excellent resistance to acid environment
	Low reaction rate, needs accelerator
	Poor moisture barrier
	Good thermal stability (but for a shorter lifetime)
Phenolic and cresol novolacs	Good moisture barrier
	Thermally not as stable as anhydride cured
	Low reaction rate, needs accelerator

Table 1- Advantages and disadvantages of the three groups of curing agents.

Next, let's discuss catalysts in more detail. They are also known as accelerators, and enhance the rate of polymerization of the epoxy resin, which in turn helps to reduce the curing time. They are typically less than 1% by weight of the mold compound formulation, but they play a significant role in determining the storage life of the mold compound pellets. This is also known as the pot life. The faster the polymerization rate, the shorter the storage lifetime.

Table 2 shows the advantages and disadvantages of the three groups of accelerators, or catalysts. Amine-based catalyzing agents have excellent reactivity, but poor shelf life, poor electrical properties, and poor humidity resistance. Organophosphines have good acceleration properties, and moderate storage life characteristics. They also have excellent electrical properties and excellent heat and humidity resistance to alkaline environments. Salts created from the two groups at the top of the table typically have moderate acceleration properties, but show excellent storage life, excellent electrical properties, and excellent heat and humidity resistance.

Accelerator	Mold Compound Characteristics
Amines	Excellent reactivity
	Poor storage life
	Poor electrical properties
	Poor humidity resistance
Organophosphines	Good acceleration
	Moderate storage life
	Excellent electrical properties
	Excellent heat and humidity resistance
Salts of the above compounds	Moderate acceleration
	Excellent storage life
	Excellent electrical properties
	Excellent heat and humidity resistance

Table 2- Advantages and disadvantages of accelerators (catalysts).

Now let's take a closer look at the filler particles. Filler particles help to decrease the overall cost of the mold compound. They also provide structural rigidity and the necessary mechanical properties in the cured mold compound material. Filler particles also help to lower the coefficient of thermal expansion, or CTE, which in turn lowers the overall stresses induced in the semiconductor chip. The shape of the filler particles plays an important role in the flow properties of the mold compound. Assuming the particles have similar volumes, irregular particles, like crushed, fused, or flaked particles will hinder flow more so than spherical particles. Filler particles also help to increase the thermal conductivity of the package, which aids in removing heat from the semiconductor chip. There are different types of filler particles. They can be flake-like particles, spherical particles, as well as fused or crystalline. Filler particles can be made from silica; alumina, which is a silica-coated aluminum nitride known as SCAN; or boron nitride. For some applications, low alpha particle emission rates are needed, so there are "clean" versions of some of these filler particles where the unstable elements have been almost completely removed. We show examples of flake-type and spherical-type filler particles in Figure 1.

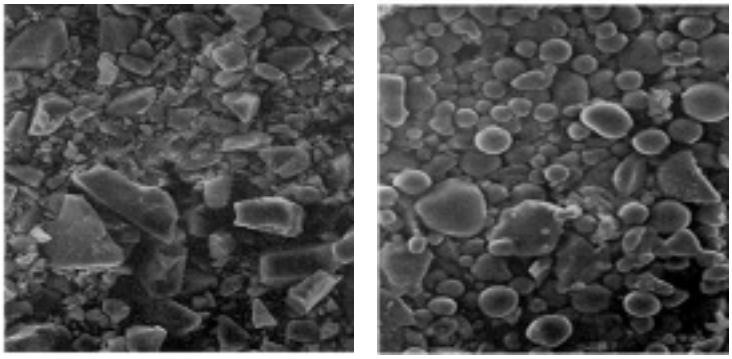

Figure 1- Ground (flake) filler particles (left), and spherical filler particles (right).

Filler particles are inert, and enhance the physical and mechanical properties of the epoxy resin. If engineers were to simply use the epoxy resin by itself, it would be costly, the coefficient of thermal expansion would be high, and the thermal conductivity of the package material would be quite low. The advantages of filler particles include: reducing the formulation cost, decreasing the coefficient of thermal expansion, and increasing the thermal conductivity. For example, without filler particles, the CTE of the package would be between 40 and 50 ppm/ºC. With basic filler particles, this value lowers to less than 25 ppm/ºC. Today's mold compound formulations can be even better, with values around 8 ppm/ºC, which is in between the value of the semiconductor die and the leadframe and wirebonds.

Filler particles help to reduce package shrinkage during the curing process; to increase the elastic modulus; to increase the hardness of the package; and to reduce moisture and gas permeability. The most common filler particles are silica. They can be crystalline silica, which provide enhanced thermal conductivity, but come with a higher coefficient of thermal expansion, or they can be ground fused silica, which provides for a lower CTE. There are also other filler materials, like hydrated magnesium silicate-talc, alumina, beryllium oxide, calcium silicate, and clay.

The particle size for inert filler material has an average size of 10 to 25 microns, but can be as big as 75 microns. The transfer molding process will typically encounter problems when the particles become larger than 100 microns. Some runner gates can be as small as 150 microns in diameter or width. Some lead fingers may only be 100 microns apart from one another. And some bond pad pitches in modern ICs can be as small as 65 microns. This can lead to blockages, voids and other problems when the particles are too large. Within the category of silica, ground fused silica is the most common. They can be particles with sharp edges, known as silica flakes, or spherical silica. Silica flakes may damage the mold tool, the passivation overcoat layer and the wirebonds, and may result in voids in certain package configurations. Spherical shaped particles improve performance, but they also cost somewhat more than silica flakes. In Figure 2, we show higher magnification images of silica flakes on the left and spherical silica on the right.

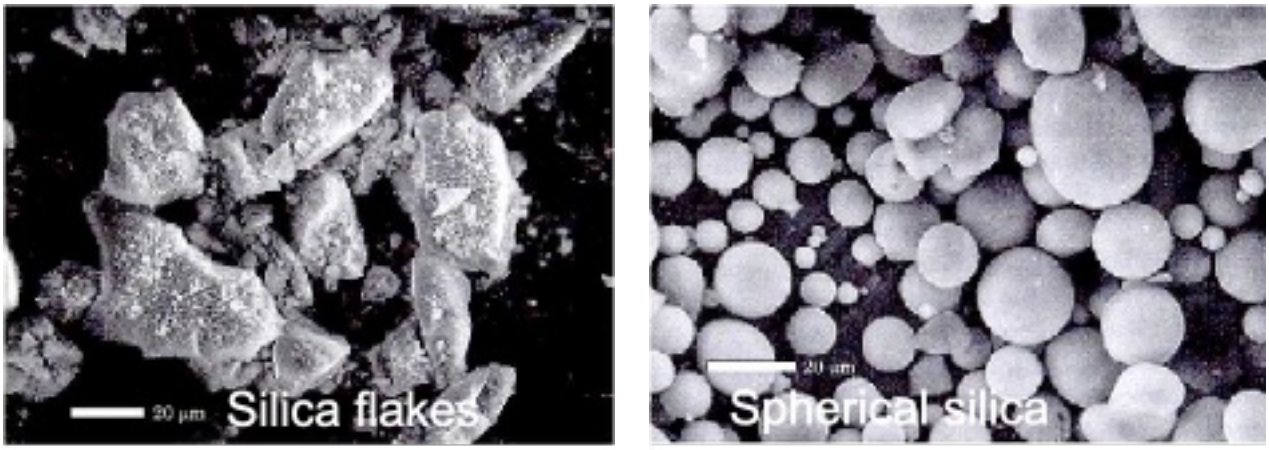

Figure 2- Higher magnification images of silica flakes (left) and spherical silica (right).

In next month's Feature Article, we will continue our discussion of the mold compound constituents by covering mold release agents in more detail.

Technical Tidbit: Insulated Gate Bipolar Transistor (IGBT) Operation

This month's Technical Tidbit covers the basic operation of an Insulated Gate Bipolar Transistor, or IGBT. The IGBT is a three-terminal power semiconductor device primarily used as an electronic switch. It combines high efficiency and fast switching. It switches electric power in many modern appliances: variable-frequency drives (VFDs), electric cars, trains, variable speed refrigerators, air-conditioners, and even stereo systems with switching amplifiers. Since it is designed to turn on and off rapidly, amplifiers that use it often synthesize complex waveforms with pulse width modulation and low-pass filters. The IGBT is used in medium- to high-power applications like switched-mode power supplies, traction motor control, and induction heating. Availability of affordable, reliable IGBTs is an important enabler for electric vehicles and hybrid cars. These devices are also used in buck and boost converters.

Although the IGBT is newer than the power bipolar or power MOSFET transistor, it has gained wide acceptance in the electronics industry. IGBTs are used in a variety of low and medium voltage applications like theatrical lighting, factory automation, and industrial drive control. By low and medium voltage, we are talking about voltages ranging from 50 to 500 volts. Some of the newest IGBT designs are capable of voltages even higher, up to 1,000 volts in some cases. The advantage of an IGBT is that it has a relatively low "on" resistance in a high voltage application. Power MOSFETs tend to have higher "on" resistance values the higher the breakdown voltage. IGBTs can also switch more quickly than a standard power MOSFET. Since the gate region in an IGBT is small relative to a power MOSFET, the device can turn on more quickly. Figure 1 shows an example of a packaged IGBT device.

Figure 1- Example of an IGBT (courtesy IXYS).

Figure 2 shows a cross-sectional view of the IGBT. The structure is very similar to that of a vertically diffused MOSFET featuring a double diffusion of a p-type region and an n-type region. An inversion layer can be formed under the gate by applying the correct voltage to the gate contact as with a MOSFET. The main difference is the use of a p+ substrate layer for the drain in the IGBT. The effect is to change this into a bipolar device as this p-type region injects holes into the n-type drift region.

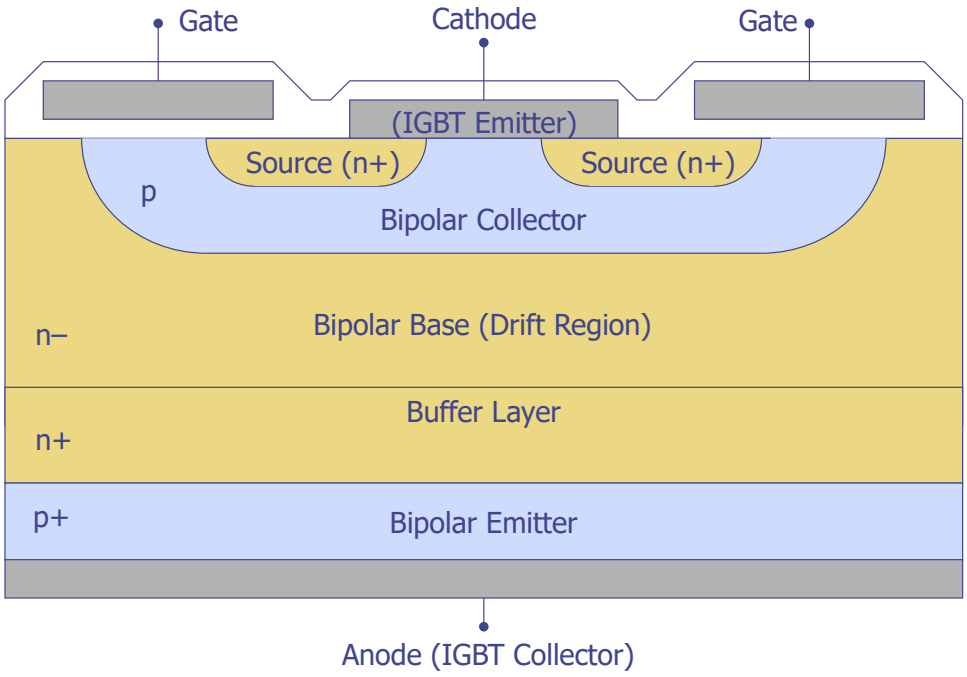

Figure 2- Cross-section diagram showing the layers in a typical IGBT.

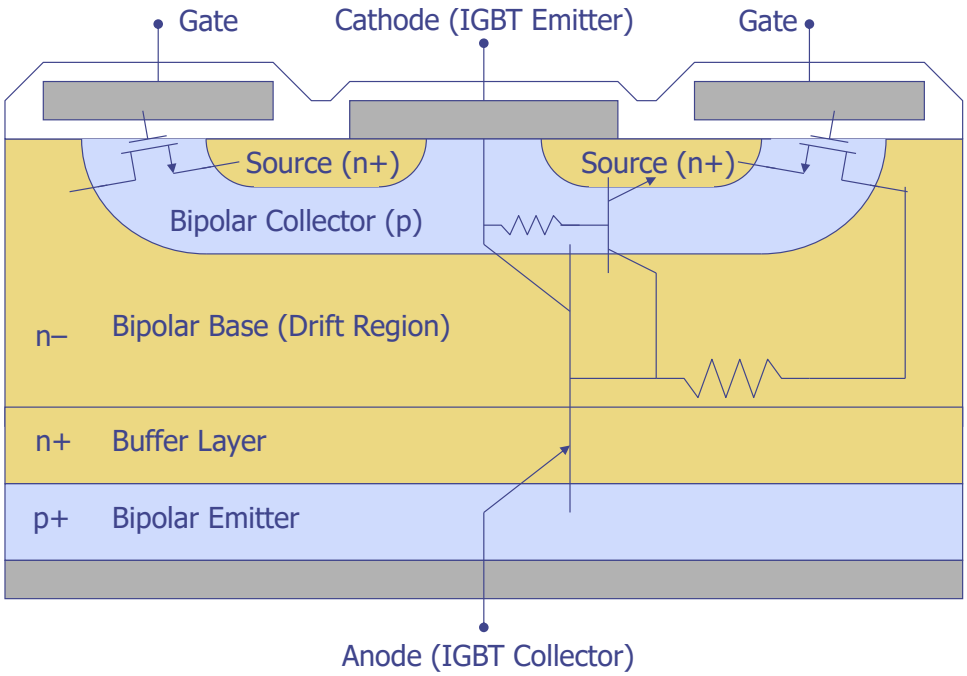

Figure 3- Cross-section diagram of the equivalent circuit associated with the IGBT.

Figure 3 shows the equivalent circuit for the IGBT. The on/off state of the device is controlled, as in a MOSFET, by the gate voltage VG. If the voltage applied to the gate contact is less than the threshold voltage, there is no inversion layer and the device is turned off. When this is the case, any applied forward voltage will occur across the reversed biased collector-base junction. The only current will be a small leakage current. The forward breakdown voltage is determined by the breakdown voltage of this junction. This is an important factor, particularly for power devices where large voltages and currents are being dealt with. The breakdown voltage of the one-sided junction is dependent on the doping of the lower-doped side of the junction; i.e. the n- side. This is because the lower doping results in a wider depletion region and thus a lower maximum electric field in the depletion region. It is for this reason that the n- drift region is doped much lighter than the p-type body region. The n+ buffer layer is often present to prevent the depletion region of collector-base junction from extending right to the p bipolar collector. However, the inclusion of this layer drastically reduces the reverse blocking capability of the device as this is dependent on the breakdown voltage of the buffer layer emitter junction, which is reverse biased under reverse voltage conditions. The benefit of this buffer layer is that it allows the thickness of the drift region to be reduced, thus reducing on-state losses. On state operation is achieved by increasing the gate voltage so that it is greater than the threshold voltage. This results in an inversion layer forming under the gate which provides a channel linking the source to the drift region of the device. Electrons are then injected from the source into the drift region, while at the same time the buffer layer emitter junction—which is forward biased—injects holes into the n- doped drift region. This injection causes conductivity modulation of the drift region where both the electron and hole densities are several orders of magnitude higher than the original n-doping. It is this conductivity modulation which gives the IGBT its low on-state voltage because of the reduced resistance of the drift region. Some of the injected holes will recombine in the drift region, while others will cross the region via drift and diffusion and will reach the junction with the p-type region where they will be collected. The operation of the IGBT can therefore be considered like a wide-base pnp transistor whose base drive current is supplied by the MOSFET current through the channel.

Ask The Experts

Q: What is a Clip QFN?

A: This is a type of QFN where a copper clip replaces the traditional wirebond interconnect for high performance MOSFETs by providing lower resistance and inductance than multiple wirebonds and improves thermal performance. We show this graphically in Figure 1. Clip QFNs combine a copper clip with traditional wirebonds, or multiple clips to completely replace the wirebonds in the package for high performance MOSFETs. The clips provide lower resistance and inductance than traditional wirebonds. This can also improve thermal performance, since the copper clip is capable of conducting more heat from the die to the outside of the package.

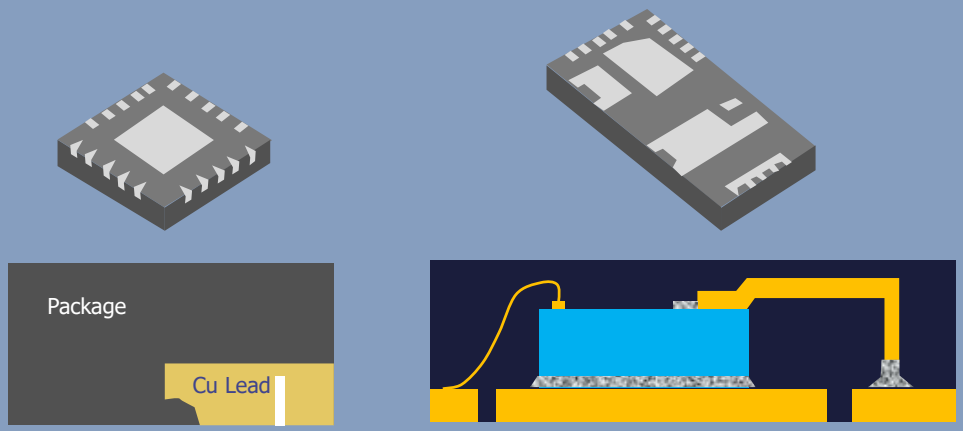

Figure 1- Traditional QFN package and cross-sectional view (left) and a Clip QFN package and cross-sectional view (right). Image courtesy ASE.

Course Spotlight: DEFECT-BASED TESTING

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's application-specific ICs and microprocessors can contain upwards of 100 million transistors. Traditional testing relies on the stuck-at-fault (SAF) to model defect behavior. Unfortunately, the SAF model is a poor model for defects. Other models and strategies are required to catch killer defects on integrated circuits. As transistor sizes decrease, the types and properties of the killer defects change. This has created a number of challenges related to the testing of components. ***Defect-Based Testing*** is a 2-day course that offers detailed instruction on the electrical behavior and test strategies for integrated circuits. We place special emphasis on electrical behavior, fault models, and test techniques. This course is a must for every manager, engineer, and technician working in IC test, IC design, or supplying test hardware and software tools to the industry.

By focusing on the fundamentals of circuit behavior and the impact of defects on circuit behavior, participants will learn how to design, write, and implement test strategies to catch defects. Our instructors work hard to explain semiconductor test without delving heavily into the complex algorithms and computer science that normally accompany this discipline.

Participants will learn basic, but powerful, aspects about defect-based testing. This skill-building series is divided into four segments:

1. **Electrical Behavior of Defects.** Participants will study the electrical behavior of defects. They will learn how open circuits, resistive vias, shorts, and transistor variations affect the electrical behavior of the individual transistor, as well as gate elements and larger blocks.

2. **Fault Models for Defect-Based Testing.** Participants will learn about the historical underpinnings of the stuck-at-fault (SAF) model. They will also learn about other testing models, including IDDQ testing, at-speed testing, and delay testing.

3. **Production Test Methods.** Participants will learn about standard digital testing, SAF testing, IDDQ, timing, low voltage tests, and other types of stress tests. They will explore the strengths and weaknesses of each test type.

4. **The Economic and Quality Impact of Defect-Based Testing.** Participants will learn how defect-based testing can actually improve test economics. They will also study the impact on quality and reliability.

COURSE OBJECTIVES

1. This course will provide participants with an in-depth understanding of defect-based testing and its technical issues.

2. Participants will understand the basic concepts of test economics, yield, test time, and the cost of test. They will also learn how defect-based testing can reduce the possibility of failures in the field.

3. This course will identify underused test techniques like IDDQ and Very Low Voltage (VLV) test techniques that can successfully find defects that are difficult to catch using conventional test techniques.

4. This course will offer the opportunity to discuss specific test problems with our expert instructors.

5. Participants will be able to identify basic and advanced principles for defect-based test.

6. Participants will understand the difficulties in extending IDDQ testing to leading edge products, and how to overcome some of these limitations.

7. Participants will become familiar with Design for Test (DFT) and Automatic Test Pattern Generation (ATPG) tools used for defect-based testing.

8. This course will introduce fundamental and advanced concepts related to extending defect-based testing to future designs.

9. Participants will learn what tools are available today to implement defect-based testing.

COURSE OUTLINE

DAY 1

1. What is Defect-Based Testing?
    a. Introduction
    b. Terminology
    c. Existing test techniques

2. CMOS IC Defect Mechanisms and Detection Techniques
    a. Normal transistor and gate behavior
    b. Sources of random and systematic defects
    c. Types of Defects and How to Detect Them
        i. Bridging defects
        ii. Resistive defects
        iii. Open circuit defects
        iv. Delay defects

3. Fault Models for Defect-Based Test
    a. Stuck-at-fault (SAF)
    b. Delay fault

DAY 2

    c. Leakage fault
    d. Methods for implementing fault models
    e. Existing software tools

4. Production Test Methods
    a. Functional testing (At-speed testing)
    b. IDDx Testing
    c. Timing Test
    d. Low Voltage Testing
    e. Stress Testing

5. Defect-Oriented test Economics and Product Quality
    a. Test set reduction
    b. Effectiveness in catching defects
    c. Yield and fallout

6. Case Histories

Upcoming Courses:

Public Course Schedule:

Defect-Based Testing - November 18-19, 2024 (Mon.-Tues.) | Munich, Germany - $1,195 until Mon. Oct. 28

EOS, ESD and How to Differentiate - November 20-21, 2024 (Wed.-Thurs.) | Munich, Germany - $1,195 until Wed. Oct. 30

Wafer Fab Processing - November 25-28, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Nov. 4

Failure and Yield Analysis - December 2-5, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Nov. 11

Semiconductor Reliability and Product Qualification - December 9-12, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Nov. 18

Semiconductor Technology Overview - February 3-4, 2025 (Mon.-Tues.) | Phoenix, Arizona - $1,195 until Mon. Jan. 13

Product Qualification Overview - February 5, 2025 (Wed.) | Phoenix, Arizona - $595 until Wed. Jan. 15

IC Packaging Technology - February 10-11, 2025 (Mon.-Tues.) | Phoenix, Arizona - $1,195 until Mon. Jan. 20

Advanced CMOS/FinFET Fabrication - February 19-20, 2025 (Wed.-Thurs.) | Phoenix, Arizona - $1,195 until Wed. Jan. 29

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We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!