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Semitracks Monthly Newsletter

Basic Overstress Protection Circuits

By Christopher Henderson

Most semiconductor components are sensitive to overstress. In fact, up to 40% of failed devices returned for analysis are classified as overstress. Since overstress is a mechanism that is so pervasive in the electronics industry, design engineers must consider methods to protect against this problem.

There are five overarching strategies to protect semiconductor devices and integrated circuits from overstress. The first strategy is to limit current through small devices. The most obvious devices that must be protected are input transistors in CMOS circuits. Other transistors that are sensitive are the inputs to differential amplifiers. The second strategy is to ensure that alternate paths exist that can channel the current around sensitive circuits. The most common manifestation of this is the input protection diode. The third strategy is to minimize supply resistance and maximize the capacitance. By minimizing supply resistance, less opportunity exists for the high current discharge creating damaging differential voltages on the chip. By maximizing chip capacitance, the device can absorb more of the discharge with a lower resulting voltage. The fourth strategy is to minimize steps and discontinuities. This helps to prevent regions of field concentration that initiate damage. The final strategy is to identify and minimize parasitic effects. Parasitic transistors, diodes, and resistors can allow voltage and current to couple to sensitive devices that might otherwise be isolated. We'll take a quick look at a couple of these strategies, and some representative circuits, below.

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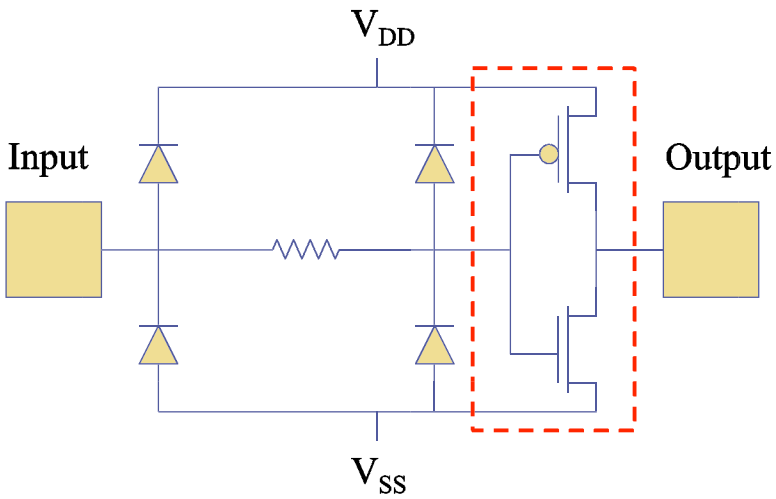

Figure 1. Basic input protection scheme.

This circuit describes a basic approach to protecting a sensitive circuit. The inverter circuit, shown inside the dashed box, contains transistors sensitive to voltage pulses. In a modern circuit, even voltages as low as 5 volts can potentially damage the gates and junctions. To protect the transistors, designers often use input protection diodes and resistors. The resistor shown in the figure will limit the current into the sensitive gate, while the diodes ensure that alternate current paths exist, should the voltage on the input go significantly above or below VDD or VSS. In this circuit, the implant-to-well, and the implant-to-substrate diodes in the source regions of the p- and n-channel transistors serve the same purpose for the output; they shunt the current around the transistor should the output go significantly above VDD or below VSS. However, this does require that the transistor junctions be quite large to handle the energy dissipation.

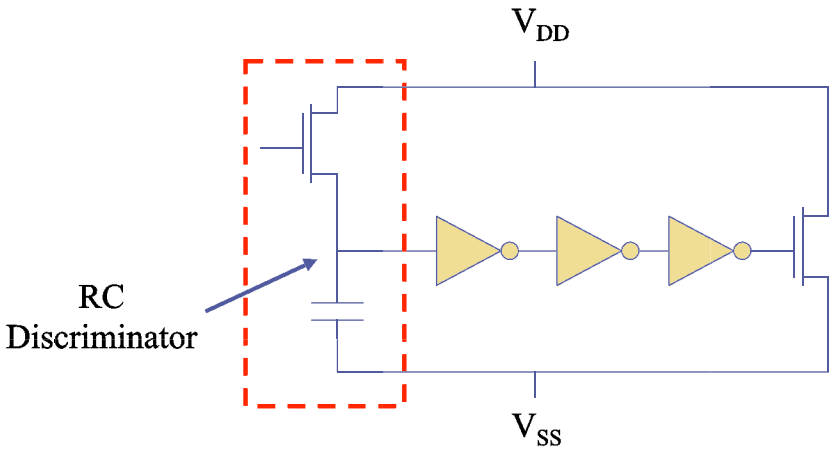

Figure 2. Basic circuit that provides frequency triggered protection for the chip power supply.

In addition to protecting the input and output pins, the entire power supply network may require some protection for larger pulses that raise the voltage on the entire chip. These circuits are known as clamps. Overstress clamps can be initiated by voltage or frequency triggering. The objective is to not be activated during circuit power up and power down, not to interfere with system functionality, but only activate during the overstress event. Frequency triggered overstress power clamps remain off during dc phenomenon but respond to the ac signal induced by the EOS or ESD pulse event. This is an example of a frequency-triggered clamp. The portion of the circuit outlined in blue is the RC discriminator that determines what range of ac events should trigger the MOSFET clamp on the right end of the circuit.

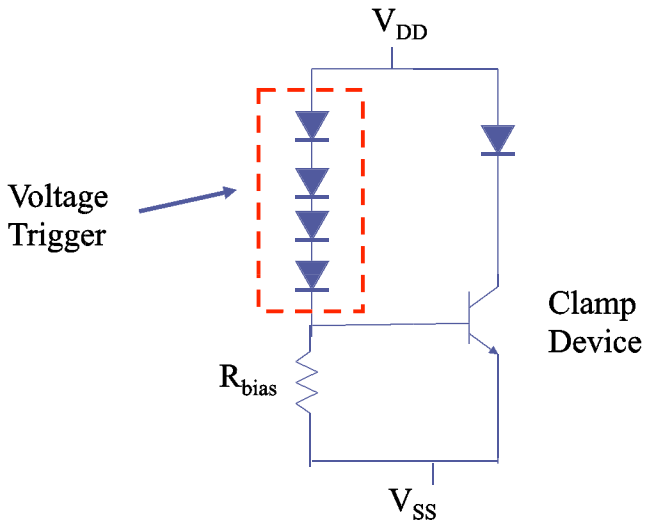

Figure 3. Example of a voltage-triggered clamp.

Voltage triggered overstress power clamps remain off during normal voltage conditions and chip operation, but turn on when a voltage condition is exceeded. This can be an over-voltage condition, overshoot, or undershoot phenomenon or any high current event. This particular structure triggers when the voltage on VDD exceeds the four diode drops, highlighted here in the voltage trigger, and the one in the base-emitter junction of the clamp device, or approximately 3.5 volts total. The bipolar clamp device then turns on, collapsing the VDD rail voltage.

In conclusion, we showed some basic overstress protection circuits. This is an important aspect of the design, as these circuits protect against a common failure mechanism endemic to almost all circuits and applications. There are many different circuit design techniques to protect against these problems. If you are interested in learning more about this topic, we encourage you to consider attending our upcoming course on ESD and Latchup Design and Technology. If you are involved in failure analysis or product engineering, we encourage you to consider our upcoming course on EOS, ESD - Can Failure Analysis Differentiate? You can find more details for both courses on our web site.

Technical Tidbit

Bosch Deep Reactive Ion Etch Process

In recent years, Microelectromechanical Systems (MEMS) have seen rapid growth as companies insert them into various applications. One particularly important technical processing breakthrough that has facilitated the proliferation of MEMS is the Bosch Deep Reactive Ion Etch (DRIE) process. The Bosch DRIE process was developed by scientists working for the etch's namesake, Robert Bosch GmbH. The Bosch etch is a process that allows precise control of the etch anisotropy by alternating two steps. The first step is the standard isotropic plasma etch using sulfur hexafluoride [SF_6]. The second step is the deposition of a Teflon-like passivation layer composed of (C_4F_8). The next SF_6 etch step removes the passivation layer from the bottom of the trench, but leaves the passivation on the sidewalls of the trench. The result is a truly vertical sidewall trench. When one examines the trenches closely in cross section, the sidewalls have a characteristic scalloped profile that is 100 – 500nm in depth. The Bosch etch can achieve etch rates of several microns per minute.

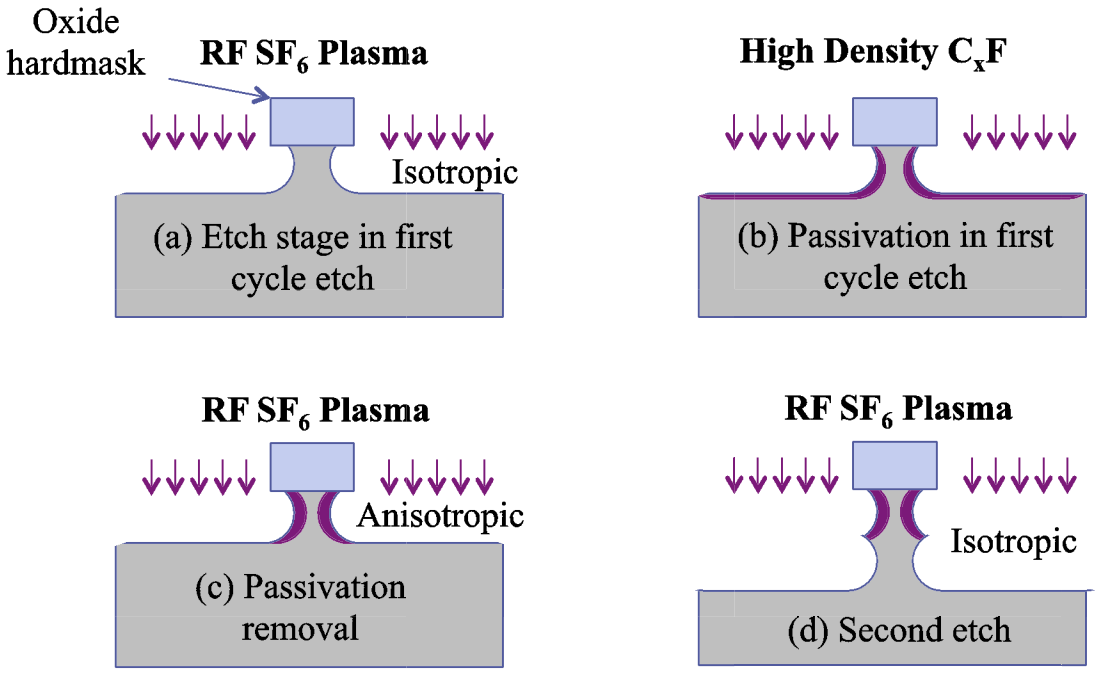

Figure 1. Graphic depicting steps in the Bosch DRIE process.

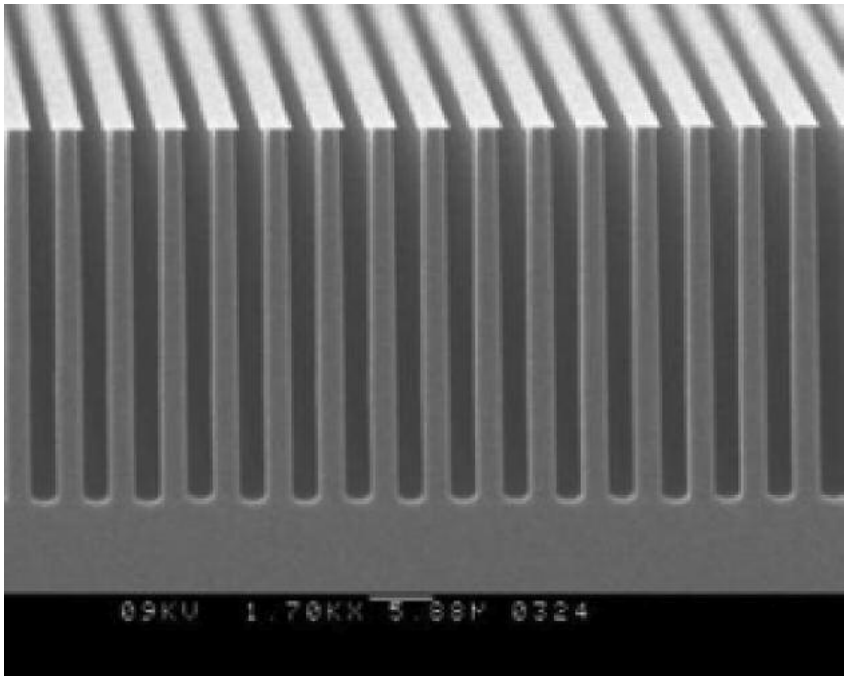

Figure 2. Results of Bosch DRIE on a silicon structure.

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Q: I am considering signing up for your Online Training System, but have a question. If I have a question about the materials, is there a way to contact anyone?

A: Yes there is. The author of the presentation can be directly contacted through the email link that is embedded in the presentation. In the upper left under the picture of the author, simply click on "email" and the interface will present a link allowing you to email the author.

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Today's 3-dimensional packages are increasingly used in mobile applications, but are they safe in an ESD environment? Be sure to join our webinar to learn more about this topic. If you are interested in attending this webinar, or if you are interested in having this done as an in-house course for your staff, please feel free to contact us at (505) 858-0454, or at info@semitracks.com.

WEBINAR OVERVIEW

This webcast will discuss electrostatic discharge (ESD) in 2.5-D and 3-D multi-chip systems. With the desired for high bandwidth, performance, and density, there is tremendous industry growth in this field. The new "3-D chip paradigm" extends into chip architecture; as a result it influences chip floor planning, placement, and integration. Since the "3D chip paradigm" affects chip architecture, electrostatic discharge (ESD) and latchup are influenced. ESD design, placement, electronic design automation (EDA), checking, verification, integration, test, and manufacturing assembly issues will be highlighted in this webcast.

The webcast will review where we have been in the past, and where we are in the present, and where we are going into the future. The early development of active chip carriers, and three-dimensional systems will be first discussed, as well as the questions, paradigms, problems, patents, and innovations. Multi-chip semiconductor chip implementations, with and without "through silicon vias" (TSV) will be discussed from an ESD and latchup perspective, highlighting advantages, disadvantages, and opportunities for innovation. With the new 3-D multi-chip structures, new ESD paradigms exist in the area of ESD design, simulation, testing, standards, and handling in both manufacturing and final test.

WEBINAR OUTLINE

1. Multi-chip Structures and the Paradigm Shift
2. Early Three Dimensional (3-D) Structures
3. 2.5 D Multi-chip Systems
4. 3 D Systems
   a. Through Silicon Vias (TSV)
5. JEDEC Wide I/O Footprint and ESD
6. ESD in 3-D
   a. ESD Issues, Questions and Paradigms
   b. ESD Architecture – Power Grids
   c. ESD Architecture - ESD Power Clamps
   d. Electronic Design Automation (EDA)
7. Summary and Conclusions

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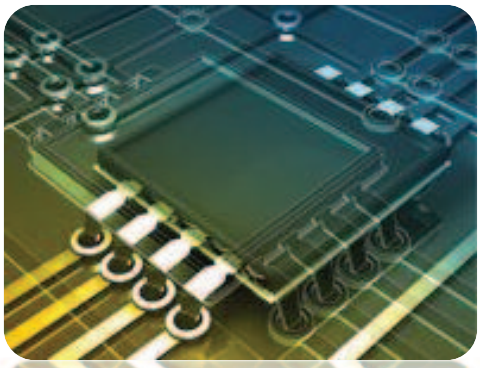

Upcoming Courses

(Click on each item for details)

EOS, ESD and How to Differentiate
November 7 – 8, 2012 (Wed – Thur)
San Jose, California

Polymers in Electronics/FTIR
November 7 – 8, 2012 (Wed – Thur)
San Jose, California

IC Packaging Metallurgy
December 3 – 5, 2012 (Mon – Wed)
Penang, Malaysia

Semiconductor Reliability
January 23 – 25, 2013 (Wed – Fri)
San Jose, California

Failure and Yield Analysis
January 28 – 31, 2013 (Mon – Thur)
San Jose, California

Upcoming Webinars

(Click on each item for details)

3-Dimensional ICs and ESD Issues
December 18, 2012 (Tue) • 11:00 A.M. EST

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