Issue 41 November 2012

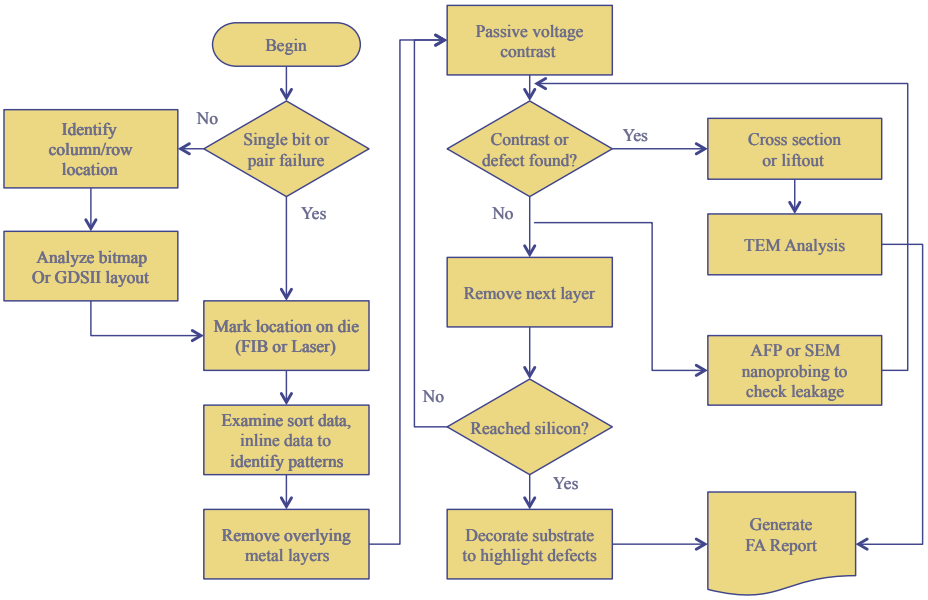
InfoTracks

Semitracks Monthly Newsletter

Failure Analysis Procedures – Part I

By Christopher Henderson

This article begins a series of five articles on Failure Analysis Procedures. I am often asked about flowcharts for FA. A flowchart describing the process for failure analysis can be useful, especially for individuals new to failure analysis. There are different ways to develop flowcharts for failure analysis. One of the more common methods is to create flows around various electrical failure modes. Here is an example of an FA flow procedure for a static random access memory device, or an IC with a failure in the memory section.



In this Issue:

We begin by identifying the type of memory failure. If the failure is a single bit failure or a bit pair failure, one can go straight to the electrical to physical bitmap conversion diagram to physically identify the location of the failing bit or bit pair. If the failure is not a single bit failure, then one should try to identify the row or column involved, or ascertain the pattern involved in the failure. One can then analyze the bitmap or the GDSII file to identify potential points of failure, and mark them for further analysis. This mark is normally placed on the front side of the device, but could be made on the backside, if one decides that a backside approach is preferred. At this point, it can also be useful to look at similar failures for patterns. This can be accomplished by looking a wafer sort data, bitmap data, and inline parametric test data. Once the sample is identified and marked, and other samples identified and marked, we can begin more destructive steps. This involves removing the overlying layers to expose the cells of interest. The metal layers obscure the bits, and our ability to image defective conditions. Once the metal layers are removed, and the metal-1 or polysilicon layers are exposed, we can perform passive voltage contrast to help localize and verify the problem row or column metal, or cell/cells. If we find a defect, then we can perform a cross-section of the problem area, or remove the section and analyze it with the higher magnification transmission electron microscope. If we don't see the defect with passive voltage contrast we can try Atomic Force Probing or SEM nanoprobing to check for leakages. If we are still not seeing a defect, then it makes sense to remove the next layer and look at it with the same tools and techniques. We can continue this process until we locate the defect, or reach the silicon. Once we reach the silicon, we can decorate the substrate with an etch to highlight potential defects.

Is this method foolproof? The answer is "no," but it does provide a worthwhile construct in which to perform an analysis. Again, these constructs can be useful for new analysts, but we need to emphasize that some failures may lie outside the context of this framework. In the next issue, we'll discuss a failure analysis flowchart for a scan-based failure.

Ask the Experts

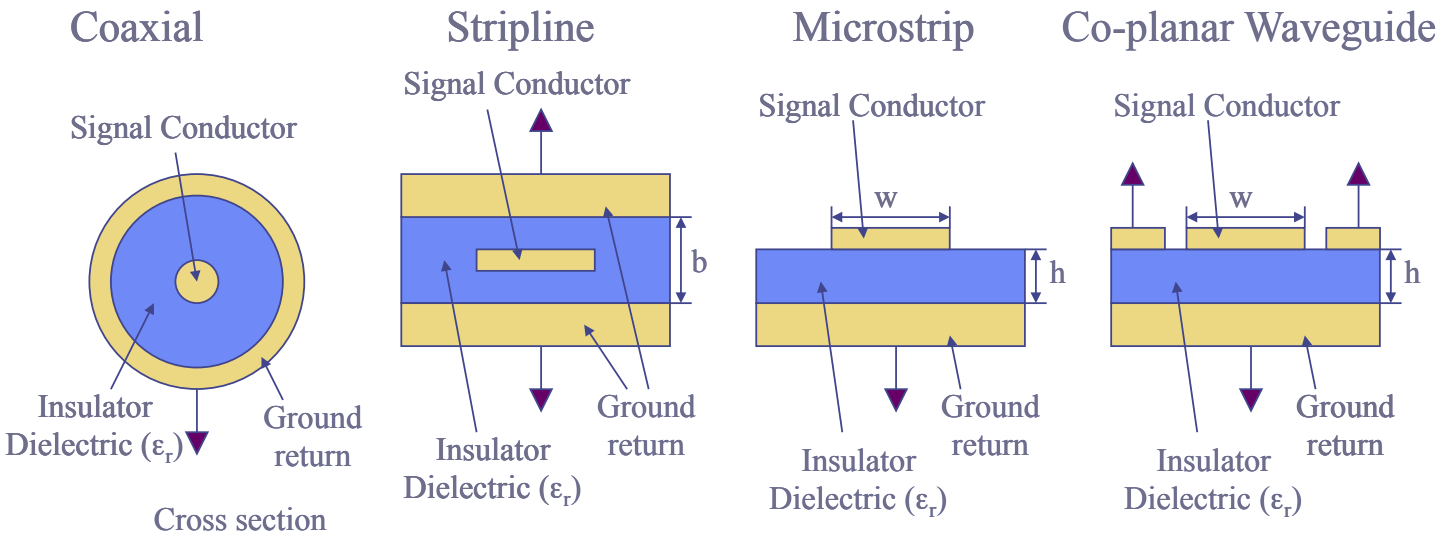
Q: Machine Model (MM) and Human Body Model (HBM) are common ESD testing requirements for power amplifier/low noise amplifier, but is Charge Device Model (CDM) also necessary during qualification?

A: CDM is an important test method when the products you produce will go through a lot of automated assembly and testing. I am not sure if that is the case for your products. You may have to check with your product engineers to determine which markets your parts go into. In general, power amplifiers would not be as sensitive to CDM damage as low noise amplifiers, but most amplifiers have ESD-sensitive inputs.

Technical Tidbit

Transmission Lines

As systems operate at increased frequencies, the transmission of signals becomes important. In the 1-10 megahertz (MHz) range, signal integrity is not normally an important issue, but above 100 MHz it becomes more important. Above 1 GHz signal integrity is highly important, and even paramount in some applications. How do engineers propagate signals through electronic systems faithfully? This is normally accomplished with good transmission line design. There are four types of transmission lines commonly used in electronic systems: coaxial, stripline, microstrip, and co-planer waveguide. The figure here shows cross-sections of the four types of transmission lines.



Coaxial is common at the system level to help shield from noise, while the other three are more common at the module or chip level. Stripline and microstrip are relatively easy to implement in conjunction with the dielectric layers on a chip. Stripline requires more layers, as it uses a top shielding layer. Microstrip uses less layers, but doesn't provide the noise immunity of coaxial or stripline. For the highest frequencies, engineers use co-planar waveguides. A co-planar waveguide uses the same structure as a microstrip, but adds grounded conductors on either side of the signal line for signal integrity. This topic is an extensive topic; there are numerous papers on this subject for integrated circuits and system-in-package devices. For more information we encourage the reader to examine "Transmission Line Design Handbook" by Brain Wadell, or "High Speed Digital Design: A Handbook of Black Magic" by Howard Johnson and Martin Graham.

Professional Development Opportunities at IEDM 2012

2012 IEEE International Electron Devices Meeting

Hilton San Francisco Union Square
December 10 – 12, 2012

- Technical Tutorials
  Saturday, December 8, 2012
- Short Courses
  Sunday, December 9, 2012

Semitracks will be in attendance at the

2012 IEEE International Electron Devices Meeting

December 10 – 12

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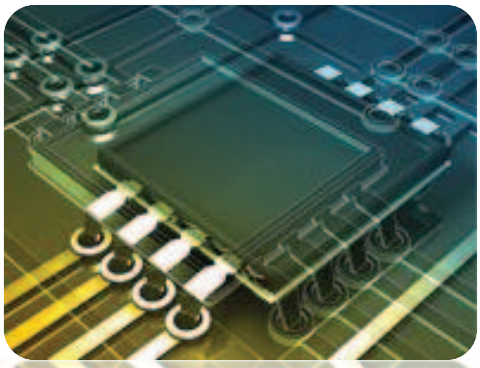

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

IC Packaging Metallurgy
December 3 – 5, 2012 (Mon – Wed)
Penang, Malaysia

Fault Isolation
January 21 – 23, 2013 (Mon – Wed)
Penang, Malaysia

Semiconductor Reliability
January 23 – 25, 2013 (Wed – Fri)
San Jose, California

Failure and Yield Analysis
January 28 – 31, 2013 (Mon – Thur)
San Jose, California

EOS, ESD and How to Differentiate
February 4 – 5, 2013 (Mon – Tues)
San Jose, California

Polymers in Electronics / FTIR
February 4 – 5, 2013 (Mon – Tues)
San Jose, California

Upcoming Webinars

(Click on each item for details)

3-Dimensional ICs and ESD Issues
December 18, 2012 (Tue) • 11:00 A.M. EST