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INFOTRACKS

YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Semiconductor Cleanroom Technology

By Christopher Henderson

In this month's Feature Article, we will conclude our discussion of Cleanroom Technology. This Article covers the wafer carriers that Automated Material Handling Systems transport.

By way of review, historically, fab operators used the SMIF, or Standard Mechanical Interface Pod to transport wafers. We show an example of a SMIF pod in Figure 1. The SMIF pod is an isolation technology developed in the 1980s by engineers at Hewlett-Packard in Palo Alto. The SMIF pod was initially used in semiconductor wafer fabrication and cleanroom environments for 150mm wafers, and is currently used for 200mm wafers as well. There is also a SEMI standard for SMIF dimensions, construction, and use. As a point of interest, the leader of the SMIF development team went on to start Asyst Technologies, with a license for the SMIF technology from SEMI. Asyst Technologies was later purchased by Brooks Automation, and Brooks Automation still sells SMIF pods for the industry, as of this writing.

WHAT'S INSIDE?

Want to take control of your learning? See page 08

Upcoming Courses:

- Failure and Yield Analysis
- Semiconductor Reliability and Product Qualification

See page 12 for more details

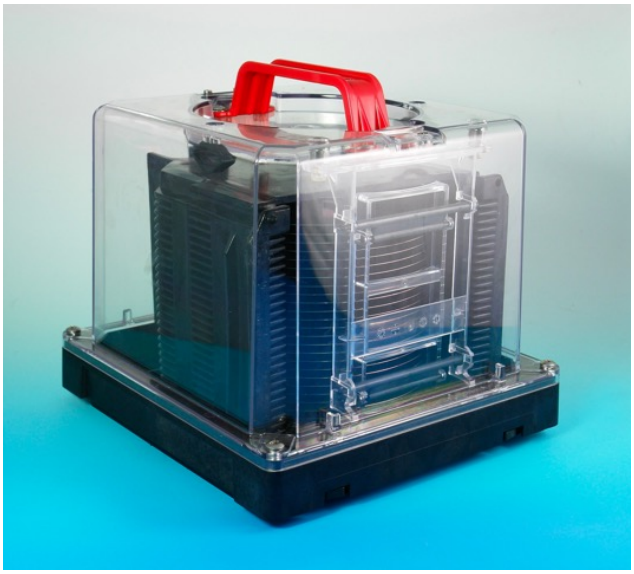


Figure 1- Example of a Standard Mechanical Interface (SMIF) Pad

Now let's discuss the Front Opening Unified Pod, or FOUP. This carrier is a replacement for the SMIF pod, and is designed to handle larger wafers. There are four main purposes of the FOUP. The first, and most obvious one, is for the transportation of wafers. The FOUP can carry up to 25 wafers at a time. Second, the FOUP protects the wafers from the environment. Even though FOUPs are used in a cleanroom, they can sometimes serve as a transportation vehicle between areas where the cleanliness levels might not be as high as the typical cleanroom. Third, the FOUP is designed to be used in such a way as to prevent lifting injuries to personnel. A FOUP containing 25 wafers can weight more than 20 pounds, or 9.5 kilograms, which can lead to injuries. FOUPs are designed to be used with AMHS equipment, so that the fab operators do not have to lift the FOUP. Fourth, FOUPs are designed to interface to process tools, so that the robotics within the process tool can remove and replace the wafers from the FOUP at the start and end of the process step or steps. FOUP technology was developed at the same time as the development of 300mm wafer processing in the early 1990s. FOUPs began to appear in production lines along with the first 300mm wafer processing tools in the mid 1990s. The size of the wafers and their comparative lack of rigidity meant that SMIF pods were not a viable form factor. FOUP technology is planned for use with 450mm wafers, should they ever go into volume production. Several FOUP SEMI standards, including SEMI E47.1-1106, are related to both 300 and 450mm wafers. We show an example of a FOUP in Figure 2.

Figure 2- Front Opening Unified Pod (image courtesy Entegris)

FOUPs are made from a specialized plastic, are designed to hold silicon wafers securely and safely in a controlled environment, and allow the wafers to be transferred between machines for processing or measurement. FOUP standards were developed by SEMI and SEMI members to ensure that FOUPs and all equipment that interacts with FOUPs work together seamlessly. In making the transition from a SMIF pod to a FOUP design, engineers replaced the removable cassette used to hold wafers with fixed wafer columns. The engineering development team relocated the FOUP door from a bottom orientation to a front orientation, where automated handling equipment can access the wafers. They designed the pitch for a 300mm FOUP to be 10mm, while they designed 13 slot FOUPs to have a pitch up to 20mm. As we mentioned before, the weight of a fully loaded 25 wafer FOUP is between 7 and 9 kilograms which means that automated material handling systems are essential for all but the smallest of fabrication plants. To allow this, each FOUP has coupling plates and interface holes to allow the FOUP to be positioned on a load port, and to be picked up and transferred by the AMHS to other process tools or to storage locations such as a stocker or undertrack storage. FOUPs may use RF tags that allow them to be identified by RF readers on tools or AMHS. FOUPs are also available in several colors, depending on the customer's wish. Finally, FOUPs have begun to include the capability to have a purge gas applied by the process, measurement and storage tools to reduce particle contamination during transport and storage, in an effort to increase device yield.

In addition to FOUP movement and storage, some AMHSs also accommodate Reticle Storage Pods, or RSPs which are used due to the sensitivity of the reticle to damage from the environment. By way of background, the reticle is the structure which is used in the lithography process to define the layers on the chip. A reticle has to be stepped and repeated in order to expose the entire wafer. This is in contrast to the term "mask". Compared to a reticle, a mask is used to refer to a pattern that could be printed in a single exposure to cover the entire wafer without any optical de-magnification. However, today, the terms reticle and mask are often used interchangeably. Each chip requires between 20 and 40 masks for the lithography process, so in a modern fab, there can be thousands of masks that are moved around and require storage. The finer the lithographic patterns, the greater the risk reticle contamination poses. Potential contamination sources include both foreign particles and chemical residues. Reticle coatings are delicate and easily damaged. Anything that touches a reticle, whether

it is an expected part of the process such as a robot arm in the fab or an unexpected contaminant such as a human hair, has the potential to cause damage. Reticles used for EUV lithography rely on reticle pods for safe storage and to protect them during lithographic patterning, inspection, cleaning, and repair. The protective pod must last for many years without introducing unwanted contamination or physical damage. Pods designed for 193nm immersion lithography are not sufficient to protect EUV reticles. The unique requirements of EUV lithography pose additional constraints and demands on pods, making the EUV reticle pod a highly specialized piece of equipment with multiple critical components. For older forms of lithography, including immersion lithography, the reticles rely on pellicles to act as "dustcovers" that protect reticles from particle contamination during pattern exposure. Pellicles need to be optically transparent, which in the case of EUV lithography means that they must be transparent to light in the EUV spectrum with wavelengths around 13.5nm. Most existing pellicle film materials absorb EUV light, but the semiconductor industry is starting to implement EUV-specific pellicles. There are both single and multiple reticle storage pods, like we show in Figure 3.

Figure 3- Single (left) and multiple (right) Reticle Storage Pods (RSPs) (images courtesy Entegris)

In conclusion, the AMHS is now an integral part of modern fabs. All new 300mm fabs in operation or under construction use an AMHS. There are a number of different components that are part of an AMHS. The major components include the Overhead Transport System, Overhead Shuttles, Automated Guided Vehicles, Carrier Stockers, and Tool Front FOUP Buffers. The AMHS transports and stores two types of carriers. The first is the Front Opening Unified Pod (FOUP), used to hold wafers, and the second is the Reticle Storage Pod (RSP), used to hold reticles. The AMHS will likely be used for the foreseeable future, as automation and cleanliness continue to drive modern semiconductor cleanroom manufacturing.

In next month's Feature Article, we will start a new topic, so stay tuned.

Technical Tidbit: Embedded Resistors

In this month's Technical Tidbit, we will discuss embedded resistors. The increase in component density and the requirement for higher performance electronic devices are driving the development of electronic systems with passive devices, such as capacitors, resistors, and inductors, embedded in the PCB or IC package. The benefits of embedded passives are the freeing up of surface space for active devices, improving performance with lower inductance and improved signal quality. Embedded passives yield a more reliable printed circuit board by reducing the number of solder joints and reduce overall cost. In this article we will focus on embedded resistors. There are two main technologies for embedded resistors: thin film and thick film. The thin film technology has many advantages over thick film because thin film technology uses vacuum deposition, such as sputtering, which gives excellent coating consistency and thickness uniformity. Figure 1 shows the process flow for a typical embedded resistor technology.

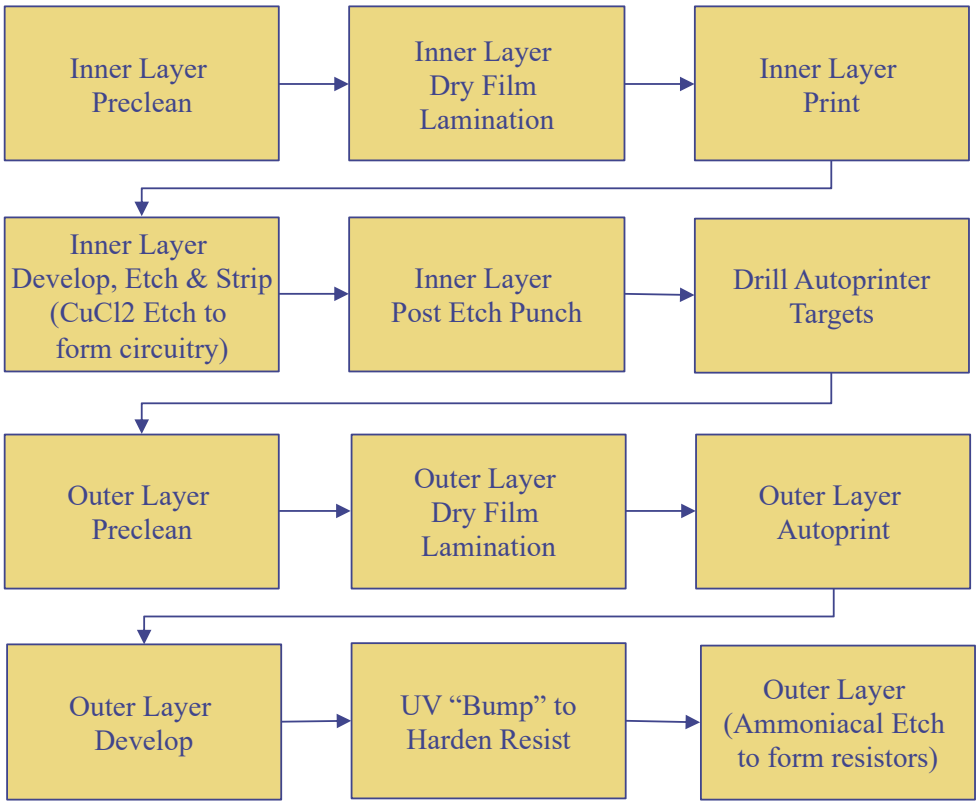


Figure 1- Process for creating embedded resistors in a printed circuit board.

Next, let's discuss the processing methods for the resistive material itself. The first is the conductive polymer coating method. This technique utilizes either graphite or carbon black as the resistive material. Chemists use phenolic resins, benzoguanamine resins, or other epoxy resins as binders to hold the graphite or carbon black in place. They may use a talc powder known as Pulvistalci, titanium dioxide, or silicon dioxide as a filler material, and ethyl acetate, methanol, or ethanol as a solvent to dilute the resistive material for dispensing. The second is a chemical plating method. Chemists use nickel phosphide for the plating material, and copper foil for the substrate. The third is a chemical vapor deposition method using a recipe originally known as Insite™ from Shipley Chemicals. The CVD process involves depositing a titanium layer on copper. The product lines from Shipley are now part of Dow Chemical. The fourth is Physical Vapor Deposition, or PVD. There are a number of materials that can be deposited as resistive material with PVD. They include NiCr, SiCr, AlSiCr, TaN, TaAl, TiSi, TiW, TiN, and others.

PVD thin-film resistive material is the most common type of embedded resistor material used in the industry. Thin-film resistive material is supplied in sheet form with resist values that range from 25Ω per square area to 1kΩ per square area. Thin-film laminates are comprised of a layer of resistive material deposited onto copper foil. The foil is then laminated onto the B-stage base material with the resistor surface side facing the base laminate. Following the first stage chemical etching process to define the overall circuit pattern, a second etching process selectively ablates a portion of the copper to expose the resistor element. We show these steps graphically in Figure 2.

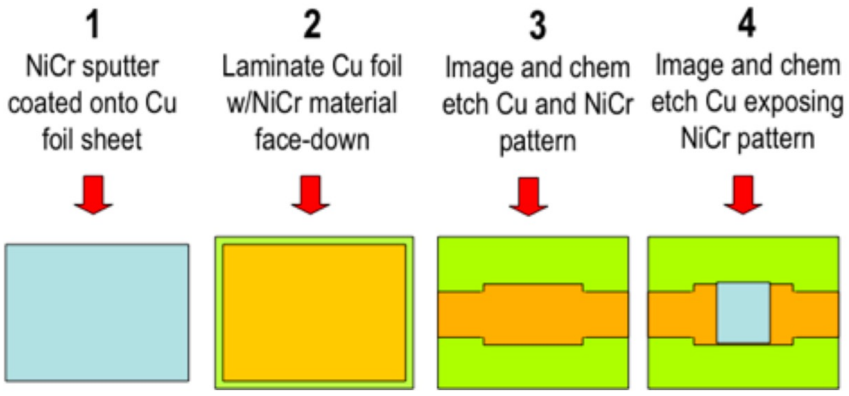


Figure 2- PVD Thick and Thin Film Resistor Process

When selecting the components for embedding with either thick-film or thin-film process, the designer must first select a base value that can enable the widest number of resistor elements. Thick-film and thin-film materials are available in a number basic resistance values.

Two examples of thick-film resistor materials would be Polymer Thick Film, or PTF, and Ceramic Thick Film, or CTF resistors. The paste-like PTF material is available in resistance values that range between 1Ω and 1 MΩ per square, while the CTF materials value will range between 10Ω and 10kΩ.

An example of a thin-film resistor material would be TCR™. TCR™ is made by sputtering a thin layer of nickel-chromium alloy onto copper foil. Nickel-chromium alloys possess high electrical resistivity, good electric performance, high thermal stability, and are a well-known chemistry. TCR™ is typically furnished in 25, 50, 100 and 250 Ω/square sheet resistivity variations. Suppliers usually state the basic sheet resistor tolerance to be +/- 5%, but laser trimming can be used to improve resistor tolerance. However, any trimming of the elements must be performed before lamination of additional circuit layers.

Ask The Experts

Q: I cannot find a specific guidance that recommends/defines the thermal condition at production stage for either automotive or industrial applications. By production, I mean the testing of the final packaged products after the assembly process. Do you have any specific training/guidance on that?

A: If I am understanding your question correctly, you are asking about what temperatures to use for testing during Production Testing, correct?

If that is the case, there aren't well-defined standards for what to do when it comes to industrial and automotive products. Many semiconductor suppliers will use the Part Operating Temperature Grade to define the temperatures at which to do final test. Testing at three different temperatures drives up the cost of test significantly though. For industrial applications, this is often determined by the customer's requirements. During the Validation and Characterization stage, there are some useful approaches for determining the range of values one might see during production testing, and then defining a "guardband" to account for the changes between low and high temperatures. One can then do the testing at one temperature with a guardband in place, but this may or may not be something your customer is willing to accept.

To establish a basic correlation between an electrical parameter and the temperature, usually 30 units is good enough. Said another way, if you test 30 units for a parameter like IIL or IIH, the results should produce a normal distribution. 30 units gives you a 90% confidence that you can match the distribution to a normal distribution. As you test an increasing number of units, most electrical parameters will create a normal distribution, but not for all electrical parameters. Parameters such as IDDQ (power supply current) and FMAX (maximum operating frequency) do not produce normal distributions.

Course Spotlight: PACKAGING FAILURE AND YIELD ANALYSIS

OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Our industry needs competent analysts to help solve these problems. ***Packaging Failure and Yield Analysis*** is a 2-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. In this version of the course, we place additional emphasis on package-level Failure Analysis. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a ***Do It Right the First Time*** approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

Participants will learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. The Process of Failure and Yield Analysis. Participants will learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.

2. The Tools and Techniques. Participants will learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools like x-ray radiography, time domain reflectometry, magnetic force imaging, infrared thermography, decapping and sample preparation.

3. Case Histories. Participants will identify how to use their knowledge through the case histories. They will learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

COURSE OBJECTIVES

1. The course will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.

2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.

3. The course will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.

4. The course will offer a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.

5. Participants will be able to identify basic technology features on semiconductor packages.

6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.

7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

COURSE OUTLINE

DAY 1

1. Introduction

2. Failure Analysis Principles/Procedures
    a. Philosophy of Failure Analysis
    b. Flowcharts

3. Gathering Information

4. Package Level Testing
    a. Optical Microscopy
    b. Acoustic Microscopy
    c. X-Ray Radiography
    d. Hermetic Seal Testing
    e. Residual Gas Analysis
    f. Magnetic Current Imaging
    g. Lock-In Thermography

5. Electrical Testing
    a. Basics of Circuit Operation
    b. Curve Tracer/Parameter Analyzer Operation
    c. Quiescent Power Supply Current
    d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
    e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
    f. Automatic Test Equipment
    g. Basics of Digital Circuit Troubleshooting
    h. Basics of Analog Circuit Troubleshooting

DAY 2

6. Decapsulation/Backside Sample Preparation
    a. Mechanical Delidding Techniques
    b. Chemical Delidding Techniques
    c. Backside Sample Preparation Techniques
        i. Warpage Control Techniques
    d. Advanced Disassembly Techniques

7. Package and Die Inspection
    a. Optical Microscopy
    b. Scanning Electron Microscopy

8. Analytical Techniques
    a. Auger
    b. ESCA/XPS

9. Focused Ion Beam Technology
    a. Physics of Operation
    b. Instrumentation
    c. Examples for Packaging FA
    d. Gas-Assisted Etching

10. Case Histories

Upcoming Courses:

Public Course Schedule:

Failure and Yield Analysis - May 13-16, 2024 (Mon.-Thurs.) | Phoenix, AZ - $2,095 until Mon. Apr. 22

Semiconductor Reliability and Product Qualification - May 20-23, 2024 (Mon.-Thurs.) | Phoenix, AZ - $2,095 until Mon. Apr. 29

Fundamentals of High-Volume Production Test - May 20-21, 2024 (Mon.-Tues.) | Phoenix, AZ - $1,195 until Mon. Apr. 29

Advanced CMOS/FinFET Fabrication - September 2-3, 2024 (Mon.-Tues.) | Singapore - $1,195 until Mon. Aug. 12

Packaging Failure and Yield Analysis - September 9-10, 2024 (Mon.-Tues.) | Penang, Malaysia - $1,195 until Mon. Aug. 19

Packaging Failure and Yield Analysis - September 23-24, 2024 (Mon.-Tues.) | Manila, Philippines -$1,195 until Mon. Sept. 2

Defect-Based Testing - November 18-19, 2024 (Mon.-Tues.) | Munich, Germany - $1,195 until Mon. Oct. 28

Wafer Fab Processing - November 25-28, 2024 (Mon.-Thurs.) | Munich, Germany -$2,095 until Mon. Nov. 4

Failure and Yield Analysis - December 2-5, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Nov. 11

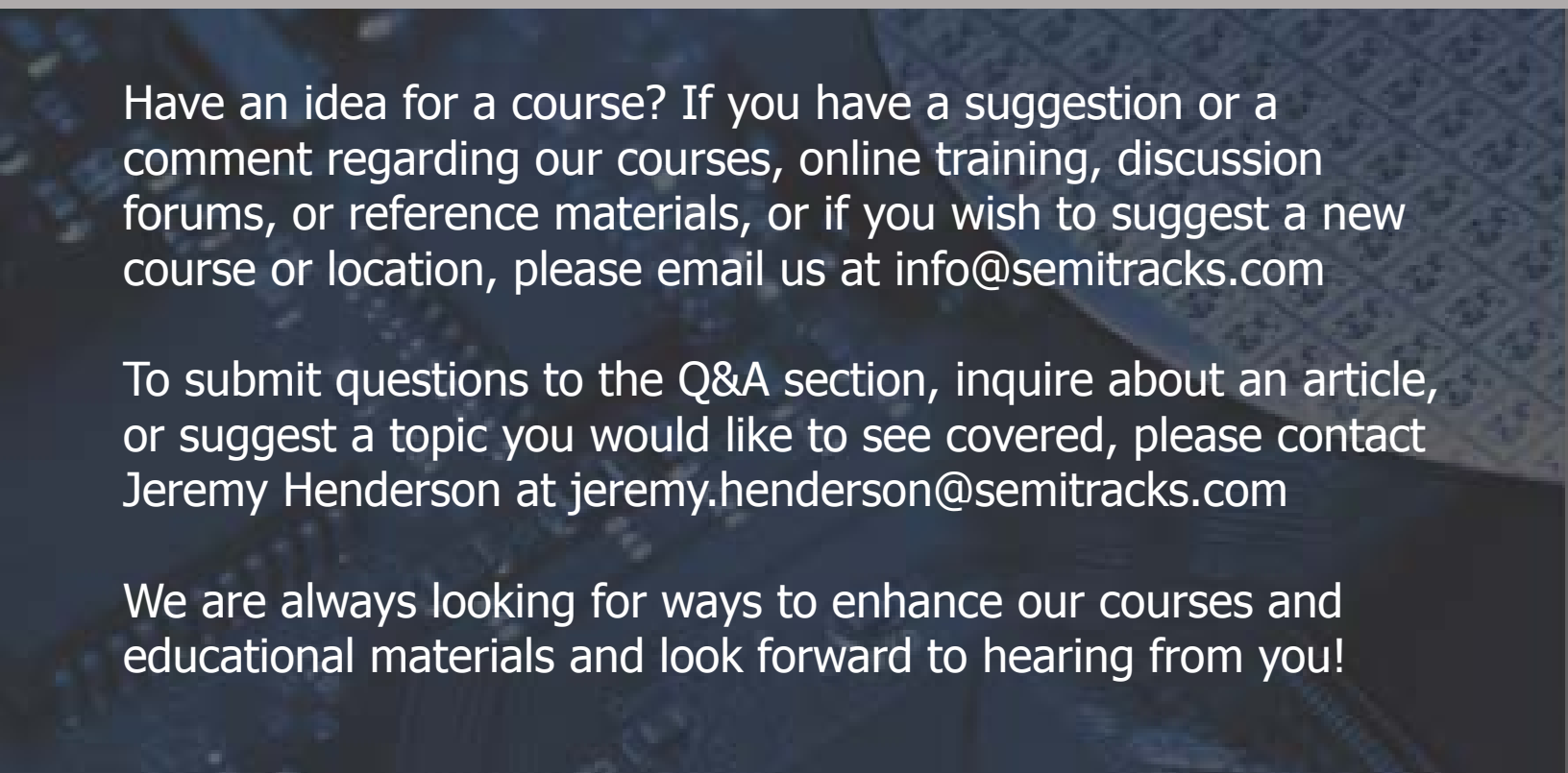
Semiconductor Reliability and Product Qualification - December 9-12, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Nov. 18

Webinar Schedule:

Semiconductor Reliability and Product Qualification Webinar - August 5-8, 2024 (Mon.-Thurs.) | Online at 8:00 AM-12:00 Noon Pacific Time - $600

Advanced CMOS/FinFET Fabrication Webinar - August 19-22, 2024 (Mon.-Thurs.) | Online at 8:00 AM-12:00 Noon Pacific Time - $600

IC Packaging Technology Webinar - August 26-29, 2024 (Mon.-Thurs.) | Online at 8:00 AM-12:00 Noon Pacific Time - $600



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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!