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Bump Processes—Part III

By Christopher Henderson

In Part III this month, we will discuss the redistribution layer process. The drawing on the left shows a standard RDL process flow. We begin by depositing an overlying thick dielectric layer using a material like polyimide or benzocyclobutane. Next we deposit a seed layer, then electro-deposit copper, then nickel, followed by lithography and patterning to create the redistribution metal line. We then deposit a second layer of dielectric and open a window where the bump will be located. We can then place the bump at this new location. The advantages to this process include the ability to use one silicon design for multiple applications and use flip-chip and wafer layer chip scale packages. The disadvantage is that the additional mask layers and processing raise the cost of the circuit and lower the final yield (see Figure 1, next page).

In terms of cost, moving from a situation with the ball directly attached to the pad, or bump on pad, to redistribution without a buffer dielectric, to redistribution with a buffer dielectric, raises the complexity and therefore the cost of the component. This may require some trade-offs.

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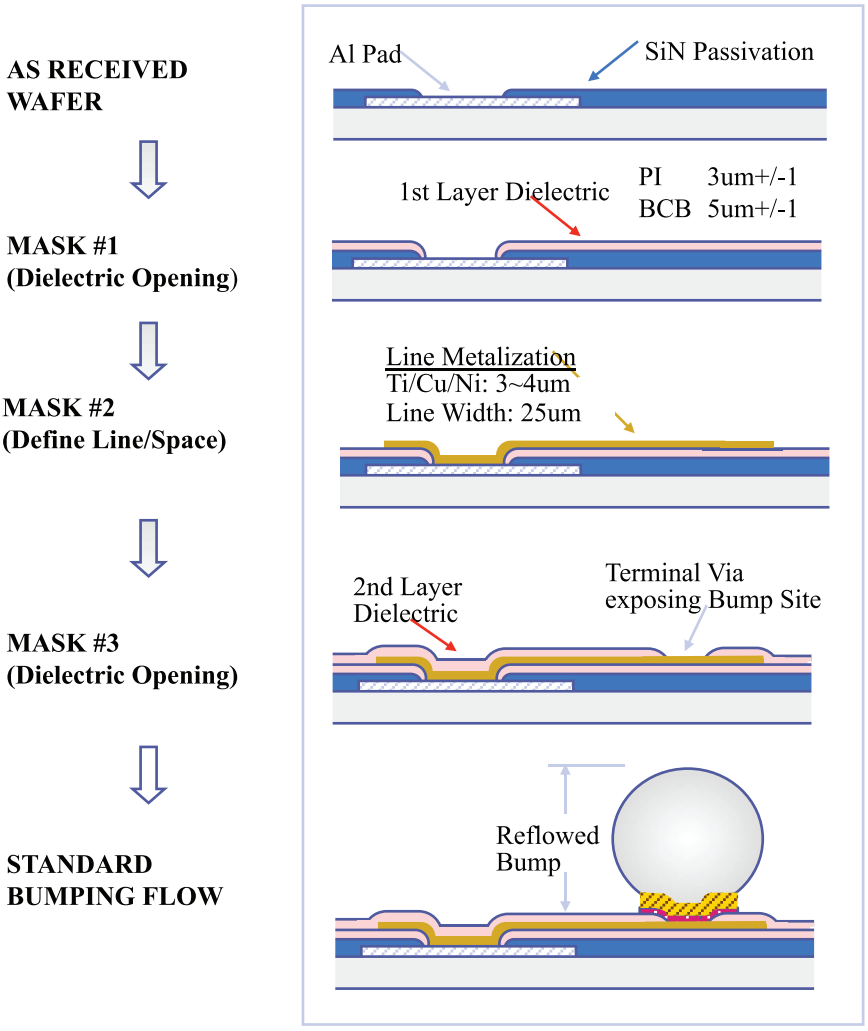

Figure 1. Wafer redistribution process flow.

Solder bumps do not only bond to the printed circuit board, but they can also be used to bond one die to another. The bonding techniques fall into three categories: thermo-compression, reflow, and direct chip attach. Thermocompression uses temperature and force and some form of gap control. With reflow, one can use temperature and gap control, or temperature and the introduction of a flux. For direct chip attach, one uses low force. The blue boxes indicate the types of solders used in the various processes. Thermo-compression works well with gold, indium and copper bumps and several alloys, while reflow can be used with lead-tin materials as well. For direct chip attach, there is no intermediate layer. The build-up of materials on the bond pads make direct contact to each other.

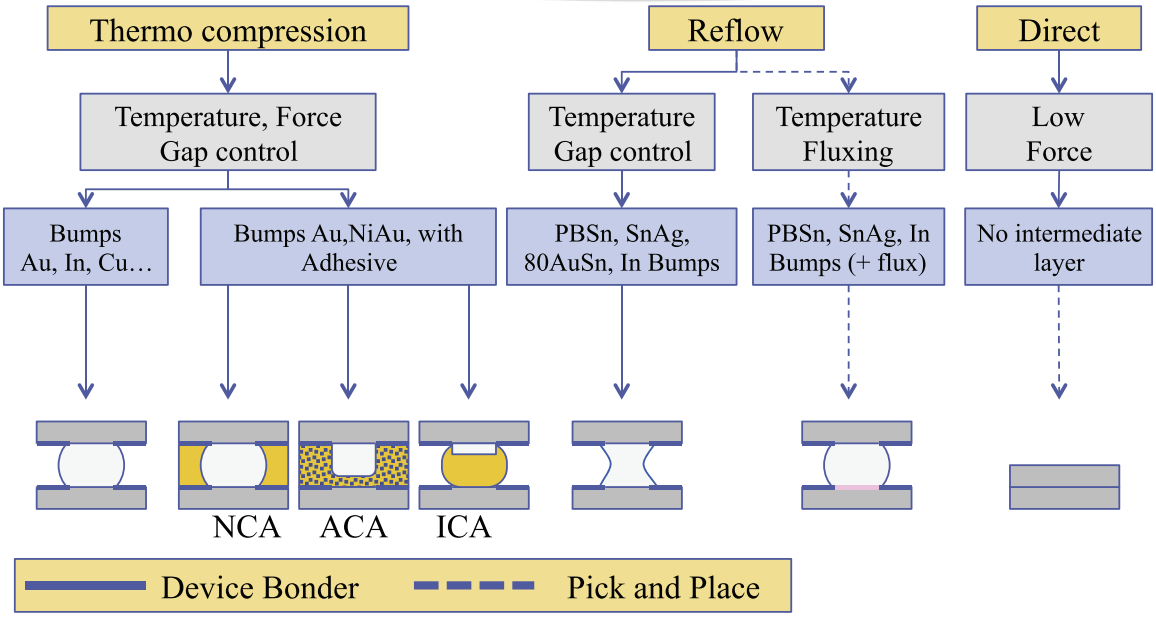

Figure 2. Common die bonding techniques. (NCA: Non-conducting Adhesive; ACA: Anisotropically Conducting Adhesive; ICA: Isotropically Conducting Adhesive)

Redistribution layer techniques work best at the wafer level. This requires an equipment set and process flow that can handle full wafers. The fab-like environment may not need the same level of cleanliness as a front-end fab, but it still requires wafer-level processing techniques. This diagram shows the basic process flow with the interface between front-end and back-end identified. In this approach, there is no test after saw, so it requires extensive testing beforehand. The back side coat is to provide for marking and to suppress cracking.

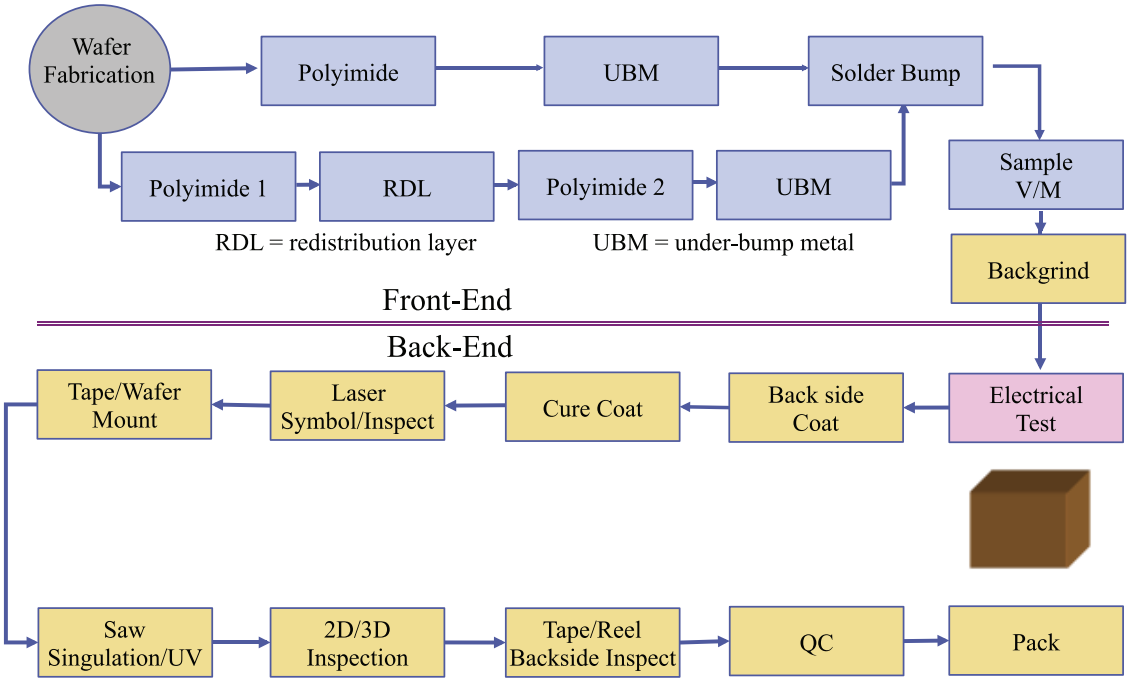

Figure 3. WCSP manufacturing flow

This is an example of a package that uses a bump process. This is the Micro-star BGA package from Texas Instruments. We show a cut-away view to expose the construction of the package traces and solder bumps. The slant in the mold compound allows for easier release from the mold forms. The Micro-star BGA uses a polyimide substrate. Some BGA formats use bizmaleimide triazine.

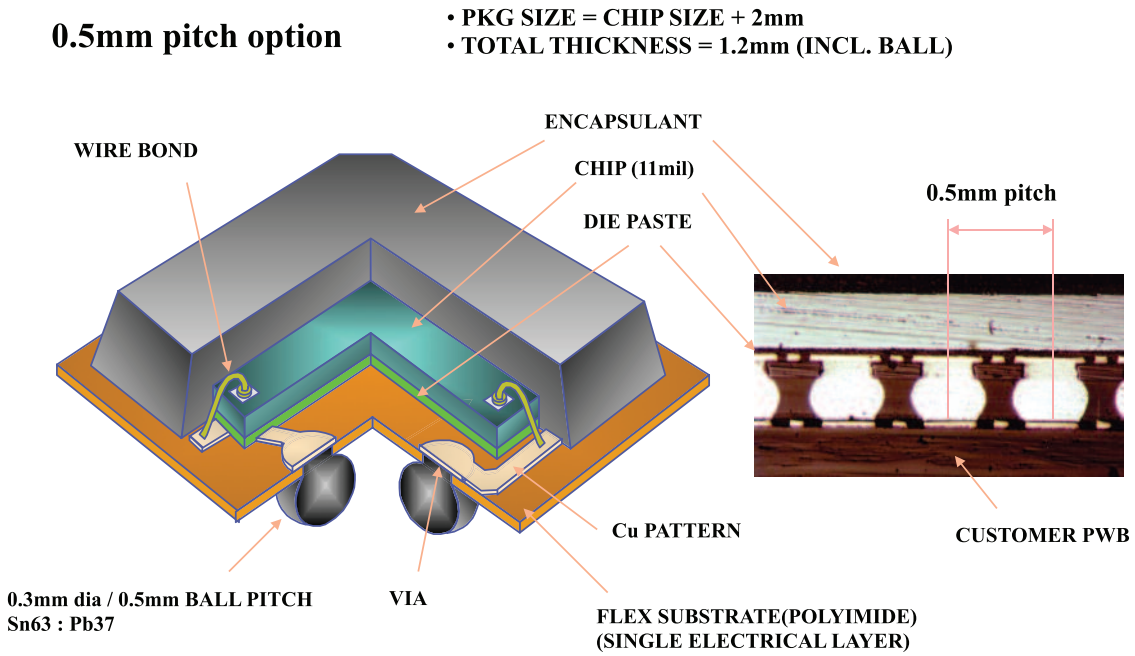

Figure 4. u*BGA package structure (courtesy Texas Instruments).

As we scale to smaller packages, one change that can be beneficial from a space standpoint is going to a lower profile bump. If we look at these cross-sections, notice that a solder ball produces a thicker package while bumps permit a thinner package. The land grid array (LGA) is a packaging technology with a square grid of contacts on the underside of a package. The contacts are to be connected to a grid of contacts on the PCB. Not all rows and columns of the grid need to be used. The contacts can either be made by using an LGA socket, or by using solder paste. LGA packaging is related to ball grid array (BGA) and pin grid array (PGA) packaging. Unlike pin grid arrays, land grid array packages are designed to fit both in a socket or be soldered down using surface mount technology. PGA packages cannot be soldered down using surface mount technology. In contrast with a BGA, land grid array packages in non socketed configurations have no balls and use a flat contact which is soldered directly to the PCB and BGA packages have balls as their contacts in between the IC and the PCBs.

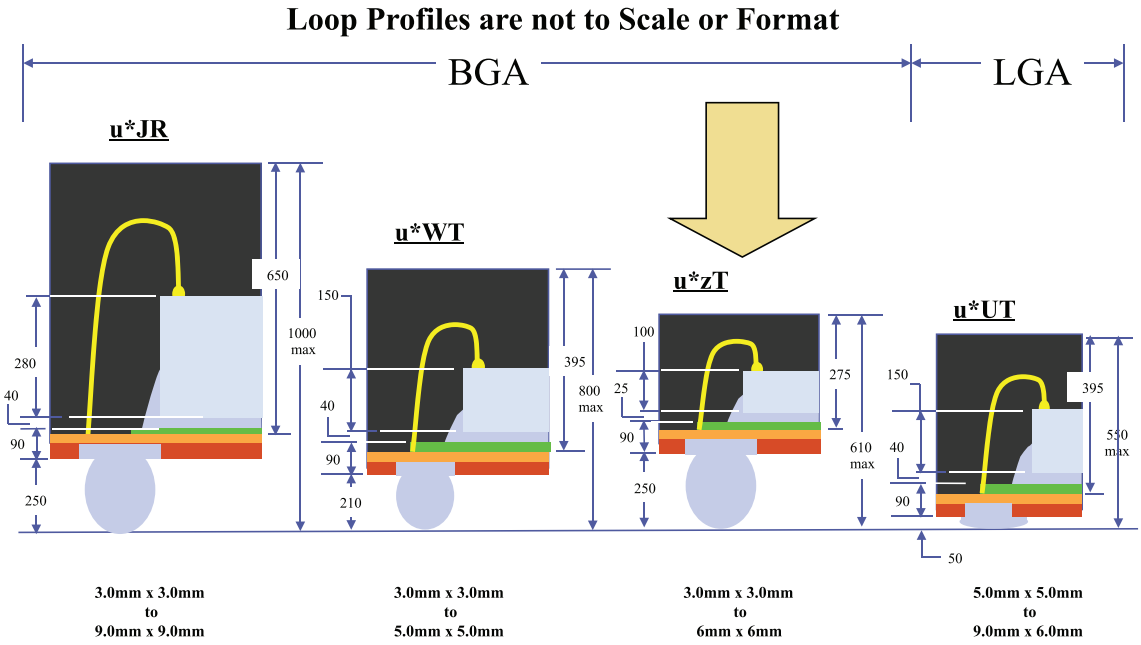

Figure 5. Cross-section comparisons.

To summarize our three-part series, we discussed the basic bumping process. This method is increasingly used when engineers must place a component in a design with limited space. There are two major methods: using solder balls and copper pillars. We also discussed redistribution layer techniques, as these methods can allow retargeting of dice in multiple applications and target smaller footprints as well. Miniaturization is driving the need for even smaller features. This will require finer pitches and lower profiles. This means that engineers will increasingly use technologies like copper pillar bumps to fit in these tight spaces.

Ask the Experts

Q: I seem to recall that the makers of PIND equipment had a tape for gettering loose material when using the PIND system with the top perforated, or with the top open as a cleaning step. Who supplies that tape?

A: There really isn't a "special" brand of tape for this work. Most analysts will simply use a heavy duty double-backed adhesive tape from a manufacturer like 3M. The main issue is examination of the particles. Double-backed tape will outgas when placed in the SEM, so pump down, especially in a Field Emission SEM, where one requires lower vacuum levels. For specific recommendations though, one might contact Spectral Dynamics (http://www.spectraldynamics.com). They sell acoustical tape circles that might work well for this applications.

Technical Tidbit

RESURF Technology

RESURF (also spelled without capital letters as resurf) stands for reduced surface field. This is a concept that takes advantage of the behavior of the depletion region in a p/n junction when one of the materials is confined. The following two figures show the principle behind RESURF. The basic device structure is shown here. It consists of a high voltage diode on a lightly doped p- substrate with a slightly higher-doped epitaxial n- layer on it, which is laterally bounded by a p+ isolation diffusion, shown on the left. The diode therefore consists of two parts: a lateral diode with a vertical n-/p+ boundary and possible lateral breakdown, and a vertical diode with a horizontal n-/p- boundary and possible vertical breakdown. For a thick epitaxial layer (~50µm) the breakdown voltage is ~500V and the maximum field is at the surface at the n-/p+ junction. The light magenta color denotes the depletion region in both images. Notice that the lateral electrical field EL is high near the n-/p+ junction (left image).

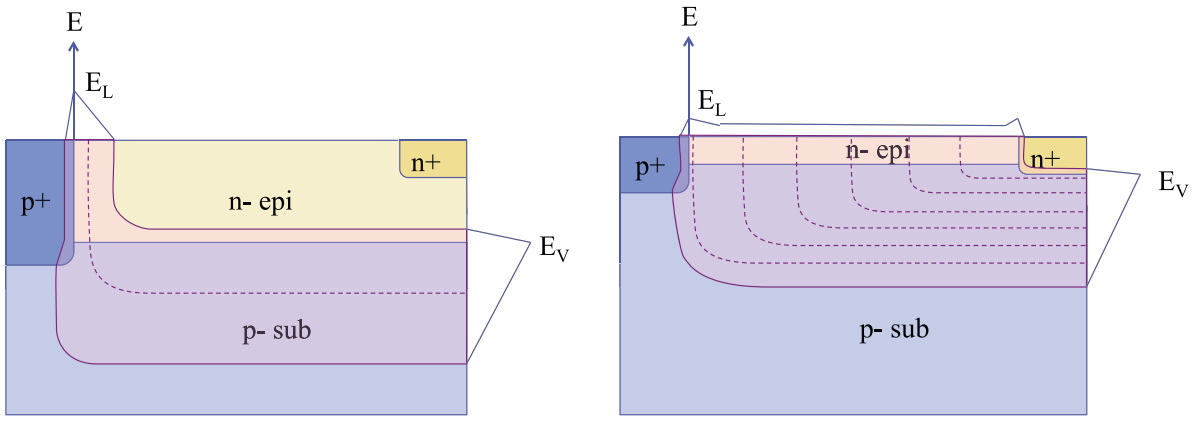

Figure 1. Cross-sectional view showing the concept behind reduced surface field technology. No RESURF effect (left image) and RESURF effect (right image).

For a much thinner epitaxial layer (~15µm) the depletion layer of the vertical n-/p- junction influences the lateral depletion layer, and reducing the surface field (right image). Since the depletion region consumes the entire n- epi region, the electrical field behavior is much different. This is a two-dimensional effect. At a higher voltage (~1200V) the field at the surface has 2 peaks, one originating from the n-/p+ junction and another just below the surface at the curvature of the n+/n- junction, with a moderate field in between. Notice that the lateral electrical E sub L is much smaller near the n-/p+ junction. This not only supports higher breakdown voltages in the structure, but reduces hot carrier damage in the oxide near the n-/p+ junction. If the lateral distance is sufficient, breakdown only occurs vertically in the semiconductor body under the n+ region. Many power semiconductor manufacturers use this technique to create higher performance devices and improve the reliability as well. However, there are some negative effects, like the emergence of the Kirk effect at the n-/n+ junction. RESURF also impacts RDS(ON), but this can in many instances be optimized by adjusting the layout, technology dimensions, and the doping levels. RESURF techniques can be used for discrete transistors, like power npn or pnp transistors, vertical DMOS (VDMOS) devices and lateral DMOS (LDMOS) devices.

Spotlight: Advanced Failure And Yield Analysis

OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Your industry needs competent analysts to help solve these problems. ***Advanced Failure and Yield Analysis*** is a two-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a ***Do It Right the First Time*** approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

Participants learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. **The Process of Failure and Yield Analysis.**Participants learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.
2. **The Tools and Techniques.** Participants learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools, light emission, electron beam tools, optical beam tools, decapping and sample preparation, and surface science tools.
3. **Case Histories.** Participants identify how to use their knowledge through the case histories. They learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.
2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.
3. The seminar will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.
4. The seminar offers a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic technology features on semiconductor devices.
6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

One unique feature of this workshop is the video segments used to help train the students. Failure and Yield Analysis is a visual discipline. The ability to identify nuances and subtleties in images is critical to locating and understanding the defect. Many tools output video images that must be interpreted by analysts. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

1. Introduction
2. Failure Analysis Principles/Procedures
    a. Philosophy of Failure Analysis
    b. Flowcharts
3. Gathering Information
4. Package Level Testing
    a. Optical Microscopy
    b. Acoustic Microscopy
    c. X-Ray Radiography
    d. Hermetic Seal Testing
    e. Residual Gas Analysis
5. Electrical Testing
    a. Basics of Circuit Operation
    b. Curve Tracer/Parameter Analyzer Operation
    c. Quiescent Power Supply Current
    d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
    e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
    f. Automatic Test Equipment
    g. Basics of Digital Circuit Troubleshooting
    h. Basics of Analog Circuit Troubleshooting
6. Decapsulation/Backside Sample Preparation
    a. Mechanical Delidding Techniques
    b. Chemical Delidding Techniques
    c. Backside Sample Preparation Techniques

7. Die Inspection
    a. Optical Microscopy
    b. Scanning Electron Microscopy
8. Photon Emission Microscopy
    a. Mechanisms for Photon Emission
    b. Instrumentation
    c. Frontside
    d. Backside
    e. Interpretation
9. Electron Beam Tools
    a. Voltage Contrast
        i. Passive Voltage Contrast
        ii. Static Voltage Contrast
        iii. Capacitive Coupled Voltage Contrast
        iv. Introduction to Electron Beam Probing
    b. Electron Beam Induced Current
    c. Resistive Contrast Imaging
    d. Charge-Induced Voltage Alteration
10. Optical Beam Tools
    a. Optical Beam Induced Current
    b. Light-Induced Voltage Alteration
    c. Thermally-Induced Voltage Alteration
    d. Seebeck Effect Imaging
    e. Electro-optical Probing
11. Thermal Detection Techniques
    a. Infrared Thermal Imaging
    b. Liquid Crystal Hot Spot Detection
    c. Fluorescent Microthermal Imaging
12. Chemical Unlayering
    a. Wet Chemical Etching
    b. Reactive Ion Etching
    c. Parallel Polishing
13. Analytical Techniques
    a. TEM
    b. SIMS
    c. Auger
    d. ESCA/XPS

14. Focused Ion Beam Technology
    a. Physics of Operation
    b. Instrumentation
    c. Examples
    d. Gas-Assisted Etching
    e. Insulator Deposition
    f. Electrical Circuit Effects
15. Case Histories

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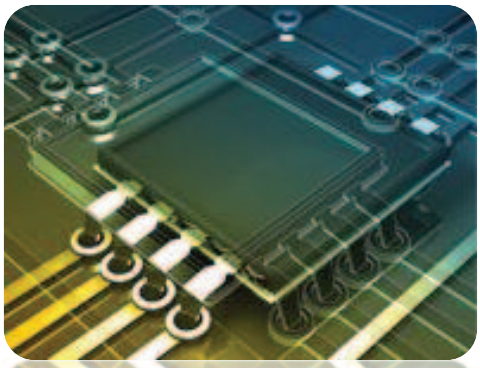

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Upcoming Courses

(Click on each item for details)

Failure and Yield Analysis
June 18 – 20, 2014 (Wed – Fri)
Penang, Malaysia

EOS, ESD and How to Differentiate
June 23 – 24, 2014 (Mon – Tue)
Singapore

Semiconductor Reliability
September 3 – 5, 2014 (Wed – Fri)
San Jose, California

Failure and Yield Analysis
September 8 – 11, 2014 (Mon – Thur)
San Jose, California