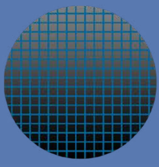
ISSUE #179
June 2024



SEMITRACKS, INC.

INFOTRACKS

YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Transfer Molding

By Christopher Henderson

In this month's Feature Article, we will begin a new series on Transfer Molding. Transfer Molding is one of the more common steps in semiconductor packaging, and provides protection for the sensitive semiconductor components and packaging interconnect.

Before we get into the subject of transfer molding, let's first take a minute to contrast transfer molding with injection molding, the other common molding technique. We show a diagram of injection molding on the left, and a diagram of transfer molding on the right. Transfer molding is a manufacturing process in which a casting material is forced into a mold. Transfer molding is different from compression, or injection, molding in that the mold is enclosed rather than open to the fill plunger, resulting in higher dimensional tolerances and less environmental impact. Compared to injection molding, transfer molding uses higher pressures to uniformly fill the mold cavity. Unlike injection molding, the transfer mold casting material may start the process as a solid. This can reduce equipment costs and time dependency. However, the transfer process may have a slower fill rate than an equivalent injection molding process. For the semiconductor industry, the advantages of transfer molding outweigh the disadvantages, so it is the most common technique used.

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- Semiconductor Reliability and Product Qualification

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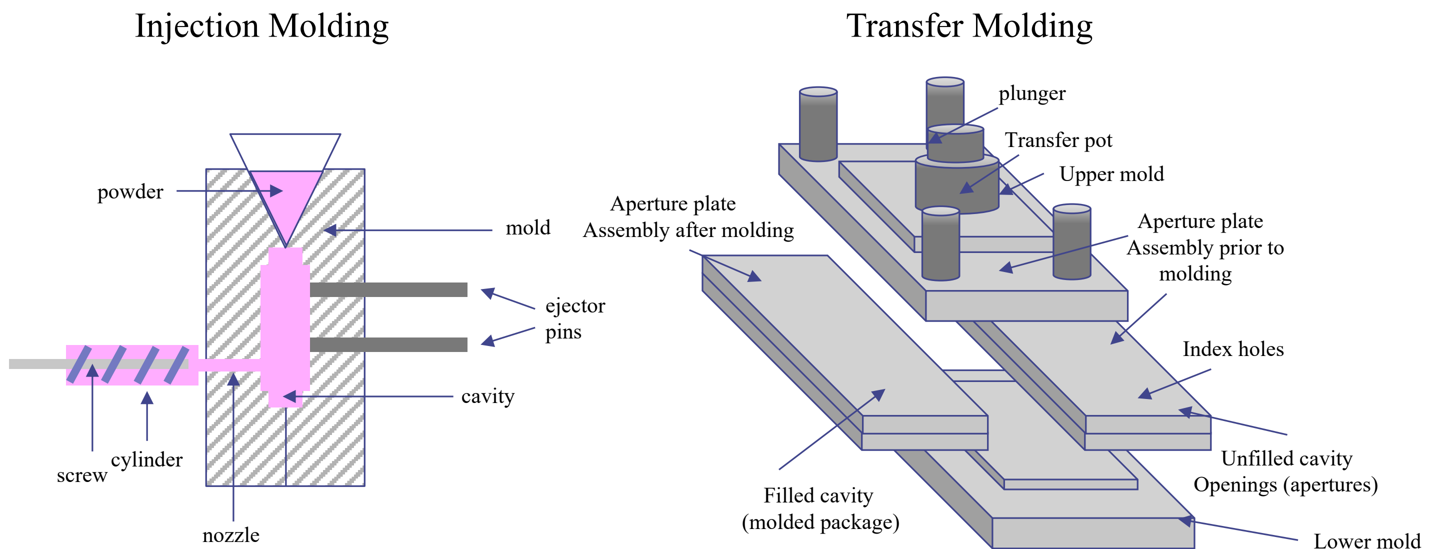


Figure 1- Comparison between Injection Molding and Transfer Molding

Molding is the process of encapsulating the device in hard plastic material. Transfer molding is the most widely used molding process in the semiconductor industry because of its capability to mold small parts with complex features. In this process, the molding compound is first preheated prior to its loading into the molding chamber. After pre-heating, the mold compound is forced by a hydraulic plunger, or ram, into the pot where it reaches the melting temperature and becomes fluid. The plunger continues to force the fluid mold compound into the runners of the mold chase. These runners serve as canals where the fluid mold compound travels until it reaches the mold cavities, which contain the leadframes or BGA substrates for encapsulation. In conventional equipment, cavities that are nearest the runner gates get filled up first. The first cavity experiences the highest filling velocity. The filling velocity decreases as the first cavity is filled. Subsequent cavities are filled with increasing velocities until the last cavity, which has the second highest filling velocity. As such, the first and last cavities are most prone to wire sweeping and die paddle shift. We show a diagram of the major steps in the image in Figure 2.

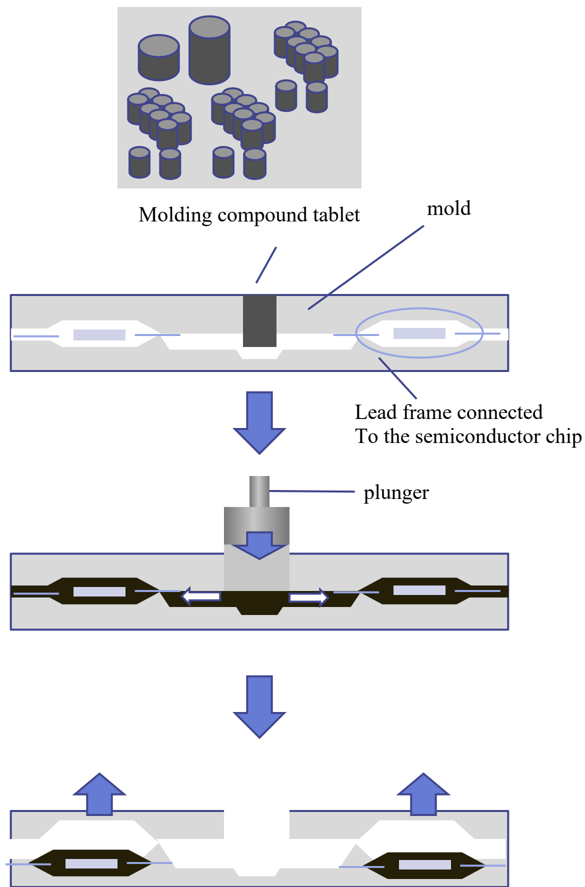
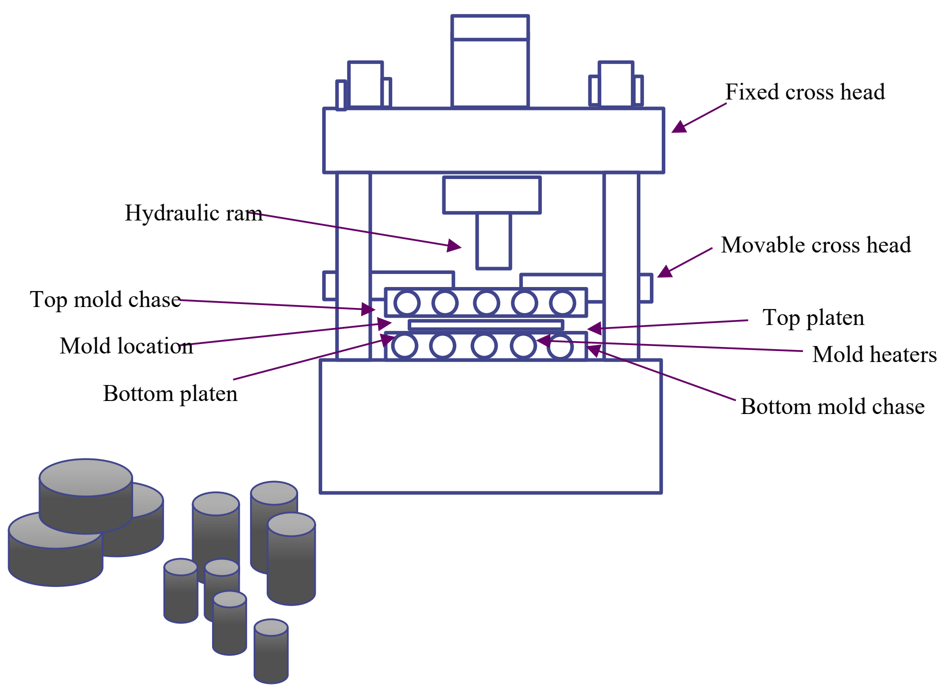
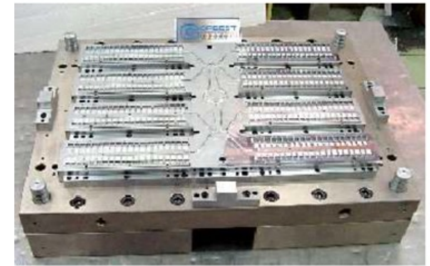


Figure 2- Major steps involved in the transfer molding process (image courtesy Hitachi Chemical)

Now let's examine the molding process more closely. The positioning and movement of the molding plates are controlled by a pressing mechanism, shown at the upper left in Figure 3. This machinery holds both the top platen and the bottom platen. The two platens together are sometimes referred to as mold cavity plates. We show an example of these at the upper right in Figure 3. The bottom platen is held in a fixed position by the bottom mold chase, and the top platen is pressed to the bottom platen by the top mold chase during the mold injection process. Both mold chases contain heaters that heat the mold compound to its melting point, once the platens are pressed together. A hydraulic ram presses down on the liquid mold compound pellets, forcing the mold compound through runner gates and into the mold cavity. The runner gates are designed specifically for the type of package to be molded. We show two examples at the center and lower right in Figure 3.





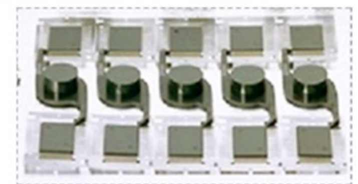
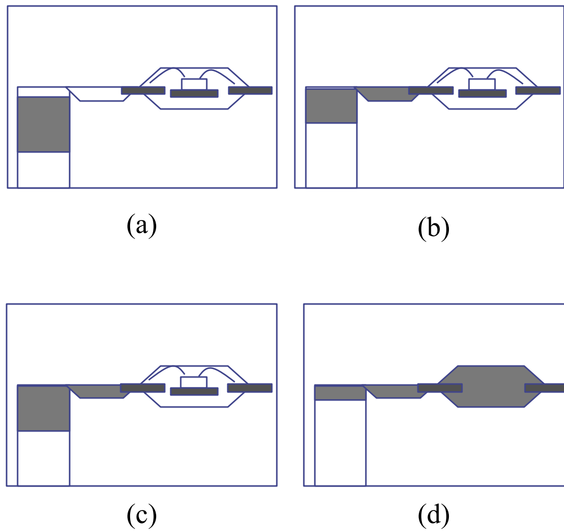
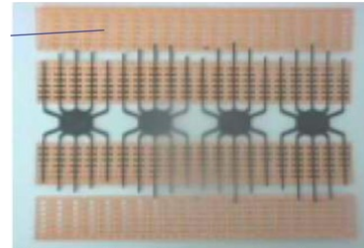


Figure 3- Molding Process

The set of images in Figure 4 show the injection molding process in more detail. The hydraulic ram presses the liquid mold compound through a series of channels known as runner gates. The mold compound enters at the gate, and the displaced air exits from vents at far side of each cavity. On the right, we show examples of different stages in the mold injection process. In the top image, one can see the mold compound pushing through the runner gates and into the package cavities. At this point, the mold compound has not reached many of the cavities in the upper group. In the middle image, the mold compound has reached through most of the cavities in the upper group. The image at the bottom shows the progress of the mold compound through the runner gates and into the cavities. The cavities on the left are closest to the hydraulic ram, while the cavities on the right are farthest from the hydraulic ram.





Mold compound enters at gate, air exits from vent

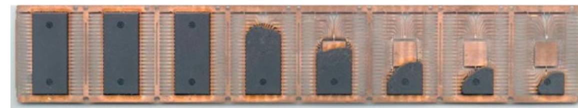
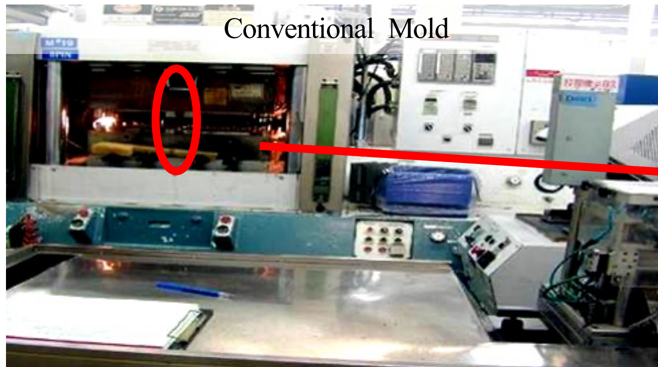
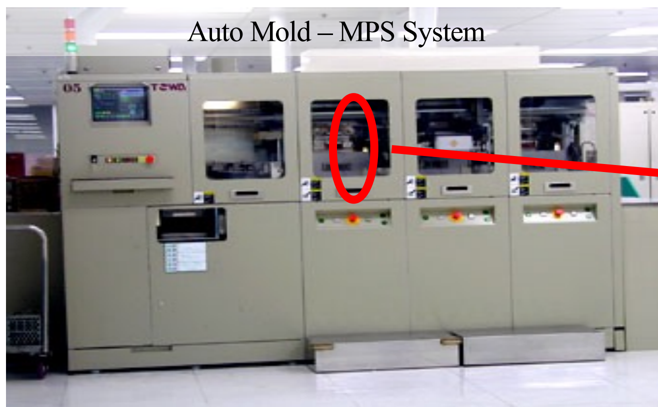


Figure 4- A typical transfer molding process

There are two types of mold injection systems commonly used in the semiconductor industry: conventional systems, and auto-molding systems. Conventional molding systems require an operator to move the product from station to station within the tool. We show this type of system, along with the tooling plates, in the upper set of images in Figure 5. Auto-molding systems provide an automated in-line process for mold, trim, form, deflash, and degate. We show this type of system, along with the tooling plates, in the lower set of images in Figure 5. Towa, a Japanese company, is one of the main suppliers of auto-molding systems.



Tooling: Mold Die



Tooling: Mold Die

Figure 5- Conventional Mold Transfer Equipment (top) and Automated Mold Transfer Equipment (bottom)

For a conventional molding process, one would load the leadframe strip into the holder in the mold compound tool. This holder would sit on the lower mold plate, or might be the lower mold plate itself. Next, one would load the mold compound pellets into the pots associated with the distribution system in the tool. Next, one would place the top mold plate over the lower mold plate containing the leadframe strip, seal the system, and set the tool to perform the mold encapsulaton process. The curing process is part of this encapsulation process as well. To avoid contamination from skin flakes and oils, one must wear gloves, like we see in Figure 6.

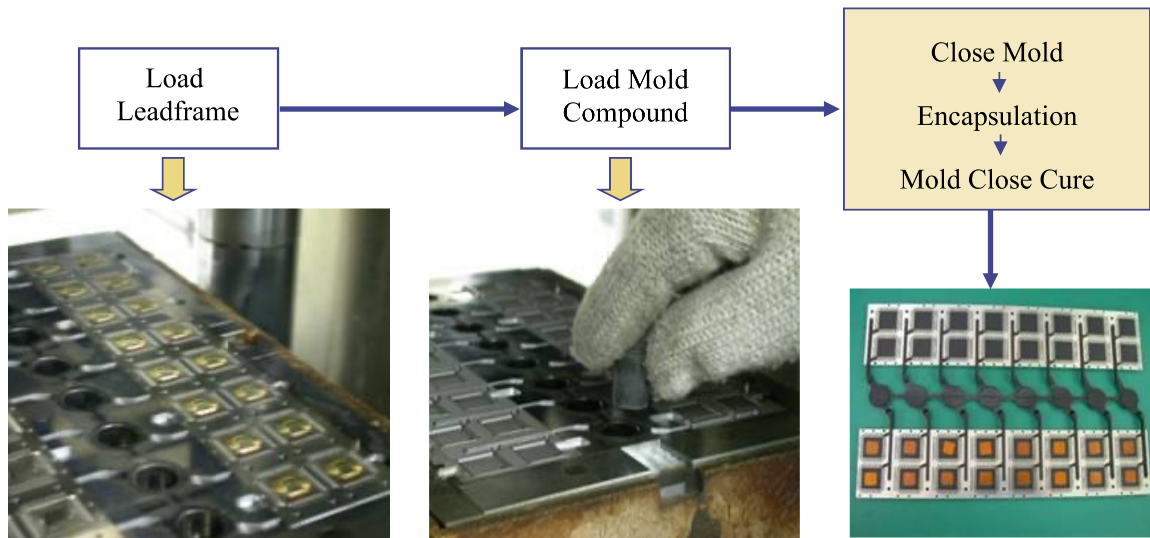


Figure 6- Loading steps for a conventional mold process.

The auto-molding process consists of a series of stations within a larger system. These stations include up to four stations for molding plates, like we show in Figure 7, a loading port, shown as doors on the left side of the system, and a cleaning, deflash and degating module on the right side of the system. These systems feature compatibility with large 100mm X 300mm substrates, also known as workpieces, compatibility with side gate and top gate configurations, and compatibility with release films. These systems contain a central pressure system that contains a "hold frame" structure. They have compact, high-precision press mechanisms, and are capable of molding large numbers of leadframes as they can have a clamping capability of up to 180 tons. These automated systems also have a significantly reduced footprint despite their compatibility with large workpieces.

Figure 7- State-of-the-art Auto Molding System (photography courtesy Towa Corporation)

Figure 8 shows a diagram of the mold plates and chase. The mold compound will travel through the runner gates at varying velocities, depending on the type of mold compound used, the configuration of the runner gates, and the distance between the pot and the mold cavity. The right portion of the slide shows an animated simulation of the mold compound entering a package cavity. The interaction between the mold compound and the package elements, like the wire bonds, is a complex one, so in many cases, this behavior must be modeled to understand if the appropriate mold compound is being used. We need different mold compounds for different packages and runner gate configurations. Furthermore, there is a tradeoff between the viscosity and the cost of the mold compound.

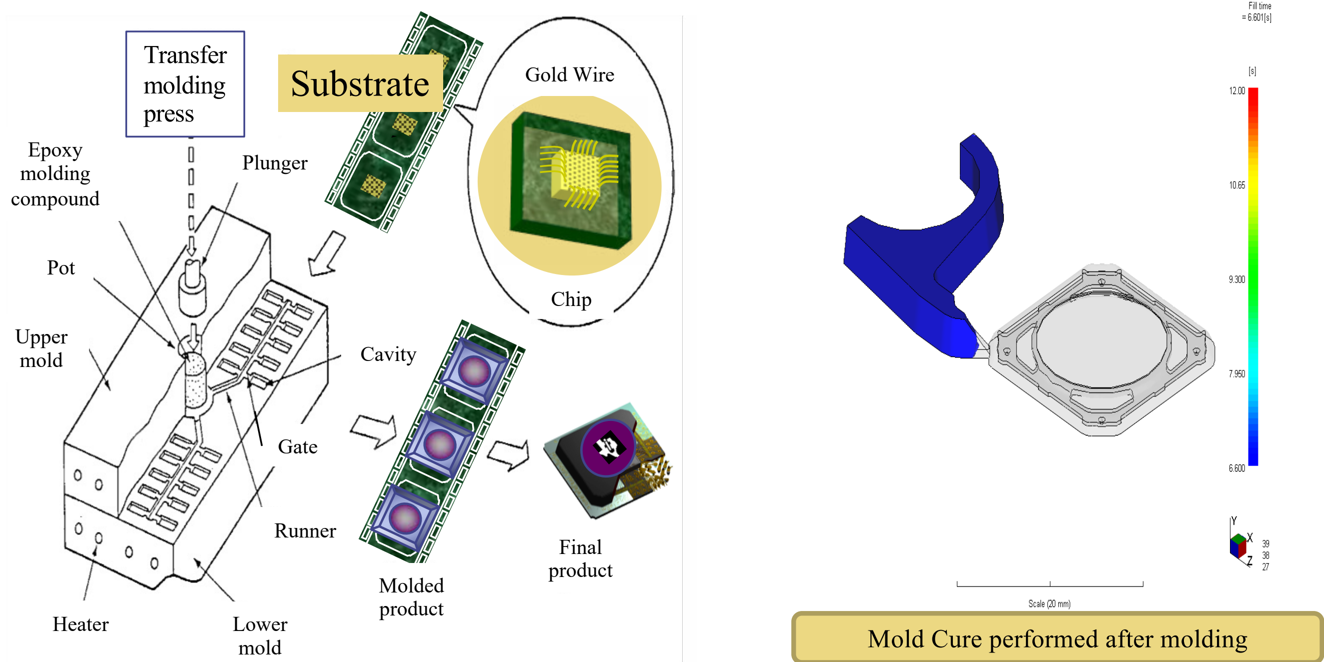


Figure 8- Molding the mold transfer process

In next month's Feature Article, we will discuss the epoxy mold compounds themselves.

Technical Tidbit:Backside Power Delivery

In this month's Technical Tidbit, we will cover the topic of Backside Power Delivery. One of the major challenges involved with the continued scaling of integrated circuits is the area needed to route power to the circuit elements. Historically, engineers have used the frontside metal interconnect system to route power to the circuit blocks. As today's chips grow into the billions of transistors, the area dedicated to frontside power delivery has increased geometrically. Furthermore, the fidelity of the power delivery has decreased due to the need to use smaller and smaller contacts and vias. The series resistance in the interconnect leads to greater voltage dips, or "droop" when circuits demand power. This series resistance also leads to higher Resistance-Capacitance, or RC, delays, which hinders high speed circuitry and impacts chip performance. To address this problem, engineers have begun looking at methods to deliver power from the backside of the silicon. We show a conceptual drawing of this approach from Intel in Figure 1. These connections do not have to share the same area as the signal interconnections. This architecture can provide lower series resistance, since the connections can be larger in diameter.

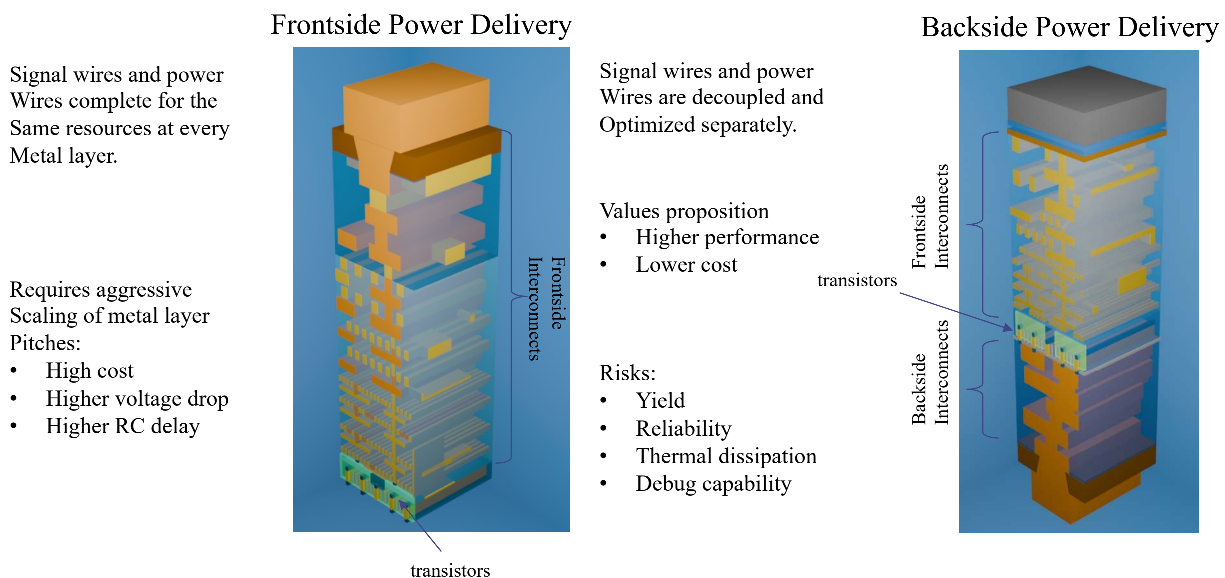
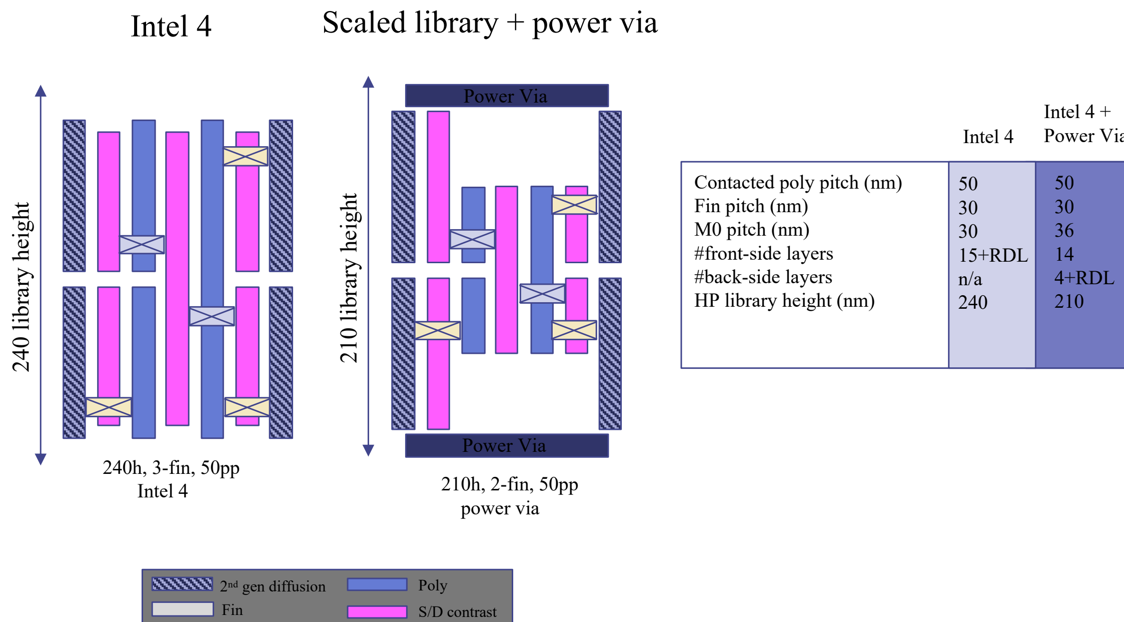


Figure 1- Example of frontside power delivery (left) and backside power delivery (right). Image adapted from Intel.

From a design perspective, the signal interconnect and the power interconnect are decoupled from one another, and can be optimized separately. The advantage of using this approach is that the chip can potentially provide higher performance. Separating these interconnects may also lead to fewer layers of interconnect. The reduction in interconnect layers in turn leads to lower processing costs. Figure 2 shows an example of Intel's standard 4nm process on the left, and Intel's 4nm process with backside power delivery on the right. Intel was able to reduce the number of fins in the standard cells from 3 to 2 in the 4nm backside power delivery process. This in turn led to a reduction in the standard cell height from 240 nm to 210 nm, or a reduction in cell size of about 12.5%.



	Intel 4	Intel 4 + Power Via
Contacted poly pitch (nm)	50	50
Fin pitch (nm)	30	30
M0 pitch (nm)	30	36
#front-side layers	15+RDL	14
#back-side layers	n/a	4+RDL
HP library height (nm)	240	210

Figure 2- Example standard cell in Intel's 4nm process (left) and Intel's 4nm process with backside power delivery (center). We show a comparison of key layers in the two technologies in the table on the right.

There are some significant challenges with this approach, however. The additional backside processing steps introduce the need to align two wafers: one with the transistors and frontside signal network, and another with the backside patterning steps for the power delivery network. This may reduce the yield of the chips. Furthermore, backside power delivery is also an unproven concept, so the reliability of this approach is not well characterized. Depending on the processing approach, the wafers may be thinned considerably, so that the backside interconnect for power delivery can be built up using standard processing steps, like those used for frontside interconnect. This leads to an ultrathin silicon wafer that is not capable of dissipating large quantities of heat. Therefore, thermal dissipation may be a significant issue. This in turn, further impacts reliability. Chips that run hotter have lower reliability. As a rule of thumb, for every 10□C hotter the circuit runs, the lifetime of the chip is cut in half. Finally, the ability to debug these chips is significantly more difficult. Modern debug and failure analysis techniques require that the analyst be able to image signals from the backside of the silicon. If there is a power network on the backside of the silicon, this capability will be severely limited.

Even with these challenges, companies like Intel believe this is a risk worth taking. To that end, Intel has demonstrated test chips with backside power delivery. The test chips they have produced show an improvement in power droop of about 30%, and an improvement in maximum frequency (Fmax) of about 6%. They have also demonstrated better silicon area usage within blocks of standard cells. Given the promising results from these test chips, we should expect to see products with backside power delivery available to customers within the next couple of years.

Ask The Experts

Q: What are the differences between using a Capillary Underfill and a Molded Underfill process on a Flip-Chip Ball Grid Array device?

A: The traditional method for underfill on a Flip-Chip Ball Grid Array (FCBGA) devices is to use Capillary Underfills (CUFs). CUFs have the advantage of fast capillary action, which allows the material to flow in and around the solder bumps on a FCBGA more quickly. Depending on the size of the FCBGA, the time frame for the capillary flow is on the order of 30 to 60 seconds. In contrast, a Molded Underfill (MUF) process takes around 180 seconds. The main challenges of the CUF process include capillary flow time, underfill voids and poor co-planarity of the packaging. Another disadvantage of the CUF is higher moisture absorption. The moisture absorption of CUF and MUF materials can be as much as a factor of three different, with MUF materials exhibiting lower moisture absorption. In addition to lower moisture absorption, MUFs have several other advantages. MUF technology allows higher filler loading of underfill materials. As such, in addition to lower moisture absorption values, MUFs also have lower CTE values and higher Young's Modulus values. Therefore, MUF packaging co-planarity can be improved by reducing the CTE mismatch between the chip and the organic substrate. This can help reduce soldering problems and improve applications involving stacked chips and stacked packages.

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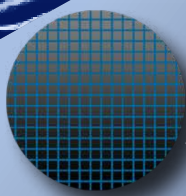

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Course Spotlight: ADVANCED CMOS/FINFET FABRICATION

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" Advanced CMOS/FinFET Fabrication is a 2-day course that offers detailed instruction on the processing used in a modern integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By concentrating on the latest developments in CMOS and FinFET technology, participants will learn why FinFETs are fast becoming the technologies of choice at feature sizes below 20nm. Our instructors work hard to explain semiconductor processing without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants will learn basic, but powerful, aspects about CMOS fabrication and FinFET technology. This skill-building series is divided into four segments:

1. **Front End Of Line (FEOL) Overview.** Participants will study the major developments associated with FEOL processing, including Ion Implantation, Rapid Thermal Annealing (RTA) for implants and silicides, and Pulsed Plasma Doping. They will also study alternate substrate technologies like SOI, as well as High-k/Metal Gates for improved leakage control.

2. **Back End Of Line (BEOL) Overview.** Participants will study the major developments associated with BEOL processing, including copper metallization and Low-k Dielectrics. They will learn about why they're necessary for improved performance.

3. **FinFET Manufacturing Overview.** Participants will learn how semiconductor manufacturers are currently processing FinFET devices and the difficulties associated with three-dimensional structures from a processing and metrology standpoint.

4. **FinFET Reliability.** Participants will also study the failure mechanisms and techniques used for studying the reliability of these devices.

COURSE OBJECTIVES

1. The course will provide participants with an in-depth understanding of Bulk technology, SOI technology and the technical issues.

2. Participants will understand how Hi-K/Metal Gate devices are manufactured.

3. Participants will also understand how FinFET devices are manufactured.

4. The course will provide a look into the latest challenges with copper metallization and Low-k dielectrics.

5. Participants will understand the difficulties associated with non-planar structures and methods to alleviate the problems.

6. Participants will be able to make decisions about how to evaluate FinFET devices and what changes are likely to emerge in the coming years.

7. Participants will briefly learn about IC reliability and the failure modes associated with these devices.

8. Participants will see a comparison between FinFETs and new alternatives (such as Gate All Around (GAA) structures and nanosheets).

COURSE OUTLINE - Lecture Time 16 Hours

1. Advanced CMOS Fabrication – Introduction

2. Front End Of Line (FEOL) Processing
    a. SOI and FD-SOI
    b. Ion Implantation and Rapid Thermal Annealing
    c. Pulsed Plasma Doping
    d. Hi-K/Metal Gates
    e. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology

3. Back End Of Line (BEOL) Processing
    a. Introduction and Performance Issues
    b. Copper
        i. Deposition Methods
        ii. Liners
        iii. Capping Materials
        iv. Damascene Processing Steps
    c. Lo-k Dielectrics
        i. Materials
        ii. Processing Methods
    d. Reliability Issues

4. FinFET Manufacturing Overview
    a. Substrates
        i. Bulk
        ii. SOI
    b. FinFET Types
    c. Process Sequence
    d. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology

5. FinFET Reliability
    a. Defect density issues
    b. Gate Stack
    c. Transistor Reliability (BTI and Hot Carriers)
    d. Heat dissipation issues
    e. Failure analysis challenges

6. Future Directions for FinFETs
    a. Comparison of FinFETs and other Techniques (GAA, Nanosheets) – Are FinFETs a better choice?
    b. Scaling

Upcoming Courses:

Public Course Schedule:

Advanced CMOS/FinFET Fabrication - September 2-3, 2024 (Mon.-Tues.) | Singapore - $1,195 until Mon. Aug. 12

Packaging Failure and Yield Analysis - September 9-10, 2024 (Mon.-Tues.) | Penang, Malaysia - $1,195 until Mon. Aug. 19

Packaging Failure and Yield Analysis - September 23-24, 2024 (Mon.-Tues.) | Manila, Philippines -$1,195 until Mon. Sept. 2

Defect-Based Testing - November 18-19, 2024 (Mon.-Tues.) | Munich, Germany - $1,195 until Mon. Oct. 28

Wafer Fab Processing - November 25-28, 2024 (Mon.-Thurs.) | Munich, Germany -$2,095 until Mon. Nov. 4

Failure and Yield Analysis - December 2-5, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Nov. 11

Semiconductor Reliability and Product Qualification - December 9-12, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Nov. 18

Webinar Schedule:

Semiconductor Reliability and Product Qualification Webinar - August 5-8, 2024 (Mon.-Thurs.) | Online at 8:00 AM-12:00 Noon Pacific Time - $600

Advanced CMOS/FinFET Fabrication Webinar - August 19-22, 2024 (Mon.-Thurs.) | Online at 8:00 AM-12:00 Noon Pacific Time - $600

IC Packaging Technology Webinar - August 26-29, 2024 (Mon.-Thurs.) | Online at 8:00 AM-12:00 Noon Pacific Time - $600

Have an idea for a course? If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please email us at info@semitracks.com

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!