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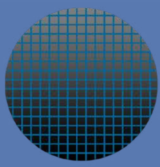

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YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Transfer Molding

By Christopher Henderson

In this month's Feature Article, we continue our series on Transfer Molding. Transfer Molding is one of the more common steps in semiconductor packaging, and provides protection for the sensitive semiconductor components and packaging interconnect. In this article, we will discuss the mold compounds themselves.

Mold compound is the polymer material that covers the die surface, wirebonds, and a portion of the leadframe in a traditional semiconductor package. Mold compound is also used in some packages as a top covering. It is important to note that many newer packages do not use mold compound. We show an example of a package that uses mold compound in Figure 1 on the left, and an example of mold compound materials in Figure 1 on the right, including both the powdered form and the pellet form. Newer equipment will often use small pellets distributed through the mold injection tool to reduce the amount of flow through channels.

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Figure 1- IC Package that uses mold compound (left), and mold compound materials (right).

What makes mold compound an important part of many semiconductor package types? There are a number of reasons that it is important. First, it provides the component with a mechanical form and structural integrity. Second, it protects the interconnections to the outside of the chip, which includes the wirebonds, the leadframe, and in the case of a flip chip device, the solder bumps. Third, it protects the die surface. Fourth, it protects the die and interconnections from corrosion due to moisture and chemicals. Fifth, it provides a platform for the next level of interconnect for a number of different package types. Plastic packaging can perform all of these functions, to some extent, without compromising the electrical function of the IC, its reliability, and its affordability. In fact, almost 90% of all IC package formats use plastic packaging to some extent. It is important to note though, that the mold compound needs to be formulated for the type of package and the molding system in which it will be used.

Let’s discuss the properties of the mold compounds used in transfer molding. There are a number of properties that are useful for mold compound materials. First is low viscosity during the mold fill. This allows for faster processing during the mold injection process, and less movement of the bond wires during the injection process. Second is a quick mold gel cure time. This also allows for faster processing times. Third would be excellent adhesion to the leadframe. This helps to reduce delaminations in the package, and moisture accumulation at the interface between the mold compound and the leadframe. Fourth is low ionic contamination levels. Low ionic contamination levels reduce the possibility of corrosion. Fifth is low moisture absorption. Low moisture absorption reduces the possibility of both corrosion and the popcorn mechanism. We will discuss the popcorn mechanism later in this series of articles. Sixth is a long shelf life. A long shelf life means that the mold compound can be purchased in larger quantities ahead of time, if

needed. Seventh is toughness, or resistance to fracturing at both low and right temperatures. Eighth is a low coefficient of thermal expansion and a low Young's Modulus. A low coefficient of thermal expansion reduces stress at the mold compound semiconductor die interface. A low Young's modulus also reduces stress at the same interface. Ninth is high thermal conductivity. High thermal conductivity aids in removing heat from the semiconductor die. Tenth is high flame retardancy. This helps reduce the chance of an electronic system catching fire should a thermal overload condition develop. Eleventh is well controlled electrical properties, including both resistivity and dielectric strength. Finally, and often most important, is cost. Low cost is always desired, especially in high volume manufacturing applications.

Mold compounds are a complex mixture of materials. The main ingredient is the epoxy resin. This is typically a binder chemical that also provides mechanical strength to the package after curing. The next ingredient is the hardener. This is a chemical that reacts with the resin and cross-links with it to help create a hard, solid material after curing. The next ingredient is the catalyst. This helps to lower the activation energy of the reaction between the resin and the hardener, and accelerate it. The next ingredient is the filler material. These filler particles are designed primarily to help tailor the coefficient of thermal expansion of the mold compound, and secondarily, to help tailor the thermal diffusion properties of the mold compound. The next ingredient is the mold-release agent. This helps the package release from the mold plates more easily. The next ingredient is the adhesion promoter. This helps the mold compound adhere to the die and the leadframe. The next ingredient is the flame-retardant agent. This helps to prevent the mold compound from catching fire from an electrical short or thermal overstress. The next ingredient is carbon black to provide the dark color to the mold compound and prevent light from reaching the semiconductor die. The final ingredient is a gettering agent. This is typically added to trap chlorine ions to prevent corrosion.

For certain applications, mold compounds need to be able to withstand high voltages and high temperatures. In order for a mold compound to have good electrical properties, four things must occur. First, the mold compound should have a low dielectric permittivity. This is needed to match to the air outside of the package and to the passivation layer inside the package. Second, the mold compound should have low electrical conductivity. This is needed to minimize leakage, and to minimize ionic transport, so that galvanic corrosion is minimized. Third, the mold compound should have a high dielectric breakdown strength. This is needed to withstand high voltages over an extended period of time, and to withstand transient voltage events. Finally, the surface should be free from surface defects, so there are no local regions where the electric field is high. In order for a mold compound to have good thermo-mechanical properties, four things must occur, as well. First, the mold compound should exhibit minimal degradation over time. This helps to improve the reliability of the component. Second, the coefficient of thermal expansion should match the surrounding materials as closely as possible. This helps to minimize stress at the interfaces between the mold compound and the semiconductor die, wirebonds, and leadframe. Third, there should be no cracking during the operation of the component, either from thermal cycling or vibration. Finally, the mold compound should exhibit a high glass transition temperature. This is needed because the physical properties of the mold compound change, typically for the worse, when the glass transition temperature is exceeded. Table 1 shows an example of three different applications, and three possible mold compound candidates for these applications.

Application	Mold compounds	Tg
BiCMOS Process	Sumitomo G720	165C
GaN Process	Shin-Etsu KMC 2285C	154C
High Voltage Process	Hitachi 8420HF10GK	130C

Table 1- Glass transition temperatures for three different mold compounds, representing use in three different applications.

The physical properties of the mold compound are determined by two major factors: composition and processing or manufacturing. Under composition, the main sub-factors include the type of resin; the ionic content of the material; the physical properties of the filler materials; the size, content and distribution of the filler particles; and the filler-resin interface. In Figure 2, we show a cross-section image of Shin Etsu's KMC2285C mold compound. The spherical particles are filler particles present in the mold compound. Under processing and manufacturing, the presence of voids or defects plays the biggest role. One important item to note about the physical properties of the mold compound is that they vary as a function of temperature, pressure, time, voltage, mechanical stress, moisture, and other factors.

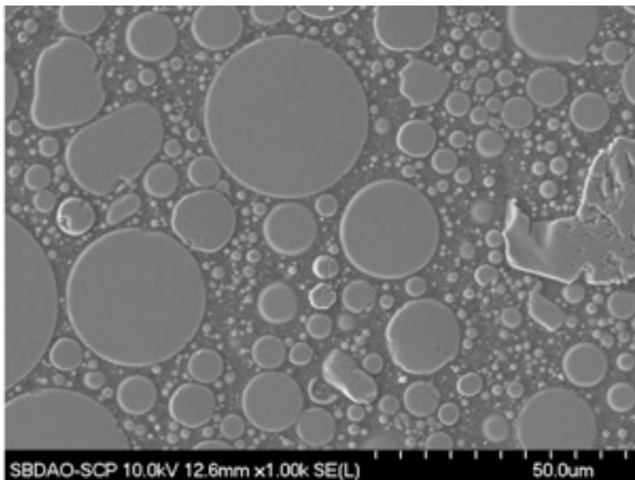

Figure 2- Scanning Electron Microscope (SEM) image of Shin Etsu's KMC2285C mold compound.

In next month's Feature Article, we will discuss the mold compound constituents in more detail.

Technical Tidbit:Standard Cell Library Evolution

In this month's Technical Tidbit, we will cover the topic of standard cell libraries, and their evolution over the past 30 to 40 years. Standard cell libraries were introduced in the 1980s to help integrated circuit (IC) designers become more productive. They are now used in virtually every chip technology. Initially, standard cell libraries did not have many limitations in terms of the layouts of the cells themselves. Figure 1 shows an example of a D Flip-Flop standard cell from approximately the 1990 timeframe.

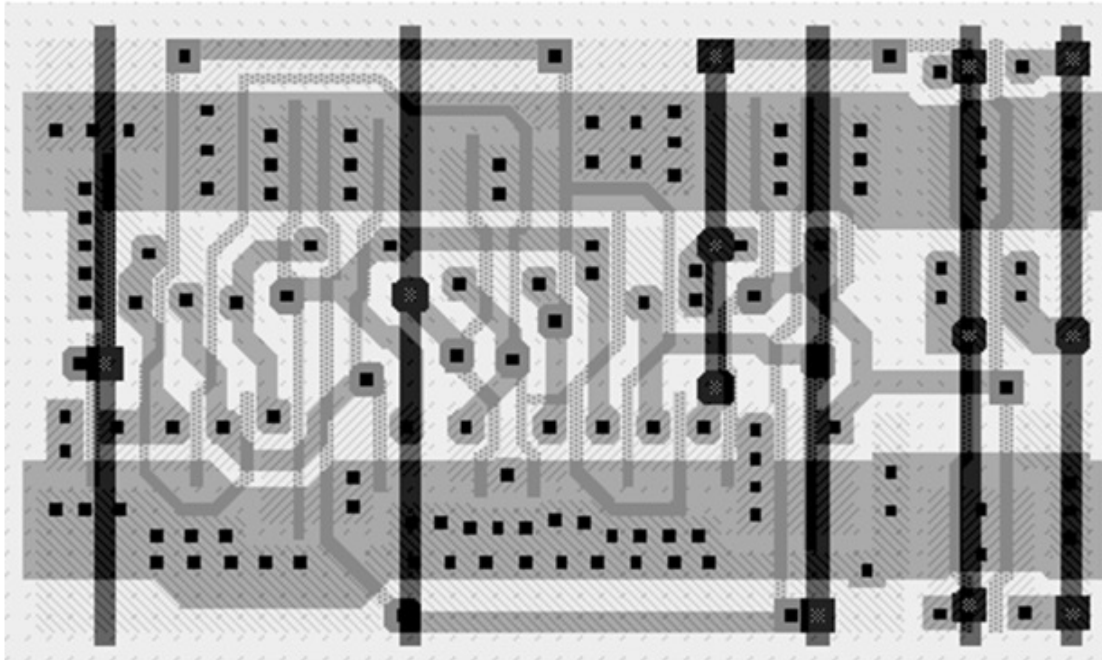

Figure 1- D Flip Flop standard cell, circa 1990.

The standard cell in Figure 1 illustrates some common principles used early on in standard cell design:

- Layouts were often done using 45° angles. This would save 10%–20% in area compared to a cell that uses only Manhattan or 90° geometry.
- Connectors were placed at the top and bottom of the cell in metal-2 on a routing grid equal to the vertical track spacing. This is a double-entry cell intended for a two-level metal process. Briefly, a track is a channel (horizontal in Figure 1) for a particular layer of interconnect. In Figure 1, the track would be associated with metal-2. A standard cell designed for a three-level metal process would sometimes have connectors placed in the center of the cell.
- Engineers might vary the transistor sizes to optimize the area and performance but maintain a fixed ratio between the n- and p-channel transistors to balance rise times and fall times.

- In Figure 1, the cell height is 64 λ (lambda = the minimum feature size in thechip design) with a horizontal (metal-1) track spacing of 8 λ . Almost universally, all cells in the library would be the same height. This is close to the minimum height that can accommodate the most complex cells in a library.
- Designers would place the power rails at the top and bottom of the standard cell, maintaining a certain width inside the cell, and seamlessly connect with the power rails in adjacent cells.
- Designers would place the well contacts (substrate connections) inside the cell at regular intervals. Additional well contacts might be placed in spacers between cells.
- In Figure 1, we show both wells. Some libraries minimize the well or moat area to reduce leakage and parasitic capacitance.
- In this time period, most commercial standard cells used metal-1 for the power rails, metal-1 for internal connections, and would avoid using metal-2 where possible except for cell connectors.

Due to the limited constraints on standard cell designs, standard cell libraries increased to include thousands of standard cells by the early 2000s. This increase happened not because of new logical functions, but rather due to flexibility that designers requested. These requests included cells with different drive strengths, different threshold voltages, different orientations, and different connection points.

However, by the 2010s, this proliferation of standard cells began to reverse itself. As technology feature sizes continued to decrease, and as designers continued to produce evermore complex designs, the layouts of standard cells became more limited. Today, lithography precludes the use of 45° angles. In state-of-the-art ICs, lithography also precludes the use of any type of bend or "T" in the interconnect materials (polysilicon and metal). Put another way, all interconnect needs to be "one-dimensional." Also, process margins limit the spacing and use of particular features, like difference-sized contacts, different metal widths, etc. Furthermore, the standard cell library architecture and its variety will be limited by the cell heights. In general, the cell height limits the available cells. The horizontal metal layers can only support a limited number of tracks, and the power rails use one track, further limiting the flexibility. In a state-of-the-art design, designers need 1 to 2 tracks for gate contacts, and 1 to 2 tracks for the output nodes. A 7-track layout has 6 internal tracks, and a 6-track layout has 5 internal tracks. Given the number and variation of logic gates designers prefer to have available for their designs, we would have about 250 cells per threshold voltage when we account for drive differences. In general, as we shrink the technology, the number of standard cells we can implement has been shrinking as well. At the 7nm node, which corresponds to approximately 20nm design feature sizes, or λ, the number of cells is probably no more than 100 to 200 at most.

One might ask why there is a diminishing number of standard cells as we decrease the feature sizes. One might think it would be the opposite. However, processing limitations severely impact the allowed geometries. Horizontal poly routing would connect the input pins in older libraries, allowing for more options, and high drive gates would typically require multiple finger transistors, but this is difficult to achieve with limited tracks. If we use the AND-OR-Invert (AOI) gate as an example with one-dimensional metal and a 6-track library, there are limited options without significantly increasing the gate area. One can see from the layout images in Figure 2, everything is tightly packed with limited margins, and as such, there are no good options without a dramatic increase in area.

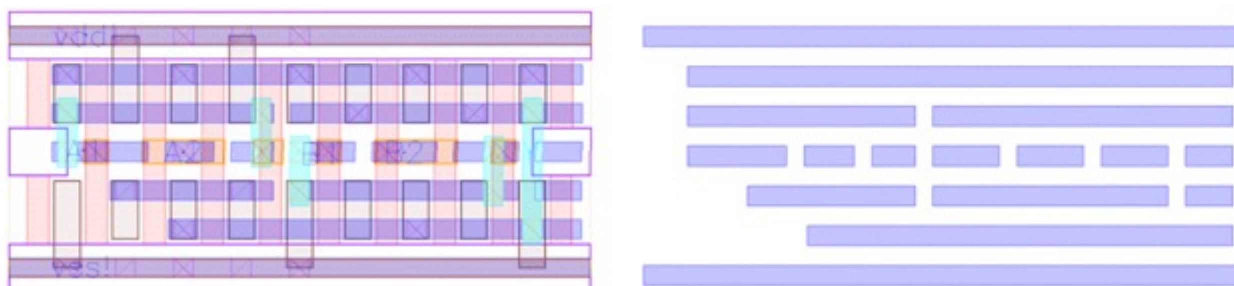

Figure 2- Example of an AOI22 standard cell (left), with one-dimensional metal-1 (shown by itself on the right), implemented in a 6-track library.

In summary, standard cell libraries have become increasingly constrained by lithography, processing, and even reliability issues. As such, the number of standard cells in a library has been decreasing since the 65nm technology node, as seen in Table 1.

Family	3µm	130nm	90nm	65nm	40nm	20nm
Lib size (approx)	<100	2000	5000	10000+	6000	100?

Table 1- Standard cell library size over the last 40 years, from the 3µm feature sizes to 20nm feature sizes.

In the future, we are not likely to see a further reduction in the number and types of standard cells. One might think that Complementary FETs would provide some ability to better utilize the vertical direction for cell variety, but it is also unlikely that we will see a return to a large number of standard cell types, given the continued constraints on manufacturing due to process limitations.

Ask The Experts

Q: What factors would determine whether packaging engineers should select an overmold or a lid for a Ball Grid Array (BGA) device?

A: There may be several factors that packaging engineers use to determine whether an overmold or a lid is appropriate for a BGA device. The primary factor would be power dissipation. High levels of power dissipation might require a metal lid with an attachment to a heat sink. Another factor would be warpage. Molding may induce stress that can create warpage in certain situations with high CTE mold compounds. A (minor) third factor would be hermeticity. If the component is going to be used in an environment where it needs to be hermetically sealed, then a metal lid, in conjunction with a ceramic package, would typically be used.

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Course Spotlight: PACKAGING FAILURE AND YIELD ANALYSIS

OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Our industry needs competent analysts to help solve these problems. ***Packaging Failure and Yield Analysis*** is a 2-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. In this version of the course, we place additional emphasis on package-level Failure Analysis. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a ***Do It Right the First Time*** approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

Participants will learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. **The Process of Failure and Yield Analysis.** Participants will learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.

2. **The Tools and Techniques.** Participants will learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools like x-ray radiography, time domain reflectometry, magnetic force imaging, infrared thermography, decapping and sample preparation.

3. **Case Histories.** Participants will identify how to use their knowledge through the case histories. They will learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

COURSE OBJECTIVES

1. The course will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.

2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.

3. The course will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.

4. The course will offer a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.

5. Participants will be able to identify basic technology features on semiconductor packages.

6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.

7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

COURSE OUTLINE

DAY 1

1. Introduction

2. Failure Analysis Principles/Procedures
    a. Philosophy of Failure Analysis
    b. Flowcharts

3. Gathering Information

4. Package Level Testing
    a. Optical Microscopy
    b. Acoustic Microscopy
    c. X-Ray Radiography
    d. Hermetic Seal Testing
    e. Residual Gas Analysis
    f. Magnetic Current Imaging
    g. Lock-In Thermography

5. Electrical Testing
    a. Basics of Circuit Operation
    b. Curve Tracer/Parameter Analyzer Operation
    c. Quiescent Power Supply Current
    d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
    e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
    f. Automatic Test Equipment
    g. Basics of Digital Circuit Troubleshooting
    h. Basics of Analog Circuit Troubleshooting

DAY 2

6. Decapsulation/Backside Sample Preparation
    a. Mechanical Delidding Techniques
    b. Chemical Delidding Techniques
    c. Backside Sample Preparation Techniques
        i. Warpage Control Techniques
    d. Advanced Disassembly Techniques

7. Package and Die Inspection
    a. Optical Microscopy
    b. Scanning Electron Microscopy

8. Analytical Techniques
    a. Auger
    b. ESCA/XPS

9. Focused Ion Beam Technology
    a. Physics of Operation
    b. Instrumentation
    c. Examples for Packaging FA
    d. Gas-Assisted Etching

10. Case Histories

Upcoming Courses:

Webinar Schedule:

Semiconductor Reliability and Product Qualification Webinar - August 5-8, 2024 (Mon.-Thurs.) | Online at 8:00 AM-12:00 Noon Pacific Time - $600

Advanced CMOS/FinFET Fabrication Webinar - August 19-22, 2024 (Mon.-Thurs.) | Online at 8:00 AM-12:00 Noon Pacific Time - $600

IC Packaging Technology Webinar - August 26-29, 2024 (Mon.-Thurs.) | Online at 8:00 AM-12:00 Noon Pacific Time - $600

Public Course Schedule:

Advanced CMOS/FinFET Fabrication - September 2-3, 2024 (Mon.-Tues.) | Singapore - $1,195 until Mon. Aug. 12

Packaging Failure and Yield Analysis - September 9-10, 2024 (Mon.-Tues.) | Penang, Malaysia - $1,195 until Mon. Aug. 19

Packaging Failure and Yield Analysis - September 23-24, 2024 (Mon.-Tues.) | Manila, Philippines -$1,195 until Mon. Sept. 2

Defect-Based Testing - November 18-19, 2024 (Mon.-Tues.) | Munich, Germany - $1,195 until Mon. Oct. 28

Wafer Fab Processing - November 25-28, 2024 (Mon.-Thurs.) | Munich, Germany -$2,095 until Mon. Nov. 4

Failure and Yield Analysis - December 2-5, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Nov. 11

Semiconductor Reliability and Product Qualification - December 9-12, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Nov. 18

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