Issue 25 July 2011

InfoTracks

Semitracks Monthly Newsletter

New Semitracks Blog!

In order to keep our readers better up-to-date and informed, Semitracks Inc. has launched its new blog!

Read more, Page 3

Capacitance-Voltage Plotting, Part II

By Christopher Henderson

Continued from June's Newsletter

Figure 3 helps to illustrate the MOS capacitance values that occur under different conditions. *The positive charge resides at the metal-oxide interface, while *the negative charge is distributed within the depletion region in the silicon. *One can represent this as two capacitors in series. *The capacitance across the oxide is straightforward to model, as it is simply the dielectric constant of the oxide divided by its thickness. To first order, the capacitance across the silicon is the dielectric constant of the silicon divided by the depletion width. We'll discuss some additional factors on the following slide. According to capacitance behavior,

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{Si}}$$

Therefore the total capacitance is given by

$$C = \frac{C_{ox}}{1 + \frac{C_{ox}}{C_{Si}}}$$

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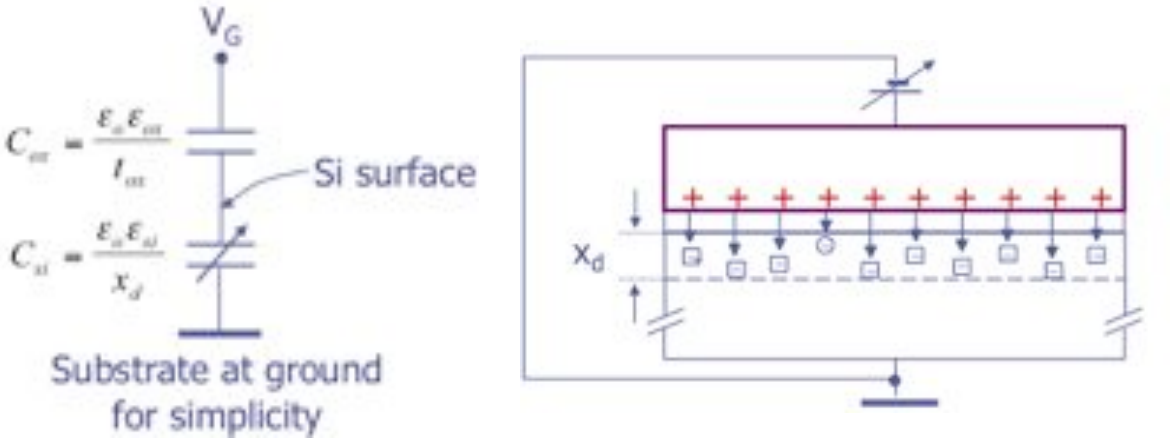


Fig. 3. Components to MOS capacitance

*To calculate the silicon capacitance at flatband, we need a method to approximate the capacitor plates in silicon. The first plate can simply be placed at the silicon surface. The second plate is placed at a depth equal to the Debye length, L sub D, *which is given by

$$L_D = \sqrt{\frac{\varepsilon_o \varepsilon_{Si} kT}{q^2(n+p)}}$$

For p-type silicon, we can ignore n, the number of electrons in the material. *The number of holes is primarily due to the number of acceptors in the material, so we can replace p with N_A. *Therefore, in flatband, the silicon capacitance per unit area is simply the dielectric constant divided by the Debye length. *One way to think about this is the Debye length is the distance over which carriers still feel disturbances.

So, to summarize our analysis of the high-frequency CV plot for an ideal MOS structure, there are three regions of interest: accumulation, depletion, and inversion. *In strong accumulation, the majority carrier concentration increases rapidly at the surface, causing the Debye length to decrease and the capacitance in the silicon to increase. As the structure goes further into accumulation, the capacitance will increase to a maximum value around the capacitance of the oxide. *As the magnitude of the accumulating voltage decreases, the majority carrier concentration decreases at the surface, causing the Debye length to increase and the capacitance in the silicon to decrease. *In depletion, the depletion width increases, causing the capacitance in the silicon to decrease. It will continue to decrease below the flatband capacitance. *In strong inversion, the inversion layer shields the sub-surface from the metal field lines. The depletion width saturates at X sub d max, the silicon capacitance at C sub silicon min, and the overall MOS capacitance at C sub min. *It should be noted that the inversion layer forms only when the inversion carriers are provided by electron-hole pairs or injection from the junction.

Stay tuned for the conclusion of this article in August!

Ask the Experts

Q: We are using the growth equation (see Excel GROWTH function for details) to model degradation in InGaN laser diodes. Is this approach acceptable for prediction purposes?

A: Using the GROWTH function in Excel presumes that the degradation process will be slow and non-catastrophic. While this approach might be acceptable on a mature process line where no catastrophic degradation occurs, it is quite dangerous to make this assumption across all device types or technologies. Some devices can degrade gradually for a period of time and then exhibit a dramatic, or catastrophic decrease in output.

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

August 29, 2011
Boston, Massachusetts

The 6th Annual AMFA is just around the corner! Please plan now to attend; registrations are open until July 30th. Semitracks' President Christopher Henderson will be running the event this year.

Learn more about this conference at:
http://www.amfaworkshop.org/

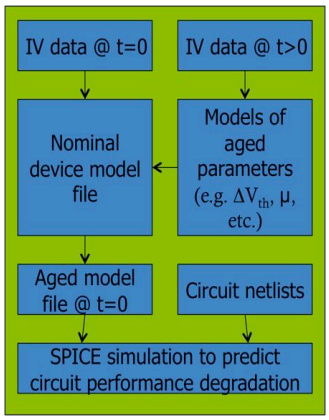
New Semitracks Blog!

Semitracks has started a blog to keep you up to date on industry developments and items that affect Semiconductor Product Engineering and Reliability. In addition to industry developments, we'll include some short articles on technology items of interest. These may vary from historical items that help place current developments in context, to future developments that are likely to affect the industry. If you have comments or feedback, or topics you would like to see addressed, please feel free to e-mail us at info@semitracks.com.

See it for yourself at:
http://www.semitracks.com/index.php/en/blog

Technical Tidbit – Compact Modeling

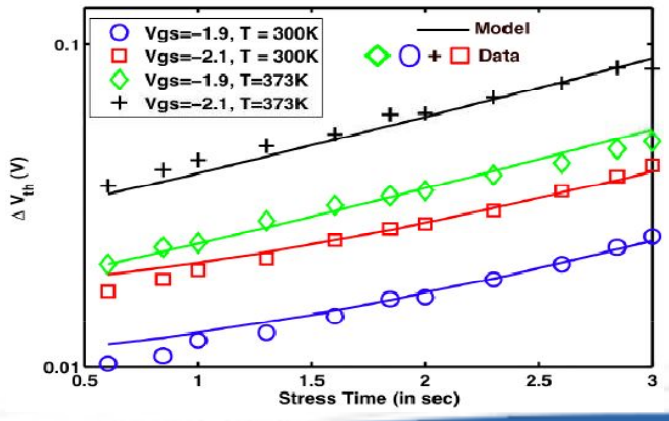
In reliability circles today, design for reliability receives a lot of attention. Within this discipline, there are a number of researchers developing compact models for reliability degradation. What exactly is a compact model? A compact model is a simplified way of thinking about a reliability degradation mechanism in terms of an input to a standard simulation tool, like SPICE. One would take reliability measurements on test structures to get data. This could be a failure mechanism like Negative Bias Temperature Instability (NBTI), Channel Hot Carrier (CHC) Degradation, Time-Dependent Dielectric Breakdown (TDDB), etc. One then fits the data to parameters that exist within the model, like threshold voltage, mobility, etc. The parameters are measured at zero stress and after stress. This forms the basis for nominal parameters and aged parameters. These parameters can then be used to simulate the behavior of standard cell libraries, or analog/mixed signal blocks. The results would then show behavior before and after stress conditions for various circuits. These changes can then be used to predict larger effects that might occur at the architectural level in the IC.



-Take reliability measurements on transistors (e.g. CHC or NBTI)

-Fit parameters to data (e.g. DV$_{th}$, μ, etc.)

-Incorporate parameters into SPICE simulations



Upcoming Courses

ESD Design and Technology

August 23-25, 2011 – San Jose CA

Interconnect Process Integration

August 24-26, 2011 - Singapore

IC Packing Metallurgy

September 12-13, 2011 – Munich, Germany

Wafer Fab Processing

September 26-29, 2011 - Singapore

Failure and Yield Analysis

October 3-6, 2011 – San Jose CA

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or e-mail us at info@semitracks.com.

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by email at jeremy.henderson@semitracks.com.

We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our website!

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