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YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Transfer Molding

By Christopher Henderson

In this month's Feature Article, we continue our series on Transfer Molding. Transfer Molding is one of the more common steps in semiconductor packaging, and provides protection for the sensitive semiconductor components and packaging interconnect. In this article, we will continue our discussion of the characteristics of mold compounds.

Hot hardness is another characteristic of mold compounds. Hot hardness measures the stiffness and resilience required for ejection from the mold plates. Different mold compounds reach the required hardening at a different degree of polymerization. Most compounds require a 60 to 90% conversion or polymerization in order to eject properly from the mold plates. Engineers measure hot hardness by using a type D durometer. It measures hardness while package is on the lower mold half, and is designed to measure the hardness of rubber, plastic, soft metals, and so forth. There is a standard, ASTM D2240-95, that specifies how to perform this test. It is based on penetration of a specific indenter. The optimum value of hardness for injection is 70 or higher. The test is performed by testing the hardness at increasing intervals of cure time. A mold compound is then ready for injection when the hardness value levels off. It is a very useful test for optimizing productivity, or throughput related to the transfer molding process.

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- Semiconductor Technology Overview
- Product Qualification Overview

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Figure 1 shows an example of the hot hardness indenter, shown on the left, and durometer, shown on the right. The durometer measures the applied force on the sample when the indenter indents the material to a certain distance. The indenter has a tip with a radius of 30 degrees. Engineers make the measurement when the indenter goes into a depth of 2.5 millimeters plus or minus 0.04 millimeters.

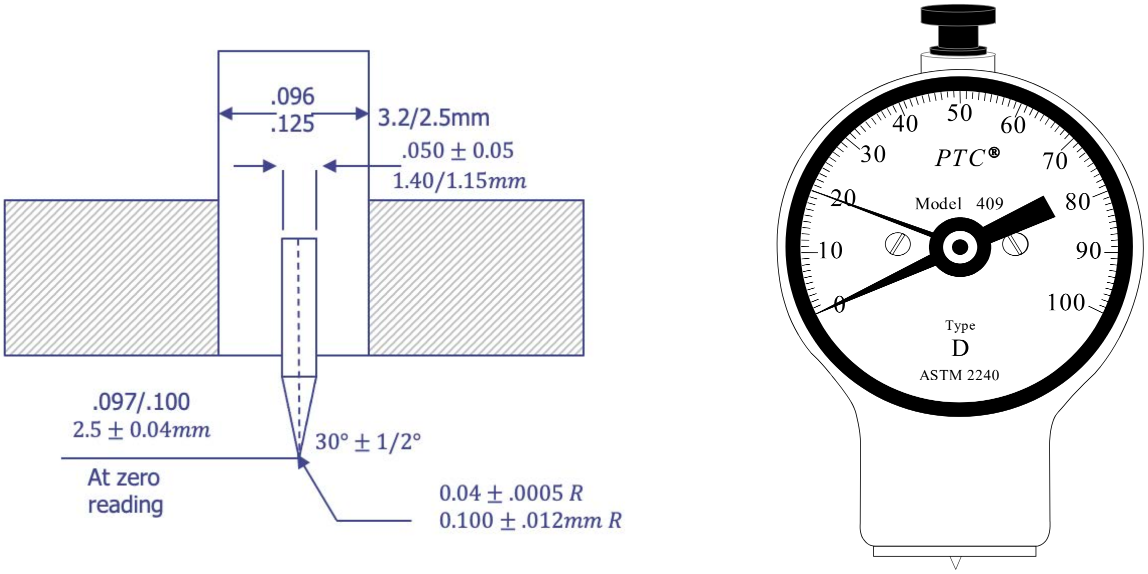


Figure 1- Calibration standard of a type D durometer (left), and a typical durometer (right).

Figure 2 shows an example graph generated using the hot hardness test. This data shows two different mold compounds and their hardness levels, known as Hardness Shore D, measured over a time range from 0 to 100 seconds. The Plaskon 3400F sample performs better from a time perspective, but obviously one must make into account other factors as well, when choosing a mold compound.

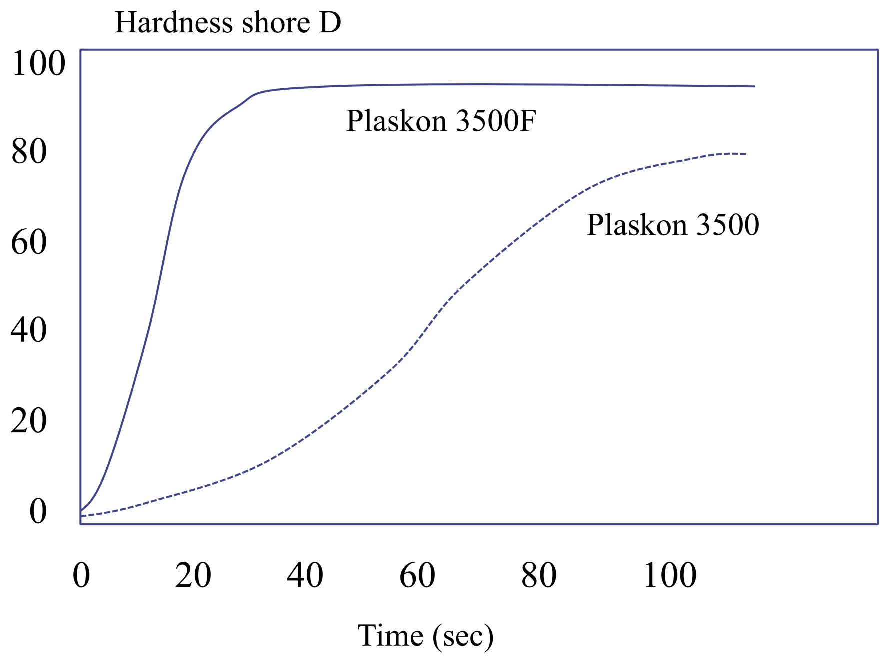


Figure 2- Example hot hardness curves for two different mold compounds at 175ºC.

The next characteristic of mold compound to examine is adhesion. Adhesion is the bonding between primary and secondary valence forces of the mold compound and other packaging elements, like the die, leadframe, bondwires, and die attach. This creates an effective seal against contaminants and moisture, which leads to improved reliability for the component. There are various tests that can be performed to assess adhesion. They include the 180º peel test, the tab pull test, and the button shear test. These types of tests typically examine the adhesion of the mold compound to the silicon die or the passivation layer. In these adhesion tests, the cured mold compound and chip are pulled apart from each other. There are specific types of molds used to form the shape of the bonded part.

The diagrams in Figure 3 show cross-section views of the peel test approach. First, one fills a pot with mold compound, and applies pressure and heat to bond the mold compound to the test sample, which is typically a passivated die. Next, the plunger is retracted, peeling the cured mold compound away from the test sample. The peeling force can be measured during the process.

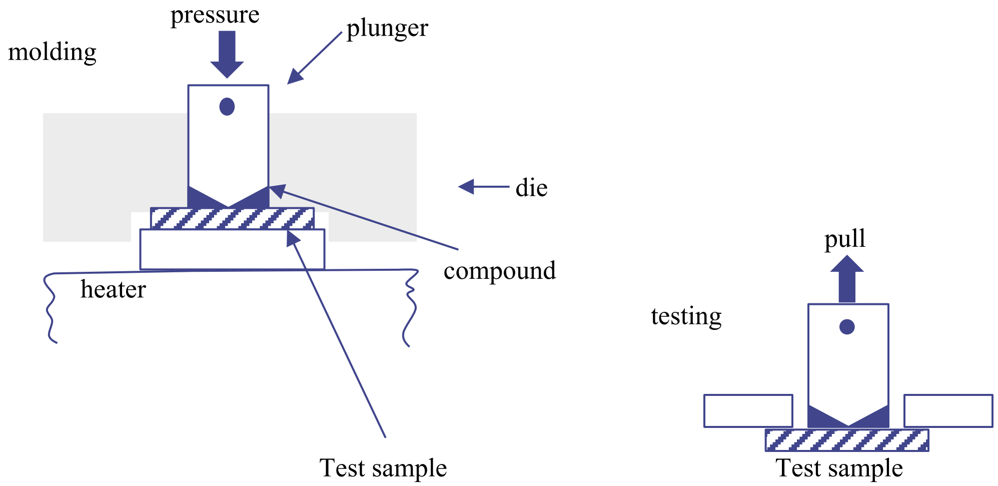


Figure 3- Graphic illustration showing the molding and test procedure for adhesion between the cured mold compound and silicon die, or its passivation layer.

Another characteristic of mold compounds is releasability. Releasability is important, because if the release process is poor, the overall packaging process requires extra cleaning time when the mold compound sticks to the mold. Furthermore, if the release process is poor, if may damage the packaged part. Therefore, process engineers need to add the proper amount of release agents into the mold compound formulation. These percentages typically range from 0.3 to 1.0 percent, and the amount of agent and the releasability are directly related to each other, as we show in the graph in Figure 4. In general, more release agent leads to a better release outcome; however, if there is too much release agent, the adhesion properties will suffer.

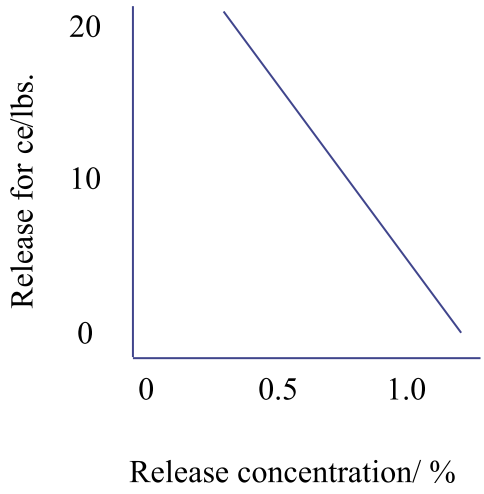


Figure 4- Graph showing releasability vs. concentration for a release agent.

Finally, two additional characteristics of mold compound that are important to understand are resin bleed and flash. Resin bleed occurs when mostly the resin component of the mold compound seeps through parting lines in the mold plates. Flash occurs when filler particles, as well as resin, escape the parting lines in the mold plates. Bleed typically occurs when the viscosity of the compound is either too low or the transfer pressure is too high. Flash, along with bleed, can occur when the mold halves are not parallel to each other, or the clamp pressure is not adequate. Resin bleed and flash can be evaluated using a specially prepared mold. This mold includes a series of rectangular flow channels starting from a central cull area. The depths of channels typically start at 5 μm and increase in steps of 5 μm. The materials will start flowing and travel the longest in the shallowest channels, creating a potential for bleed and flash. Since this test requires special hardware that does not match that of a typical set of mold plates used for production, it is best to use production plates and equipment for testing this characteristic.

In next month's Feature Article, we will continue our discussion of Transfer Molding by discussing Storage and Handling.

Technical Tidbit: Nanoindentation

This month's Technical Tidbit covers the materials characterization technique known as nanoindentation, which is an important technique to examine dielectric materials. We show a diagram of the instrument in Figure 1. A loading coil applies pressure to a diamond tip. The tip presses into the sample, creating an indentation in the sample. The displacement gauge measures the depth the tip presses into the sample, and this depth measurement can be converted into a hardness number for the sample. A Berkovitch (trigonal) diamond tip is used to measure the applied load vs. the displacement. This allows the engineer to obtain the Young's modulus and hardness measurements.

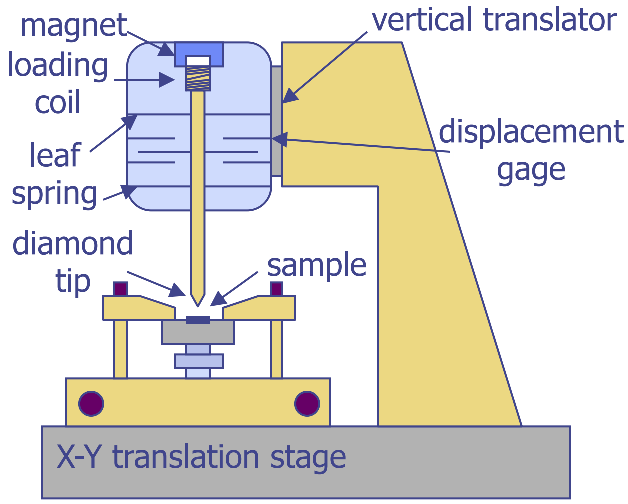
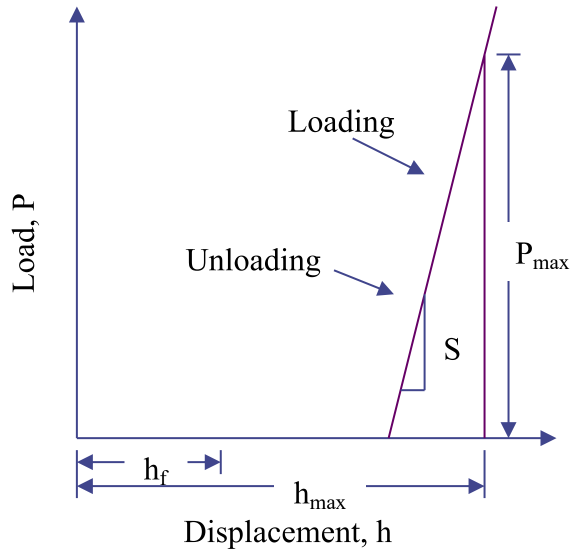


Figure 1- Diagram of the nanoindentation hardware.

The graph in Figure 2 shows the load as a function of displacement. Notice that the loading curve generally requires a larger load to achieve a particular displacement than the unloading curve does. This is generally due to the plastic deformation of the materials that occurs during the loading process, which in turn means there is less "rebound" in the materials during the unloading process.

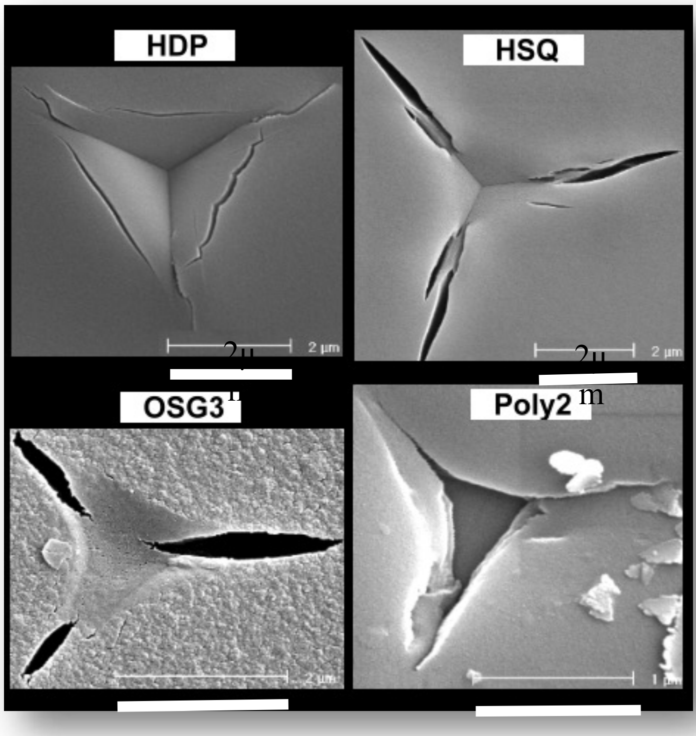
$$E_r = \frac{\sqrt{\pi}}{2} \frac{S}{\sqrt{A}}$$



$$H = \frac{P_{max}}{A}$$

Figure 2- Graph showing load as a function of displacement in a nanoindentation system.

The Scanning Electron Microscope, or SEM images in Figure 3 show nanoindentation marks on four different materials. At the upper left, we show a high-density plasma oxide; at the upper right, we show hydrogen silsequioxane, at the lower left, we show an organo-silicate glass, and at the lower right, we show a polysilicon-2 layer that has some dielectric material beneath it. Notice that the high-density plasma oxide has the highest Young's modulus at 72 gigapascals. The polysilicon layer has the lowest Young's modulus at 4.3 gigapascals for two reasons. First, the material is polycrystalline, which causes the material to break more easily, and second, the material sits on top of dielectrics, which increases the fragility of the polysilicon layer to a certain extent.



E=72GPa
H=10GPa

E=7GPa
H=0.9GPa

E=12.2GPa
H=1.7GPa

E=4.3GPa
H=0.3GPa

Figure 3- SEM images of nanoindentation marks.

Although nanoindentation is not a commonly used technique, it is useful for developing a deeper understanding of thin film materials properties and interfaces. As such, process and reliability engineers should be aware of the technique.

Ask The Experts

Q: What is the thermal conductivity of the mold compound epoxy resin by itself?

A: The mold compound epoxy resins by themselves have typical conductivity values of 0.1-0.2 W/mK. More generally, epoxies are traditionally considered to be thermally insulative with typical thermal conductivity values of 0.1-0.2 W/mK. To create a more thermally conductive adhesive, process engineers add filler systems to allow heat to flow more quickly through the cured matrix. Depending on the type of filler system used, cured epoxy can have a resulting bulk thermal conductivity value from 2 W/mK up to as high as 10 W/mK.

Course Spotlight: FAILURE AND YIELD ANALYSIS

OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Your industry needs competent analysts to help solve these problems. ***Failure and Yield Analysis*** is a 4-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a ***Do It Right the First Time*** approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

Participants will learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. **The Process of Failure and Yield Analysis.** Participants will learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.

2. **The Tools and Techniques.** Participants will learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools, light emission, electron beam tools, optical beam tools, decapping and sample preparation, and surface science tools.

3. **Case Histories.** Participants will identify how to use their knowledge through the case histories. They will learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

COURSE OBJECTIVES

1. This course will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.

2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.

3. This course will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.

4. This course will offer a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.

5. Participants will be able to identify basic technology features on semiconductor devices.

6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.

7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

COURSE OUTLINE

DAY 1

1. Introduction

2. Failure Analysis Principles/Procedures
   a. Philosophy of Failure Analysis
   b. Flowcharts

3. Gathering Information

4. Package Level Testing
   a. Optical Microscopy
   b. Acoustic Microscopy
   c. X-Ray Radiography
   d. Hermetic Seal Testing
   e. Residual Gas Analysis

5. Electrical Testing
   a. Basics of Circuit Operation
   b. Curve Tracer/Parameter Analyzer Operation
   c. Quiescent Power Supply Current
   d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
   e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
   f. Automatic Test Equipment
   g. Basics of Digital Circuit Troubleshooting
   h. Basics of Analog Circuit Troubleshooting

DAY 2

6. Decapsulation/Backside Sample Preparation
   a. Mechanical Delidding Techniques
   b. Chemical Delidding Techniques
   c. Backside Sample Preparation Techniques

7. Die Inspection
   a. Optical Microscopy
   b. Scanning Electron Microscopy

8. Photon Emission Microscopy
   a. Mechanisms for Photon Emission
   b. Instrumentation
   c. Frontside
   d. Backside
   e. Interpretation

9. Electron Beam Tools
   a. Voltage Contrast
      i. Passive Voltage Contrast
      ii. Static Voltage Contrast
      iii. Capacitive Coupled Voltage Contrast
      iv. Introduction to Electron Beam Probing
   b. Electron Beam Induced Current
   c. Resistive Contrast Imaging
   d. Charge-Induced Voltage Alteration

DAY 3

10. Optical Beam Tools
   a. Optical Beam Induced Current
   b. Light-Induced Voltage Alteration
   c. Thermally-Induced Voltage Alteration
   d. Seebeck Effect Imaging
   e. Electro-optical Probing

11. Thermal Detection Techniques
   a. Infrared Thermal Imaging
   b. Liquid Crystal Hot Spot Detection
   c. Fluorescent Microthermal Imaging

12. Chemical Unlayering
   a. Wet Chemical Etching
   b. Reactive Ion Etching
   c. Parallel Polishing

DAY 4

13. Analytical Techniques
   a. TEM
   b. SIMS
   c. Auger
   d. ESCA/XPS

14. Focused Ion Beam Technology
   a. Physics of Operation
   b. Instrumentation
   c. Examples
   d. Gas-Assisted Etching
   e. Insulator Deposition
   f. Electrical Circuit Effects

15. Case Histories

Upcoming Courses:

Public Course Schedule:

Semiconductor Technology Overview - February 3-4, 2025 (Mon.-Tues.) | Phoenix, Arizona - $1,295

Product Qualification Overview - February 5, 2025 (Wed.) | Phoenix, Arizona - $695

IC Packaging Technology - February 10-11, 2025 (Mon.-Tues.) | Phoenix, Arizona - $1,195 until Mon. Jan. 20

Advanced CMOS/FinFET Fabrication - February 19-20, 2025 (Wed.-Thurs.) | Phoenix, Arizona - $1,195 until Wed. Jan. 29

Failure and Yield Analysis - March 3-6, 2025 (Mon.-Thurs.) | Phoenix, AZ - $2,095 until Mon. Feb. 10

Have an idea for a course? If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please email us at info@semitracks.com

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!