Issue 20 February 2011

InfoTracks

Semitracks Monthly Newsletter

Semitracks Online Training

Have you ever thought: there must be an easier way to learn about the semiconductor field without having to take so much time out of my busy schedule to attend classes…

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Future Memory Technologies – Part 2

By Christopher Henderson

Another contender as a future non-volatile memory technology is Resistive Random Access Memory, sometimes shortened to RRAM or ReRAM. A prototype RRAM chip is shown in Figure 1. Several major manufacturers are working on RRAM, including: Samsung, Micron, Macronix, and Elpida Memories. The technology is somewhat similar to Conductive Bridging RAM and Phase Change Memory, which we discussed in the previous issue. IMEC in Belgium has also done extensive research into this technology.

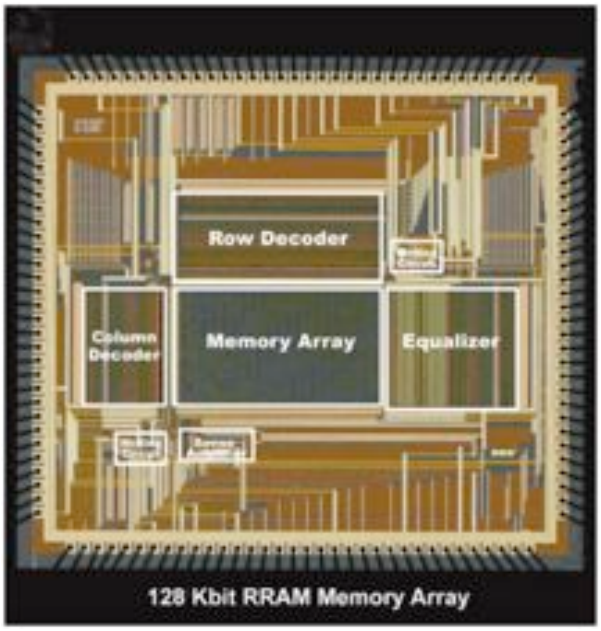

Figure 1. 128 Kbit RRAM array from a collaboration between AIST, Sharp, ULVAC, and Kanazawa University.

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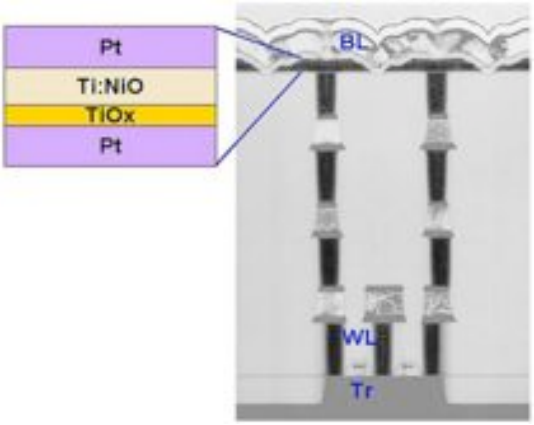

Figure 2. Cross-section of an RRAM cell. The switch is located in the backend of the process.

The basic concept is that one can create a conducting path through a dielectric layer by applying a high voltage (see Figure 2). The conducting path, or filament can be reset, restoring the high resistance path and reformed to create a low resistance path at will. This filament path may actually be multiple paths, according to researchers. There are different types of materials that can exhibit this behavior. They include perovskites, chalcogenides, and transition metal oxides. Some of the leading transition metal oxides include nickel oxide, titanium oxide, tungsten oxide, hafnium oxide, and heterostructures such as aluminum oxide/titanium oxide. Ironically, even silicon dioxide can be used for this application. The failure mechanism engineers try to avoid in standard CMOS, time-dependent dielectric breakdown, is the mechanism by which the programming occurs.

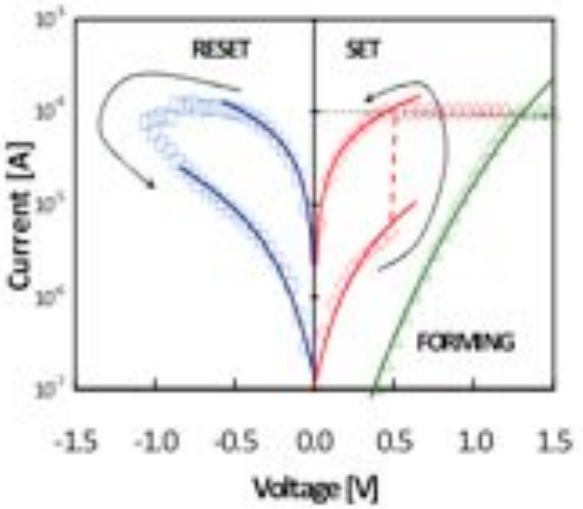

Figure 3. Forming, reset and set currents for a Resistive RAM test structure (area = $2x10^{-5}$ cm^2, HfO_2 thickness of 5nm and Ti_xN_y electrodes. The researchers used a current compliance of 10^{-4} Amps

RRAM has the potential to become the front runner for future memory technologies. RRAM can operate much faster than Phase Change Memory. The switching time can be on the order of 10ns. Compared to MRAM, RRAM has a much smaller cell size. The cell size is less than $8F^2$, where F is the smallest feature size. It can also function at lower operating voltages than standard flash memories. RRAM also has the potential to scale down below 30nm. While standard flash memory is now below 30nm, the cell size is larger, so RRAM can still accommodate more cells in the same silicon area. Researchers believe that the mechanism might involve oxygen motion, which might allow for scaling down to as low as 2nm. The filament dimensions during the forming process are also key factors to a stable, reliable device(1)

(1) G. Bersuker, et. al., "Diode-less Nano-scale ZrOx/HfOx RRAM Device with Excellent Switching Uniformity and Reliability for High-density Cross-point Memory Applications," ***Proc. Int. Elec. Dev.***

Ask the Experts

Q: I am detecting sulfur on the top of packaged devices as well as on the bond pads of printed circuit boards in our manufacturing process. What might be causing this contamination?

A: There are several common sources of sulfur in PCB manufacturing and assembly. They include: outgassing of elastomers vulcanized with sulfur, contamination in the PCB board itself, sulfur in the solder resist material, stop-off lacquer, contamination from paper or paperboard (cardboard) materials, and industrial environments or city environments with high sulfur or sulfide concentrations.

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

IRPS
International Reliability Physics Symposium

April 10-14, 2011
Monteray, CA, USA

For nearly 50 years, IRPS has been the premier conference for engineers and scientists to present new and original work in the area of microelectronics reliability. Drawing participants from the United States, Europe, Asia, and all other parts of the world, IRPS seeks to understand the reliability of semiconductor devices, integrated circuits, and microelectronic assemblies through an improved understanding of both the physics of failure as well as the application environment.

If you would be interested to meet with Semitracks personnel at IRPS, please call or e-mail us.

Learn more about this conference at:
http://www.irps.org/

Semitracks Online Training Spotlight

Our online semiconductor training courses can be customized for your job function. The structure of the material allows you, the user, to learn when you have a few moments free, alleviating the need to carve a large block out of your schedule. Other disciplines allow you to cross-train for potential promotions or transfers or to simply do a better job in your current position. The material is always current and interactive, allowing you to learn the material easily. You can search our databases for answers to questions you might have or simply use it as a reference.

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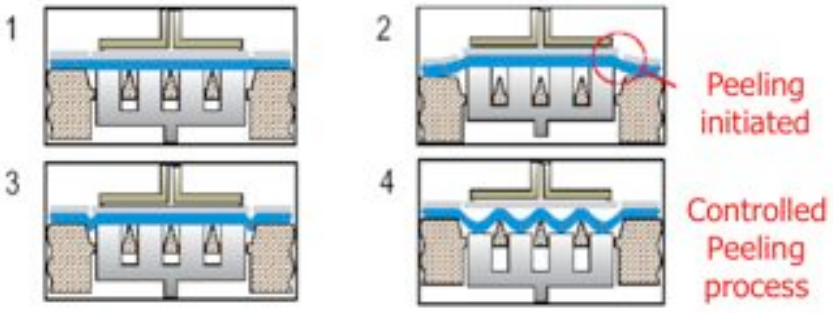
Technical Tidbit

Dice Before Grinding

Usually, wafers are ground down before the sawing operation. However, some organizations have been exploring a process where the sawing operations occur first, followed by the backgrinding operation. This is sometimes referred to as "Dice Before Grinding", or DBG. The conventional grind before sawing is shown in the upper row. Three variations of the DBG approach are shown in the lower rows. DBG can be done with or without Chemical Mechanical Polish, or CMP. CMP can be useful when a higher quality interface is needed between dice. DGB can also be accomplished using standard wafer saw processes, or with reactive ion etching.

One concern with thin dice is how to handle them. The dice are especially prone to damage during pick and place operations. The key is to initiate the peeling process from the backing tape without damaging the dice. This diagram shows an approach to doing just that. This process involves raising and then lowering the ejector assembly. By raising it, one can initiate the peeling process at the edge of the die. By then lowering the ejector assembly, one can achieve a controlled peeling process in which the backing tape peels away from the die, but the die is held in position by the ejector pins.



Upcoming Courses

Failure and Yield Analysis

February 28-March 3, 2011 - San Jose, CA, USA

Wafer Fab Processing

February 28-March 3, 2011 - San Jose, CA, USA

IC Packaging Design and Modeling

March 7-9, 2011 - San Jose, CA, USA

Yield Analysis

March 10-11, 2011 – Kuala Lumpur, Malaysia

Wafer Fab Processing

March 14-18, 2011 - Kuala Lumpur, Malaysia

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or e-mail us at info@semitracks.com.

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by email at jeremy.henderson@semitracks.com.

We are always looking for ways to enhance our courses and educational materials.

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