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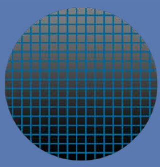

SEMITRACKS, INC.

INFOTRACKS

YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Transfer Molding

By Christopher Henderson

In this month's Feature Article, we continue our series on Transfer Molding. Transfer Molding is one of the more common steps in semiconductor packaging, and provides protection for the sensitive semiconductor components and packaging interconnect. In this article, we will begin our discussion of the characteristics of mold compounds.

In order for mold compound to work properly in its applications in packaging, it must meet certain characteristics. These characteristics are often tested and certified by the supplier, but the packaging organization may wish to verify the results through their own incoming inspections and tests. Ultimately, the question is whether or not the material will work properly in the manufacturing operations, and on through the lifetime of the component in the field. There may also be storage and handling requirements for the mold compound. Use of an appropriate procedure will help prolong the shelf life of the material. There are eight common molding characteristics that compound manufacturers will examine. They include: Viscosity, Spiral flow length, Gel time, Hot hardness, Adhesion (to leadframe/substrate), Releasability (from mold), Resin bleed, and Flash. We will discuss these in more detail below.

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Probably the most important mold compound characteristic, from a manufacturing process perspective, is viscosity. It is defined as a quantity expressing the magnitude of internal friction, as measured by the force per unit area resisting a flow. Viscosity is important to understand, because it is critical to ensure cavity filling without damaging wire bonds, chips, or any parts of the mold. Viscosity is normally measured with a viscometer, like the Brabender Viscograph, shown in Figure 1. This machine is a type of torque rheometer that measures resistance to twin screws that turn within the liquid material. This is known as "apparent viscosity." This equipment can provide useful information about the lifecycle of a thermoset at a given molding temperature. A big problem with thermosetting compounds is that their viscosity at a particular temperature and time is not enough information to understand their behavior. The key points in measuring the viscosity include the minimum torque reached, and the time duration at minimum torque. We should also note that for thermoplastics, the viscosity does not change if the temperature is constant.

Figure 1- Image of a Viscograph system (courtesy Brabender).

Figure 2 shows a notional example of a Brabender torque rheometer time curve at a given mold temperature. We plot torque as a function of time. In a typical mold compound, the torque initially falls as the plastic melts and becomes more liquid. It stays in the liquid phase with a minimal torque value for a given period of time. Then, after some amount of time, the torque begins to increase, as the mold compound cures.

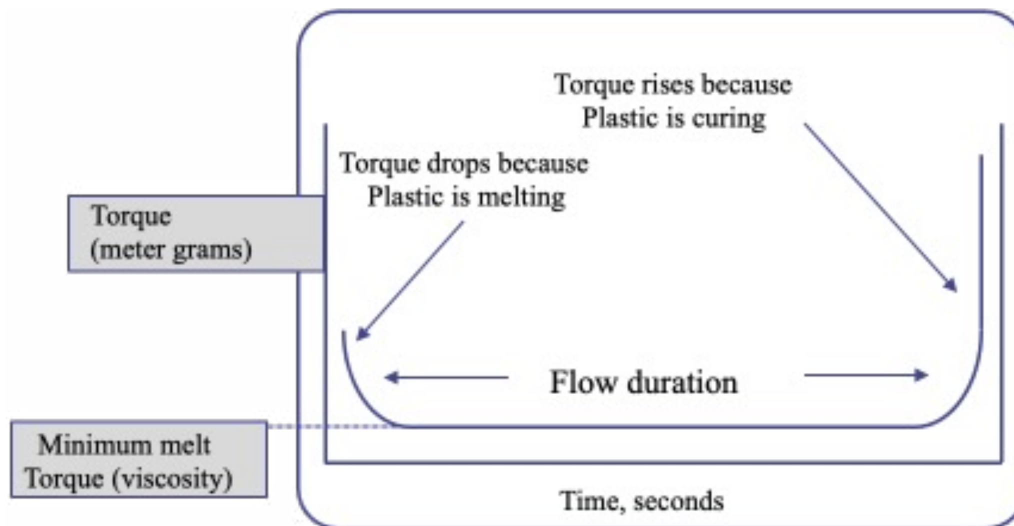

Figure 2- Brabender torque rheometer time curve at mold temperature.

Now, let's look at mold compound viscosity change as a function of the mold injection process. One typically creates a viscosity curve for a given mold compound material. Please refer to the graph in Figure 3 for the following discussion. Initially, when the mold injection process starts, the mold compound is a solid tablet. At this point, the viscosity is quite high, represented by point A on the graph. As the mold compound tablet begins to melt, the viscosity drops significantly, represented by points B and C, eventually reaching a minimum value at point D in the graph. In the range between points C and E, the mold compound flows through the runners and gates from the pot and enters the mold cavities. After the mold compound fills the cavities, the viscosity increases as the resin-hardener system reaches its gelation point, represented by point F. As the mold compound cures, the viscosity continues to increase, represented by point G, reaching a point where the packages can be released from the mold plates. The viscosity increases further as the mold compound reaches its final hardness, represented by point H. There are a couple of important points to make about this process. The time between points C and E on the curve represents the maximum time it should take to the mold compound to fill the mold cavities. If they fill too soon, then there will be resin bleed into surrounding structures. If they fill too late, the abrasive action of the mold compound will result in increased wire sweep, potential damage, and incomplete filling.

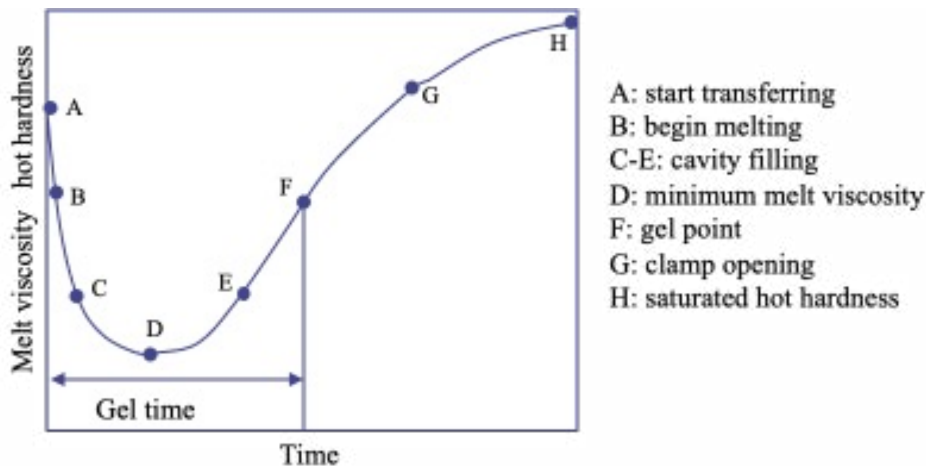

Figure 3- Graphic illustration of melt and cure properties in transfer molding.

One technique for measuring viscosity in a controlled manner is to measure spiral flow length. This is the flow length along a spirally bent tube at a given temperature and pressure. The flow of the mold compound stops when the gel point is reached. This procedure is codified in ASTM Standard D3123-94. The recommended pressure is 1000 pounds per square inch and the recommended mold temperature is 150ºC. One records the flow length and time until the flow ceases. This technique measures the melt viscosity, gelation rate, and fusion under pressure as a single parameter – spiral flow length. Generally, this is the basis for defining floor and shelf life for a mold compound.

Another characteristic of mold compound is its gelation time, or gel time. Gel time is defined as the point when the three-dimensional structure of the compound begins to appear. This is accompanied by a significant increase in viscosity, or inability to smear into a thin coating. Process engineers use gel time to establish the upper limit of the mold cycle time. Gel time is measured with a gel plate (a type of hot plate) with precise temperature control and probe capability. One places a small amount on the plate at a set temperature, which is typically 170ºC. One uses a wooden stick to stir and smear the thin coating, and then looks for signs of three-dimensional structure forming in the liquid. This technique is quite subjective, and therefore, requires an experienced technician.

In next month’s Feature Article, we will continue our discussion of Transfer Molding Characteristics.

Technical Tidbit: Endpoint Detection for Dry Etch Processes

This month's Technical Tidbit covers endpoint detection for dry etch processes. End point detection is critical during the etch process. We need methods to be able to determine when an etch step is complete. In a dry etch application, it is obviously desirable to do this as an in-situ measurement, so that we can provide immediate feedback to the etch system to terminate the etch step. In general, time is not an effective method for determining when the etch should stop due to chamber ageing effects, loading effects on the wafers that vary due to product type, and other non-uniformities. Therefore, there are two basic methods of determination: optical emission spectroscopy and laser interferometry/reflectance. Optical emission spectroscopy is by far the most common method used for end point detection. This technique measures the change in intensity of the optical emission from the wafer as the etch process progresses. This emission is the optical radiation emitted when electrons relax, or fall from a higher energy state into a lower energy state. As a point of clarification, the electrons in the gas molecules in the plasma gain energy from the RF energy used in the dry etch process. The intensity of the optical emission is a function of the relative concentration of the gas species in the plasma used for the etch process, and the by-products produced by the etch process. Process engineers will typically monitor both the reactive species and the by-product species with this technique.

The concept behind optical emission spectroscopy is straightforward. Figure 1 illustrates this concept. When an incident electron interacts with an element, it can scatter off of a valence electron, ejecting the electron from its shell location. The primary electron will also scatter away from the element. This is a higher energy state, and physics tells us that elements prefer a lower energy state. After a short period of time, an electron in a higher energy shell location will fall into the empty shell location, giving off a photon. This photon will have a characteristic wavelength, defined by the element and the shell transition.

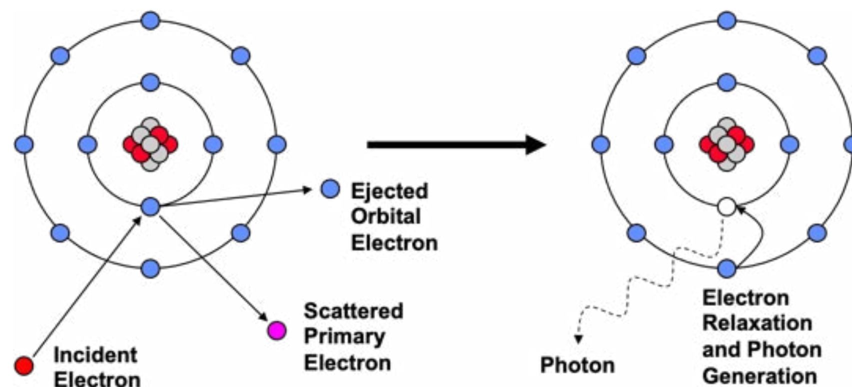

Figure 1- Concept behind optical emission spectroscopy.

Table 1 shows the monitored species and emission wavelengths for some common thin film materials. The wavelengths monitored generally fall in a range from 250 to 800 nm, or from the near-ultraviolet through the visible spectrum.

Film	Species Monitored	Wavelength (nm)
Photoresist	CO	297.7, 483.5, 519.8
	OH	308.9
	H	656.3
Silicon, Polysilicon	F	704
	SiF	777
Silicon Nitride	F	704
	CN	387
	N	674
Aluminum	AlCl	261.4
	Al	396

Table 1- Species and emission wavelength for optical emission endpoint detection.

The second technique is laser interferometry/reflectance. This technique is also called optical interferometry. This technique measures the intensity of the light reflected from the thin films on the wafer. Laser interferometry measures the intensity of the signal from transparent films on reflective substrates, while laser reflectance measures the intensity of the signal from non-transparent films. With this information, one can infer the remaining thickness of the film. The major disadvantage of this technique is that it can only use information from a small area on the wafer. Many modern tools will have one or both techniques integrated into the tool to aid in metrology efforts.

Ask The Experts

Q: I have a question about etching silicon. Is it possible to perform a decorative etch that highlights the differences between n-type and p-type silicon, or can you only highlight doping differences, as is the case with traditional etches like the Dash Etch?

A: This is an interesting question, and depends on what lengths you're willing to go to highlight the difference. Some groups have tried, and had varying degrees of success, developing etches that are selective to n-type and p-type silicon. One researcher, Simon Wang, published work on this topic when he was working at Delco Electronics (a subsidiary of GM). He used a pulsed electrochemical approach. The reference for the work is below:

S. Wang, et.al., "An Etch-Stop Utilizing Selective Etching of N-Type Silicon by Pulsed Potential Anodization," IEEE Jour. Micro. Sys., Vol. 1, No. 4, pp. 187-192, Dec. 1992

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Course Spotlight: ADVANCED CMOS/FINFET FABRICATION

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" ***Advanced CMOS/FinFET Fabrication*** is a 2-day course that offers detailed instruction on the processing used in a modern integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By concentrating on the latest developments in CMOS and FinFET technology, participants will learn why FinFETs are fast becoming the technologies of choice at feature sizes below 20nm. Our instructors work hard to explain semiconductor processing without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants will learn basic, but powerful, aspects about CMOS fabrication and FinFET technology. This skill-building series is divided into four segments:

1. **Front End Of Line (FEOL) Overview.** Participants will study the major developments associated with FEOL processing, including Ion Implantation, Rapid Thermal Annealing (RTA) for implants and silicides, and Pulsed Plasma Doping. They will also study alternate substrate technologies like SOI, as well as High-k/Metal Gates for improved leakage control.

2. **Back End Of Line (BEOL) Overview.** Participants will study the major developments associated with BEOL processing, including copper metallization and Low-k Dielectrics. They will learn about why they're necessary for improved performance.

3. **FinFET Manufacturing Overview.** Participants will learn how semiconductor manufacturers are currently processing FinFET devices and the difficulties associated with three-dimensional structures from a processing and metrology standpoint.

4. **FinFET Reliability.** Participants will study the failure mechanisms and techniques used for studying the reliability of these devices.

COURSE OBJECTIVES

1. This course will provide participants with an in-depth understanding of Bulk technology, SOI technology and the technical issues.

2. Participants will understand how Hi-K/Metal Gate devices are manufactured.

3. Participants will also understand how FinFET devices are manufactured.

4. This course will provide a look into the latest challenges with copper metallization and Low-k dielectrics.

5. Participants will understand the difficulties associated with non-planar structures and methods to alleviate the problems.

6. Participants will be able to make decisions about how to evaluate FinFET devices and what changes are likely to emerge in the coming years.

7. Participants will briefly learn about IC reliability and the failure modes associated with these devices.

8. Participants will see a comparison between FinFETs and new alternatives (such as Gate All Around (GAA) structures and nanosheets).

COURSE OUTLINE

DAY 1

1. Introduction – Advanced CMOS Fabrication

2. Front End Of Line (FEOL) Processing
   - a. SOI and FD-SOI
   - b. Ion Implantation and Rapid Thermal Annealing
   - c. Pulsed Plasma Doping
   - d. Hi-K/Metal Gates
   - e. Processing Issues
     - i. Lithography
     - ii. Etch
     - iii. Metrology

3. Back End Of Line (BEOL) Processing
   - a. Introduction and Performance Issues
   - b. Copper
     - i. Deposition Methods
     - ii. Liners
     - iii. Capping Materials
     - iv. Damascene Processing Steps
   - c. Lo-k Dielectrics
     - i. Materials
     - ii. Processing Methods
   - d. Reliability Issues

DAY 2

4. FinFET Manufacturing Overview
   - a. Substrates
     - i. Bulk
     - ii. SOI
   - b. FinFET Types
   - c. Process Sequence
   - d. Processing Issues
     - i. Lithography
     - ii. Etch
     - iii. Metrology

5. FinFET Reliability
   - a. Defect density issues
   - b. Gate Stack
   - c. Transistor Reliability (BTI and Hot Carriers)
   - d. Heat dissipation issues
   - e. Failure analysis challenges

6. Future Directions for FinFETs
   - a. Comparison of FinFETs and other Techniques (GAA, Nanosheets) – Are FinFETs a better choice?
   - b.Scaling

Upcoming Courses:

Public Course Schedule:

Semiconductor Technology Overview - February 3-4, 2025 (Mon.-Tues.) | Phoenix, Arizona - $1,195 until Mon. Jan. 13

Product Qualification Overview - February 5, 2025 (Wed.) | Phoenix, Arizona - $595 until Wed. Jan. 15

IC Packaging Technology - February 10-11, 2025 (Mon.-Tues.) | Phoenix, Arizona - $1,195 until Mon. Jan. 20

Advanced CMOS/FinFET Fabrication - February 19-20, 2025 (Wed.-Thurs.) | Phoenix, Arizona - $1,195 until Wed. Jan. 29

Failure and Yield Analysis - March 3-6, 2025 (Mon.-Thurs.) | Phoenix, AZ - $2,095 until Mon. Feb. 10

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!