

INFOTRACKS

YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY



Transfer Molding

By Christopher Henderson

In this month's Feature Article, we continue our series on Transfer Molding. Transfer Molding is one of the more common steps in semiconductor packaging, and provides protection for the sensitive semiconductor components and packaging interconnect. In this article, we will start a discussion of the constituents of mold compounds.

Let's take a closer look at the composition of the mold compound. Mold compounds consist of an epoxy resin, a hardener, filler particles, a flexibilizer, a catalyst, and a mold release agent. We will make some brief comments about each item now, and then cover them in more detail in the following slides. One particular type of epoxy resin used is biphenyl, which is a dual aromatic ring structure. Another type of epoxy resin used is the multi-aromatic ring structure which is known for its ability to provide better heat resistance. Another option is cyanate esters, which consist of oxygen, carbon and nitrogen atoms bonded to a dual or multi-aromatic ring structure. Bisphenol A is an example of this. Another common epoxy resin is Epoxy Ortho Cresol Novolac, sometimes called EOCN. Cresol Novolac epoxy resins provide high heat-resistance, as well. Another class of high heat resistant epoxy resins are the phenol epoxies.

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Upcoming Courses:

- **Advanced CMOS/FinFET Fabrication**
- **Packaging Failure and Yield Analysis**

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Dicyclopentadiene-Phenol epoxy resin is an example of this. Yet another class of high heat resistant epoxy resins are the phenyl epoxies. Naphthalene-Phenyl epoxy resin is an example of this class. These epoxy resins also have ultra-low conductivity, and low ionic transport. The primary hardeners used in mold compounds are Phenol Novolacs and Anhydride. Phenol Novolacs, or Phenol formaldehyde resins are synthetic polymers obtained by the reaction of phenol and formaldehyde. One reacts phenol and formaldehyde directly to produce a thermosetting network polymer, or one can restrict the formaldehyde to produce a prepolymer which can be molded and then cured with the addition of more formaldehyde and heat. Another category of hardeners are the anhydrides. Anhydride curing agents are some of epoxy's oldest curing agents, and probably the most widely used curing agent in epoxy molding compounds over the history of mold compounds. These chemicals incorporate themselves into the overall structure of the cured material. The primary filler particles are silicon dioxide particles, but aluminum oxide, magnesium oxide, aluminum hydroxide, and titanium oxide can also be used. Most mold compound formulations use a coupling agent, or surfactant, to improve the compatibility between the filler particles and the resin to help improve adhesion properties of the compound. Mold compound formulations also make use of a flexibilizer, or toughening agent. This helps to decrease the Young's Modulus, increase adhesion, and decrease the shrinkage during mold cure. These are typically silicone-based materials. Mold compound also contains a catalyst to help increase the reaction rate. Finally, mold compounds may also contain a mold release agent, flow improvement agents, and color pigments.

The graph in Figure 1 shows the percentages of the main constituents in a typical mold compound formulation. These numbers might vary somewhat from formulation to formulation, but this pie chart will give a good idea as to the approximate values.

- For filler particles, we assume silica particles. The actual percentage can range from 60 to 90%.
- For epoxy resin material, we might use Ortho Cresol Novolac, Biphenyl, Dicyclopentadiene, or some form of a multi-aromatic epoxy resin. The actual percentage can range from 5 to 10%.
- For a hardener, we might use Phenol Novolac, or a Flexible Phenol. The actual percentage can range from 5 to 10%.
- For a Flame Retardant Agent, we might use a metal hydroxide, or a bromine-based compound, or antimony oxide. The actual percentage is less than 10%.
- For a Catalyst, we might use a nitrogen compound or phosphorus compound. The actual percentage is less than 1%.
- For a Coupling Agent, we might use a Silane Compound. The actual percentage is less than 1%.
- For a Mold Release Agent, we might use a Natural or Synthetic Wax. The actual percentage again is less than 1%.
- Finally, there may be other constituents, like a Colorant, or Low-Stress Additive. Again, the actual percentage is less than 1%.

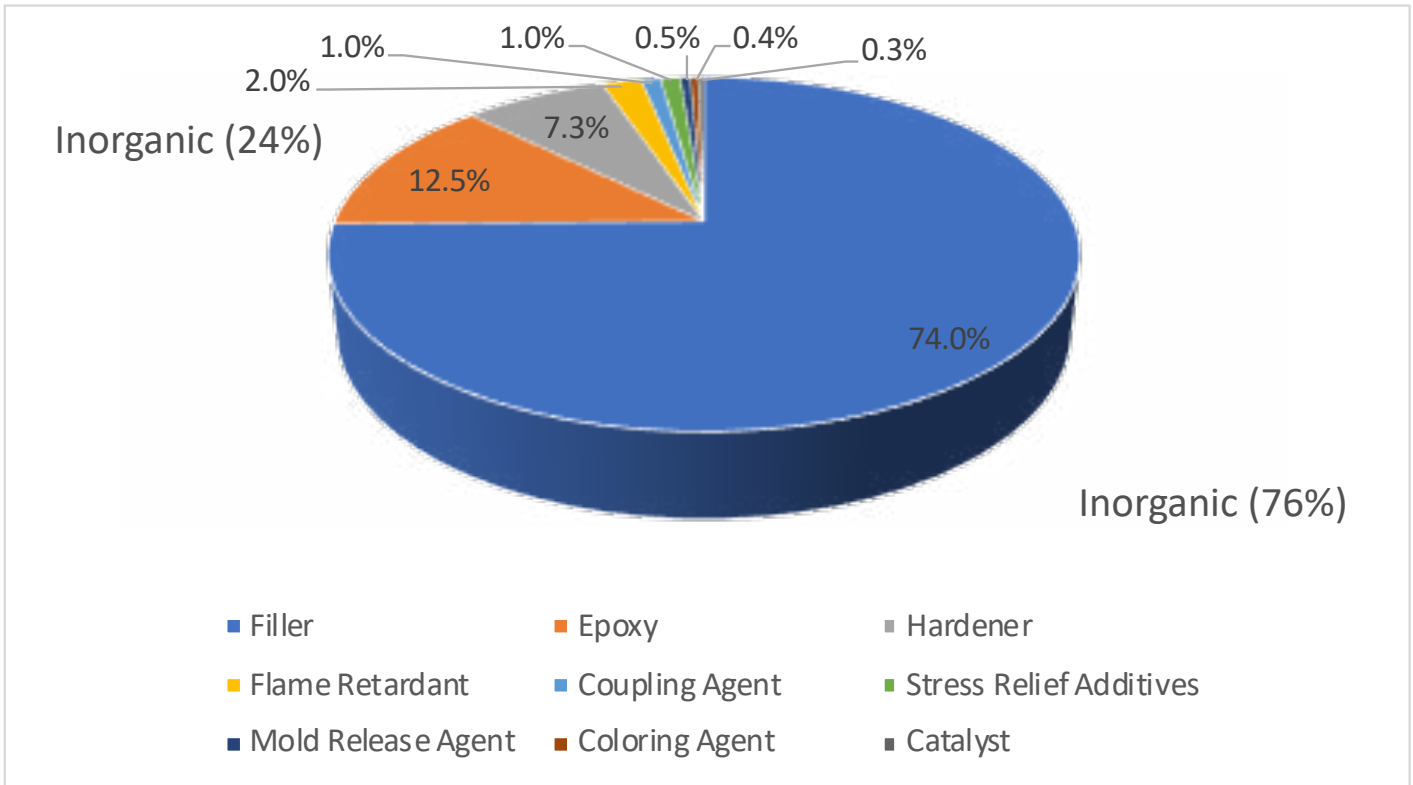


Figure 1- Graph shows the percentage of constituents in a typical mold compound formulation.

Some of the constituents of the mold compound are organic, while others are inorganic. In Table 1, we list the main constituents and the categories to which they belong. To get a sense for how big the mold compound tablets, or preforms, are, we show in Figure 2 various preforms, and a 12-ounce soft drink can for comparison purposes on the right.

Organic Components	Inorganic Components
Epoxy Resin	Filler
Hardener (or Curing Agent)	Coupling Agent
Catalyst (or Accelerator)	Flame Retardant
Flame Retardant	
Mold Release Agent	
Coloring Agent	

Table 1- Table showing categories of mold constituents.

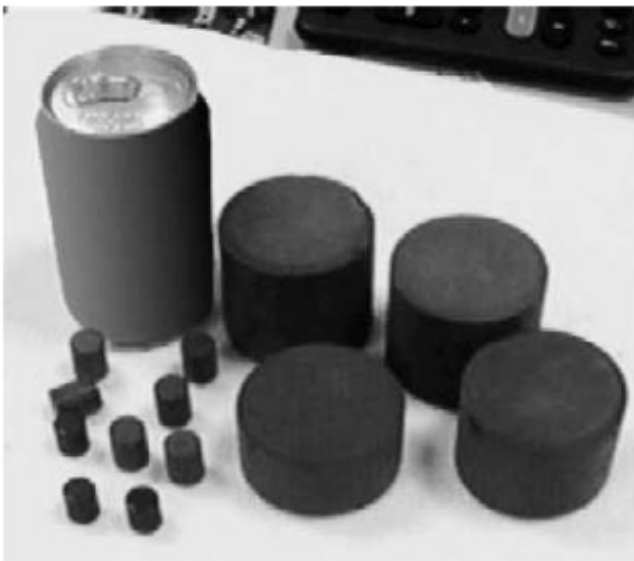


Figure 2- Various sizes of mold compound preforms compared to a 12oz. soft drink can.

In next month's Feature Article, we will continue our discussion of the mold compound constituents.

Technical Tidbit: Exhaust Byproducts During Epitaxial Deposition

This month's Technical Tidbit covers exhaust byproducts that are generated during epitaxial deposition. Exhaust byproducts are a natural occurrence when flowing gases containing silicon (Si), chlorine (Cl), and hydrogen (H) are subjected to thermal energy (heat). As the molecules and atoms in the gases become heated, their bonds are broken and they recombine to form byproducts. This occurs both in the heated process chamber and downstream in the exhaust plumbing where the temperature drops. One big safety concern is that the byproducts of recombined silicon, chlorine, and hydrogen can ignite within minutes after exposure to air. When high densities of these byproducts are present, explosions can occur.

Chlorosilane processes such as Dichlorosilane (DCS - SiH_2Cl_2) and Trichlorosilane (TCS - SiHCl_3) form SiCl_2 based (chlorosilane) polymers. These polymers are a viscous liquid. If a chlorosilane polymer is exposed to air, the surface of the viscous liquid reacts with moisture (H_2O) and forms a silicon dioxide (SiO_2) layer or outer crust, with viscous liquid (polysiloxanes from polychlorosilanes) underneath. This siloxane polymer can occur within 10 minutes of exposure to air. Depending on the extent of exposure, there may be some chlorine remaining in the polymer. Exposure to air can occur due to a leak in the exhaust plumbing and hardware, or disassembly for maintenance. Figure 1 shows an example of this polymer deposit that forms in the exhaust system.



Figure 1- Chlorosilane polymer build-up in exhaust system from an epitaxial deposition system.

Silicon and silicon compounds deposit in the lines as highly excited atoms in a transient state (metastable intermediates) reactive to air (oxygen, water vapor), water or physical shock. Examples of physical shock are friction caused by a pressurized gas stream, sudden movement, or the vibration of a piece of hardware. The amount and reactivity of exhaust byproducts varies from system to system and process to process, depending on temperature, pressure, and the source gases. Oxygen and water (H₂O) moisture in the air react with the deposits. Partially reacted deposits are dangerous. When they continue their reaction, they can ignite in flames (e.g., a "pop" or "flash") and when confined, can explode. Partially reacted deposits can ignite in 3-5 minutes after exposure to air. Partially reacted deposits will also ignite when exposed to friction (e.g., a sudden inrush of air), heat (e.g., heated gas flows), or mechanical shock (e.g., banging on an exhaust line). Once the deposits are fully reacted, they are no longer pyrophoric. The remaining material is basically sand (SiO₂). We show examples of the reacted deposits in Figure 2.



Figure 2- Examples of fully reacted amorphous silicon dust visible in the portions of the exhaust plumbing during a cleaning process.

Why does this happen? The primary reason is that the epitaxial deposition process is very inefficient. During silicon deposition only 1% of the gas typically binds to the surface of the wafer. The other 99% is exhausted, releasing unbound silicon throughout the exhaust plumbing. This residual silicon deposits on pipe walls; binds to other ions, atoms and radicals in the gas stream; or flows to an abatement device.

Finally, it is important to understand what conditions might typically cause the byproducts to react. This list shows the more common conditions:

- During maintenance activities, when exhaust plumbing, chamber, or scrubber is disassembled and the deposits are exposed to air.
- After restarting the system or chamber, the deposits can be exposed by an inrush of air caused by the pump. This occurs following maintenance.
- When an EMO (Emergency Off) button is pressed.
- The system has been powered down. Examples: relocation, idle, power failure.
- Cleaning using concentrated acid or alcohols. Examples: IPA, Hydrofluoric acid (HF).
- Cleaning using pressurized gas, like spraying N₂ or pressurized water.
- When a leak has introduced air to the exhaust line, a pump, or an abatement device. Examples: load lock, poorly connected seals, or thermocouple sheath.
- Occasionally during wafer processing. Usually, nothing remains to determine root cause.

In summary, exhaust byproducts deposited during epitaxial deposition can pose not only a maintenance issue, but also a safety hazard. As such, these exhaust byproducts must be periodically removed from the chamber and the exhaust system and plumbing. Furthermore, certain common conditions can cause a reaction to occur, so careful cleaning and maintenance procedures are necessary.



Ask The Experts

Q: When do customers prefer to use a die attach film and when do they prefer to use B-Stage for attaching the die to the package substrate?

A: Die attach film is straightforward to use, but has limitations in terms of the amount of waste that is generated from the excess film that remains after the die attach process is complete. Die attach film also typically comes in a single thickness. B-Stage can be applied with varying thicknesses, making it more flexible than die attach epoxies or films. B-Stage generates less waste, but the process is more challenging to control. There are two different temperatures for B-stage curing processes. The A-stage curing process occurs at a lower temperature, while the B-stage curing process occurs at a higher temperature. The glass transition temperatures of B-stage compounds are typically in the 35-50°C range, and the B-stage curing conditions are in the 125°C range, making them only suitable for lower temperature processes. Furthermore, there is the added challenge of dealing with a liquid on the backside of a wafer. B-stage is best done at the wafer-level, since it is applied as a liquid film.

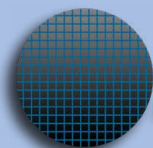
Learn from our Subject Matter Experts

A photograph of a person wearing a denim shirt, sitting at a desk and working on a laptop. The person's hands are visible, and they appear to be focused on their work. The background is blurred, showing what looks like a computer monitor and other office equipment. The entire image has a blue tint.

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Course Spotlight: DEFECT-BASED TESTING

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's application-specific ICs and microprocessors can contain upwards of 100 million transistors. Traditional testing relies on the stuck-at-fault (SAF) to model defect behavior. Unfortunately, the SAF model is a poor model for defects. Other models and strategies are required to catch killer defects on integrated circuits. As transistor sizes decrease, the types and properties of the killer defects change. This has created a number of challenges related to the testing of components. Defect-Based Testing is a 2-day course that offers detailed instruction on the electrical behavior and test strategies for integrated circuits. We place special emphasis on electrical behavior, fault models, and test techniques. This course is a must for every manager, engineer, and technician working in IC test, IC design, or supplying test hardware and software tools to the industry.

By focusing on the fundamentals of circuit behavior and the impact of defects on circuit behavior, participants will learn how to design, write, and implement test strategies to catch defects. Our instructors work hard to explain semiconductor test without delving heavily into the complex algorithms and computer science that normally accompany this discipline.

Participants will learn basic, but powerful, aspects about defect-based testing. This skill-building series is divided into four segments:

1. **Electrical Behavior of Defects.** Participants will study the electrical behavior of defects. They will learn how open circuits, resistive vias, shorts, and transistor variations affect the electrical behavior of the individual transistor, as well as gate elements and larger blocks.
2. **Fault Models for Defect-Based Testing.** Participants will learn about the historical underpinnings of the stuck-at-fault (SAF) model. They will also learn about other testing models, including IDDQ testing, at-speed testing, and delay testing.
3. **Production Test Methods.** Participants will learn about standard digital testing, SAF testing, IDDQ, timing, low voltage tests, and other types of stress tests. They will explore the strengths and weaknesses of each test type.
4. **The Economic and Quality Impact of Defect-Based Testing.** Participants will learn how defect-based testing can actually improve test economics. They will also study the impact on quality and reliability.

COURSE OBJECTIVES

1. This course will provide participants with an in-depth understanding of defect-based testing and its technical issues.
2. Participants will understand the basic concepts of test economics, yield, test time, and the cost of test. They will also learn how defect-based testing can reduce the possibility of failures in the field.
3. This course will identify underused test techniques like IDDQ and Very Low Voltage (VLV) test techniques that can successfully find defects that are difficult to catch using conventional test techniques.
4. This course will offer the opportunity to discuss specific test problems with our expert instructors.
5. Participants will be able to identify basic and advanced principles for defect-based test.
6. Participants will understand the difficulties in extending IDDQ testing to leading edge products, and how to overcome some of these limitations.
7. Participants will become familiar with Design for Test (DFT) and Automatic Test Pattern Generation (ATPG) tools used for defect-based testing.
8. This course will introduce fundamental and advanced concepts related to extending defect-based testing to future designs.
9. Participants will learn what tools are available today to implement defect-based testing.

COURSE OUTLINE

DAY 1

1. What is Defect-Based Testing?
 - a. Introduction
 - b. Terminology
 - c. Existing test techniques
2. CMOS IC Defect Mechanisms and Detection Techniques
 - a. Normal transistor and gate behavior
 - b. Sources of random and systematic defects
 - c. Types of Defects and How to Detect Them
 - i. Bridging defects
 - ii. Resistive defects
 - iii. Open circuit defects
 - iv. Delay defects
3. Fault Models for Defect-Based Test
 - a. Stuck-at-fault (SAF)
 - b. Delay fault

DAY 2

- c. Leakage fault
 - d. Methods for implementing fault models
 - e. Existing software tools
4. Production Test Methods
 - a. Functional testing (At-speed testing)
 - b. IDD_x Testing
 - c. Timing Test
 - d. Low Voltage Testing
 - e. Stress Testing
5. Defect-Oriented test Economics and Product Quality
 - a. Test set reduction
 - b. Effectiveness in catching defects
 - c. Yield and fallout
6. Case Histories

Upcoming Courses:

Webinar Schedule:

[IC Packaging Technology Webinar](#) - August 26-29, 2024 (Mon.-Thurs.) | Online at 8:00 AM-12:00 Noon Pacific Time - \$600

Public Course Schedule:

[Advanced CMOS/FinFET Fabrication](#) - September 2-3, 2024 (Mon.-Tues.) | Singapore - \$1,195 until Mon. Aug. 12

[Packaging Failure and Yield Analysis](#) - September 9-10, 2024 (Mon.-Tues.) | Penang, Malaysia - \$1,195 until Mon. Aug. 19

[Packaging Failure and Yield Analysis](#) - September 23-24, 2024 (Mon.-Tues.) | Manila, Philippines - \$1,195 until Mon. Sept. 2

[Defect-Based Testing](#) - November 18-19, 2024 (Mon.-Tues.) | Munich, Germany - \$1,195 until Mon. Oct. 28

[Wafer Fab Processing](#) - November 25-28, 2024 (Mon.-Thurs.) | Munich, Germany - \$2,095 until Mon. Nov. 4

[Failure and Yield Analysis](#) - December 2-5, 2024 (Mon.-Thurs.) | Munich, Germany - \$2,095 until Mon. Nov. 11

[Semiconductor Reliability and Product Qualification](#) - December 9-12, 2024 (Mon.-Thurs.) | Munich, Germany - \$2,095 until Mon. Nov. 18

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!