Issue 62 August 2014

InfoTracks

Semitracks Monthly Newsletter

Thermal Processing

By Christopher Henderson

In this month's newsletter, we'll be discussing Thermal Processing. There are four main thermal processes: thermal oxidation, thermal annealing, thermal diffusion, and thermal nitridation. With thermal oxidation, engineers react silicon with oxygen to grow a thin film of high quality thermal oxide. This is one of two common methods for creating silicon dioxide; the other is the use of chemical vapor deposition to deposit the layer. With thermal annealing, engineers use heat to activate dopants and repair silicon lattice damage from ion implantation. They also use annealing to form silicide layers, like titanium, cobalt, or nickel silicides by reacting the metal with the silicon surface. They also can use annealing to densify oxides like those deposited by chemical vapor deposition. With thermal diffusion, engineers can redistribute implanted dopants in the silicon. And finally, with thermal nitridation, engineers can react silicon with oxygen and a nitrogen-containing gas like nitrous oxide or nitric oxide to grow a nitrided dielectric like silicon oxynitride.

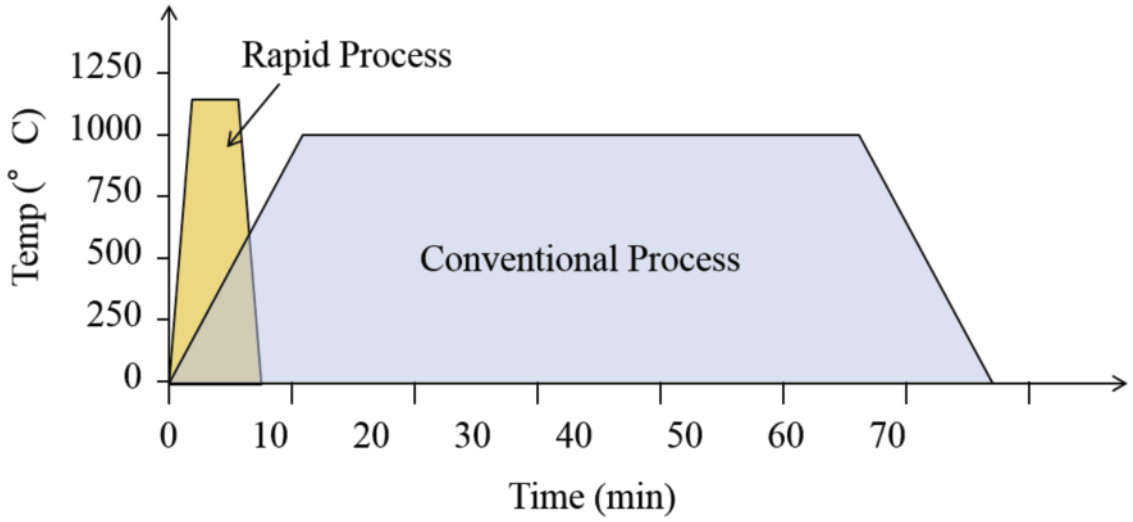
Other thermal processes include chemical predeposition and chemical vapor deposition. Historically, engineers used chemical predeposition as a method of doping prior to the development of ion implantation. One would deposit a dopant-containing material, known as a precursor, on a heated wafer surface. Precursors can be solids, liquids, or gases. Engineers control the amount of dopant introduced into the Si by two factors: the solid solubility of the dopant and the diffusivity of the dopant. Both factors are a strong function

In this Issue:

SEMITRACKS, INC.
Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

of temperature. Although chemical predeposition is no longer used in mainstream integrated circuit processing, it is still used in some specialized applications like compound semiconductor processing and new applications like silicon nanoparticle formation. Another more common thermal process is Chemical Vapor Deposition, or CVD. It is not a conventional thermal process, but it does occur at relatively high temperatures. We discuss CVD in more detail elsewhere in this system.

Let's make a few comments on thermal budgets. This is the upper limit to the amount of heat and time the process can endure without creating harmful side effects. One of the biggest problems with thermal processing is that it not only moves atoms that one wants to move, but it also moves atoms one would prefer not to move. For example, a silicide step that uses high temperatures might cause the source-drain implants to move further. This means that engineers need to be careful about how they construct the process in order to limit these effects. This phenomenon led scientists to come up with the term "thermal budget." We measure the total amount of thermal energy received by the wafer during thermal processing, and then work to stay below this number. As process nodes shrink, the thermal budget also shrinks, making this task quite difficult today. It is something all scientists and engineers need to characterize and study for their processes.



One of the more important thermal processes is thermal oxidation. Engineers use silicon dioxide, both thermal and CVD, for several uses. The first one is as a surface dielectric. We use surface dielectrics to isolate devices from one another like transistors, capacitors, and interconnect. Device manufacturers sometimes isolate transistors using LOCOS (pronounced "low-cos") field oxide. They also isolate inter-metal dielectric, or IMD, with oxide as well, although this oxide is normally a deposited oxide.

The second use is as a device dielectric. Process engineers use this dielectric within a device to actively control the device operation. For example the gate oxide controls the MOS (pronounced "M-O-S") transistor threshold voltage and drive current, and the capacitor oxide controls capacitance, like one might use for DRAM (pronounced "D-ram") cells.

The third use is as a mask. Engineers do this for ion implantation, where the oxide protects underlying film from being doped, and for etching, where the oxide protects the underlying film from being etched, like a sidewall spacer oxide.

The fourth process application for an oxide layer is the etch stop. This allows complete etching of an

uncovered area while preventing etching of the underlying film in the covered area.

The fifth application is surface passivation. A surface passivation reduces the reactivity of silicon surface and protects against contamination. This is a common final layer on semiconductor devices to provide protection in the package.

The sixth and final application is as a buffer layer. A buffer layer prevents film peeling when two films have very different coefficients of thermal expansion. A common use of the buffer layer is the pad oxide between the silicon nitride mask layer and the silicon surface. This pad oxide helps prevent damage to the silicon during subsequent thermal processing, which leads to stacking faults and other crystalline damage in the silicon.

Application	SiO2 Thickness (nm)
Gate oxide insulators for MOS devices	1.5 – 10.0
Tunnel oxides in EEPROMS and Flash memories	6.0 – 10.0
Screen oxides for ion implantation	10.0 – 20.0
Sidewall liners for shallow trench isolation (STI)	15.0 – 40.0
Field oxide for LOCOS isolation	200 – 400
Re-oxidation of the etched gate stack sidewall damage	5.0 – 7.5
Inter-polysilicon dielectric	4.0 – 20.0
Masking film against ion implantation and diffusion	100 – 200
Sacrificial oxides for gate applications	6.0 – 15.0
Capacitor dielectric in DRAM circuits	5.0 – 10.0

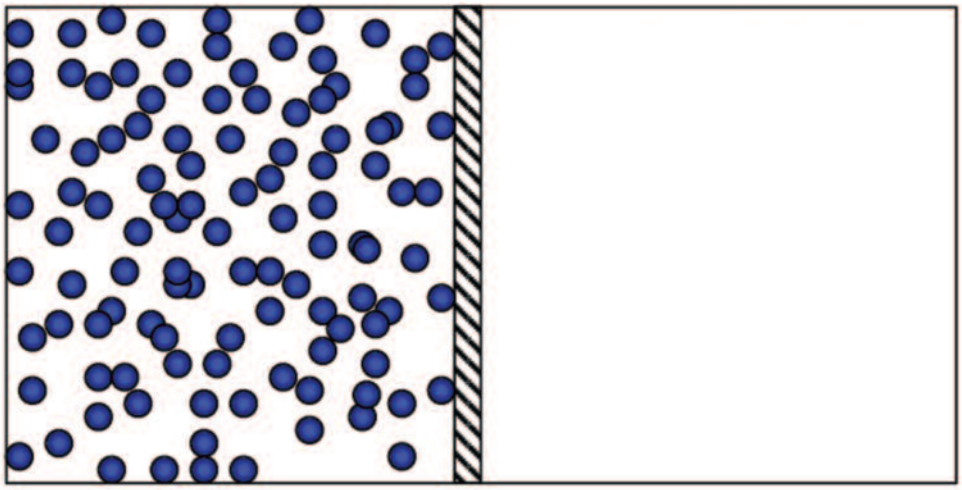
Ranges of thermal oxide thickness used in VLSI processing

This table summarizes some of the more important process applications for silicon dioxide. As you can see, silicon dioxide can be used for a wide range of applications within a semiconductor device, ranging from gate oxides, to re-oxidation steps, to sacrificial layers to enable defect-free processes subsequent to the step.

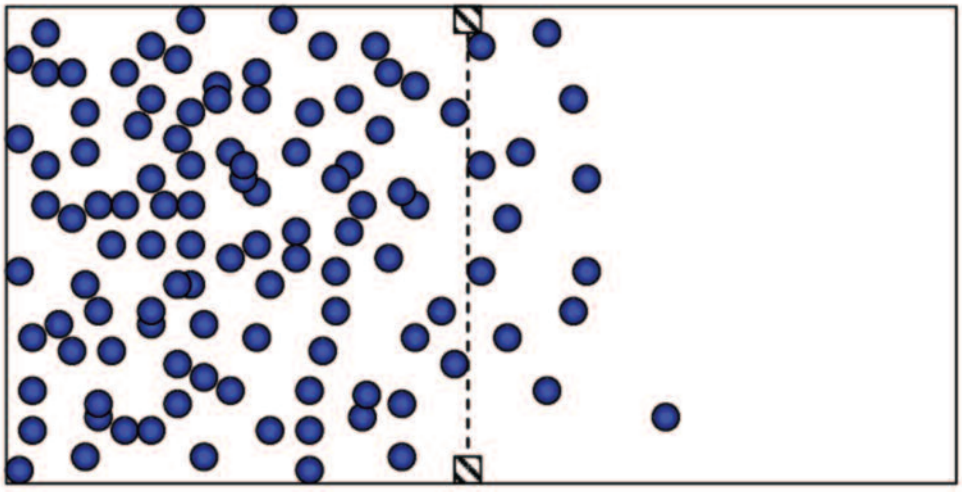
Technical Tidbit

Diffusion

Most of us usually learn about diffusion in college in terms of their mathematical equations. However, visualizing diffusion can make it much easier to understand. This series of images can help us visualize the concept. Let's assume we have a hypothetical situation where we have a number of charge carriers in a box like we show here.



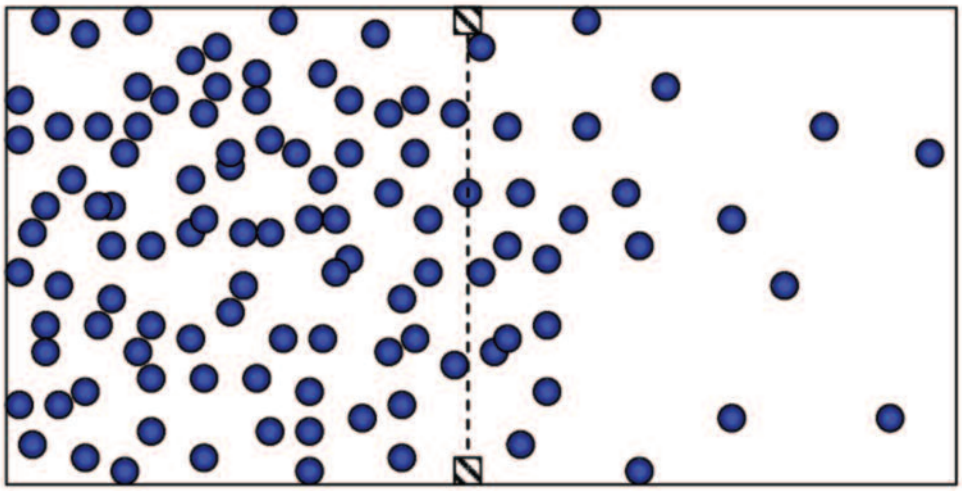
These carriers will move around within the box, and the speed of their movement will be governed by the temperature of the system. The lower the temperature, the slower the carriers move; the higher the temperature, the faster the carriers move. Notice that we have a lot of carriers on the left, and no carriers on the right.



Now, let's remove the wall. Since the carriers move randomly, about half are moving to the left and half are moving to the right at any given point in time. Those near the boundary can now move across the boundary. Because the barrier is now missing, there is a net movement to the right, because those right

on the boundary have a 50% chance of moving to the right, and a 50% chance of moving back to the left. Fick's Laws are the equations that govern this motion.

In general then, we have this random motion that results in a definite and predictable motion of the entire population of the carriers, and we call this Gaussian or Fickian diffusion. Like the movement of carriers, diffusion slows down with temperature, and with state changes from liquid to solid, but it still



occurs, even at very low temperatures. Not only does this occur in semiconductor materials, but it is also associated with other mechanisms, like intermetallic growth. For instance, Kirkendall voiding with intermetallic growth as an example of this, since diffusion of gold into aluminum occurs more quickly than diffusion of aluminum into gold.

Ask the Experts

Q: What is the p-value term in an ANOVA (Analysis of Variance) calculation?

A: The P value tests the null hypothesis that data from all groups are drawn from populations with identical means. Therefore, the P value answers this question:

If all the populations really have the same mean, what is the chance that random sampling would result in means as far apart as observed in this experiment?

If the overall P value is large, the data do not give you any reason to conclude that the means differ. Even if the population means were equal, you would not be surprised to find sample means this far apart just by chance. This is not the same as saying that the true means are the same. You just don't have compelling evidence that they differ. If the overall P value is small, then it is unlikely that the differences you observed are due to random sampling. You can reject the idea that all the populations have identical means. This doesn't mean that every mean differs from every other mean, only that at least one differs from the rest.

Spotlight: EOS, ESD, and How to Differentiate

OVERVIEW

Electrical Overstress (EOS) and Electrostatic Discharge (ESD) account for most of the field failures observed in the electronics industry. Although EOS and ESD damage can at times look quite similar to each other, the source each and the solution can be quite different. Therefore, it is important to be able to distinguish between the two mechanisms. The semiconductor industry needs knowledgeable engineers and scientists to understand these issues. ***EOS, ESD, and How to Differentiate*** is a two-day course that offers detailed instruction on EOS, ESD and how to distinguish between them. This course is designed for every manager, engineer, and technician concerned with EOS, ESD, analyzing field returns, determining impact, and developing mitigation techniques.

Participants learn to develop the skills to determine what constitutes a good ESD design, how to recognize devices that can reduce ESD susceptibility, and how to design new ESD structures for a variety of technologies.

1. **Overview of the EOS Failure Mechanism.** Participants learn the fundamentals of EOS, the physics behind overstress conditions, test equipment, sources of EOS, and the results of failure.
2. **Overview of the ESD Failure Mechanism.** Participants learn the fundamentals of ESD, the physics behind overstress conditions, test equipment, test protocols, and the results of failure.
3. **ESD Circuit Design Issues.** Participants learn how designers develop circuits to protect against ESD damage. This includes MOSFETs, diodes, off-chip driver circuits, receiver circuits, and power clamps.
4. **How to Differentiate.** Participants learn how to tell the difference between EOS and ESD. They learn how to simulate damage and interpret pulse widths, amplitudes and polarity.
5. **Resolving EOS/ESD on the Manufacturing Floor.** Participants see a number of common problems and their origins.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of electrical overstress, the models used for EOS, and the manifestation of the mechanism.
2. Participants will understand the ESD failure mechanism, test structures, equipment, and testing methods used to achieve robust ESD resistance in today's components.
3. The seminar will identify the major issues associated with ESD, and explain how they occur, how they are modeled, and how they are mitigated.
4. Participants will be able to identify basic ESD structures and how they are used to help reduce ESD susceptibility on semiconductor devices.
5. Participants will be able to distinguish between EOS and ESD when performing a failure analysis.
6. Participants will be able to estimate a pulse width, pulse amplitude, and determine the polarity of an EOS or ESD event.
7. Participants will see examples of common problems that result in EOS and ESD in the manufacturing environment.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, written text material, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The course notes offer dozens of pages of additional reference material the participants can use back at their daily activities.

COURSE OUTLINE

Day 1

1. Introduction
   a. Terms and Definitions
   b. ESD Fundamentals
   c. EOS Fundamentals
2. Electrical Overstress Device Physics
   a. Sources of EOS
   b. EOS Models
   c. Electrothermal Physics
3. Electrostatic Discharge Device Physics
   a. ESD Models
   b. ESD Testing and Qualification
   c. ESD Failure Criteria
   d. Electrothermal Physics
   e. Electrostatic Discharge Failure Models
   f. Semiconductor Devices and ESD Models
   g. Latchup
4. EOS Issues in Manufacturing
   a. Charging Associated with Equipment
      i. Testers
      ii. Automated Handling Equipment
      iii. Soldering Irons
   b. Charge Board Events
   c. Cable Discharge Events
   d. Ground Loops/Faulty Wiring
   e. Voltage Differentials due to High Current
   f. Event Detection

Day 2

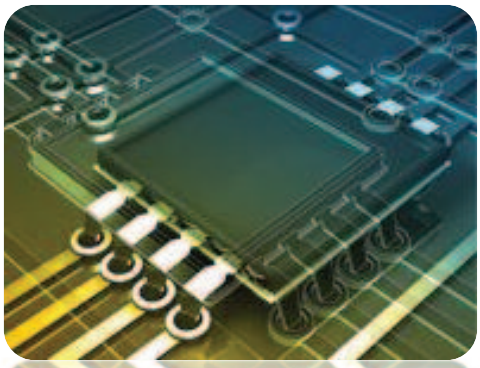
5. ESD Protection Methods
   a. Semiconductor Process Methods
   b. MOSFET Design
   c. Diode Design
   d. Off-Chip Drivers
   e. Receiver Networks
   f. Power Clamps
6. Differentiating Between EOS and ESD
   a. EOS Manifestation
   b. ESD Manifestation
   c. Circuit considerations
      i. Chip level
      ii. System level
   d. Simulating ESD
   e. Simulating EOS
7. EOS/ESD Design and Modeling Tools
   a. Electrothermal Circuit Design
   b. Electrothermal Device Design
   c. ESD CAD Design

Semitracks is planning to exhibit at this year's International Symposium for Testing and Failure Analysis. Please stop by and see us. Please call us at 1-505-858-0454 or email us at info@semitracks.com to schedule.

40th Annual International Symposium for Testing and Failure Analysis

Conference and Exposition

November 9 – 13 • Houston, Texas
Stop by and see us!
For more information on the symposium, visit
http://www2.asminternational.org/content/Events/istfa
Please feel free to contact us to set up an appointment while you are there!



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

~

For more information on Semitracks online training or public courses, visit our web site!

http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Semiconductor Reliability
September 3 – 5, 2014 (Wed – Fri)
San Jose, California, USA

Failure and Yield Analysis
September 8 – 11, 2014 (Mon – Thur)
San Jose, California, USA

Product Qualification
January 26 – 27, 2015 (Mon – Tue)
San Jose, California, USA

Wafer Fab Processing
January 26 – 29, 2015 (Mon – Thur)
San Jose, California, USA

EOS, ESD and How to Differentiate
January 28 – 29, 2015 (Wed – Thur)
San Jose, California, USA