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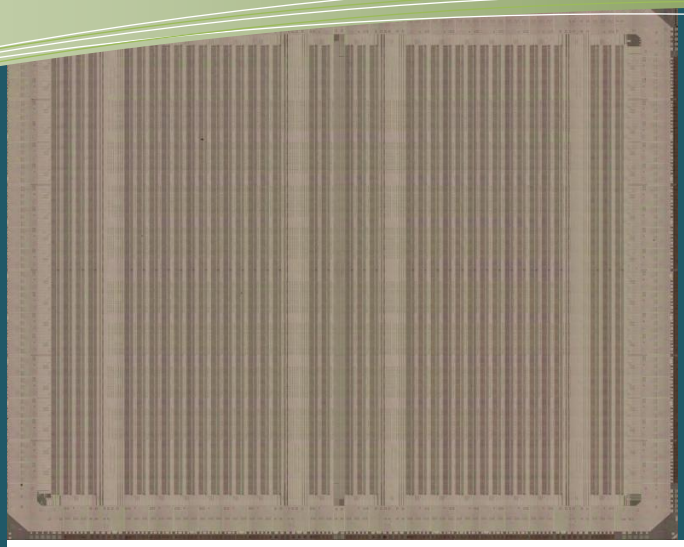
SEMITRACKS MONTHLY NEWSLETTER

INFOTRACKS



[inside this issue]

Upcoming Courses

Semitracks offers live seminars in Europe, North America, and Asia, and our online classes can be accessed anywhere in the world. Click on any course title to find out more.

Failure and Yield Analysis

September 8-11, 2009
Munich, Germany

Semiconductor Reliability

September 14-16, 2009
Munich, Germany

MEMS Technology

October 5-6, 2009
Austin, TX, USA

Photovoltaics Overview

October 7, 2009
Austin, TX, USA

Photovoltaics Technology and Manufacturing

October 8, 2009
Austin, TX, USA

Wafer Fab Processing

October 19-22, 2009
Enschede, Netherlands

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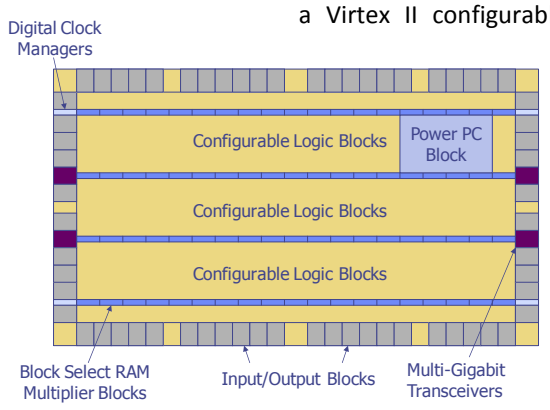
For information about online courses, click here.

What's Inside an FPGA?

[By Chris Henderson]

Increasingly, Field Programmable Gate Arrays (FPGAs) are replacing custom ASICs. Today's FPGAs can incorporate large amounts of logic, memory, and other specific functions, such as processor cores, high speed signaling, and standard interface protocols. The image at the head of this article shows the chip layout for the Xilinx Vertex II, a common FPGA. We will use this FPGA to discuss some of the basic features of these powerful chips.

Opposite is the basic block layout for the Xilinx Virtex II Pro FPGA. The majority of the die is populated with configurable logic blocks for implementing functionality. Some blocks, like the IBM Power PC 405 series core, can be reserved for drop-in processing elements. The channels between the logic blocks are configured as block select RAM multipliers; these blocks can perform 18-bit by 18-bit multiplication operations. On the periphery, the blocks can be configured with digital clock managers, multi-gigabit serial transceivers, and highly versatile input-output blocks. The digital clock managers can reduce clock skew problems across the chip, generate a wide range of clock frequencies, perform clock multiplication or division, and provide phase shifting. The multi-gigabit serial transceivers provide high frequency serial communications on and off the FPGA. Finally, the input/output logic blocks provide for a multitude of voltage and drive levels, as well as newer concepts like low voltage differential signaling.



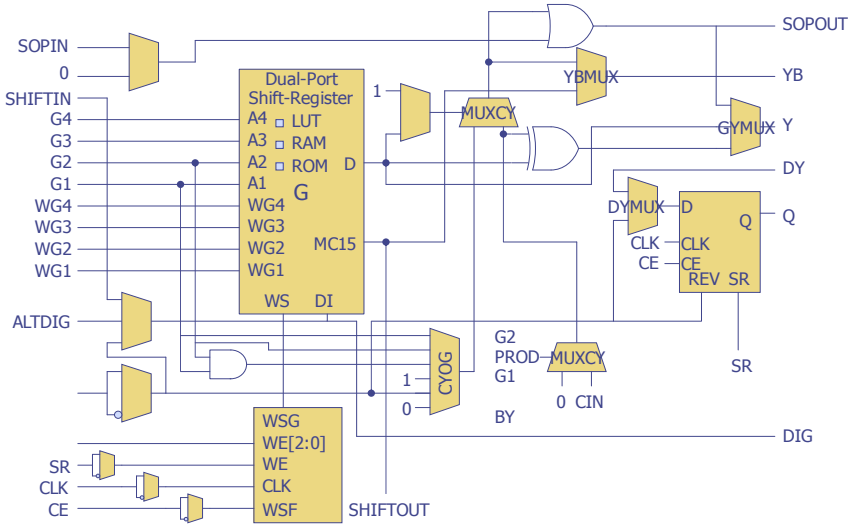
The basic block layout for the Xilinx Virtex II Pro FPGA

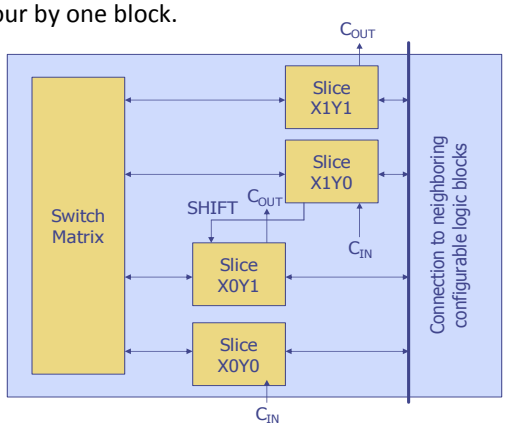
As shown in the diagram on the following page, a Virtex II configurable logic block contains four similar slices that are split into two columns of two slices each. Each column contains two independent carry logic chains and one common shift chain. Every slice is tied to a switch matrix that allows access from the general routing matrix. Each slice has an upper half and a lower half. Each half contains a dual port shift register that can be configured as a lookup table, 16 bits of random access memory, or a 16-bit variable tap shift register element. Each half also contains a register/latch function to implement sequential logic and the logic to permit integration of the two halves.

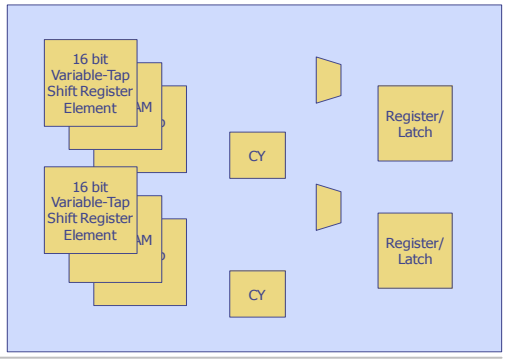
The Xilinx Virtex II cell architecture, shown in detail below, represents an advanced FPGA cell design. In the case of the Virtex II, a complementary

slice is not shown. The basic function generator is implemented as a four-input lookup table, labeled here as block G. This results in a propagation delay that is independent of the function that one implements. The function can exit the cell block through the GYMUX, go to the dedicated exclusive or gate, input the carry logic multiplexer, feed the d input on the register, or feed the logic from the bottom slice to implement more complex logical functions. The register can be configured either as an edge-triggered d flip flop or as a level sensitive latch.

Each slice has clock, clock enable, set, and reset signals to provide additional control. The set function can be configured to be either synchronous or asynchronous. The dual port shift register can also be configured as memory. One can implement a sixteen by one bit synchronous random access memory resource. Since two slices can work in tandem, one can create a variety of memory blocks ranging from single port sixteen by eight blocks to a dual port sixty-four by one block.







Above: Detailed architecture of the Xilinx Virtex II Pro.
Top Right: Figure showing the top-level architecture of a configurable logic block.
Bottom Right: Figure showing the logic elements contained within each configurable logic block.

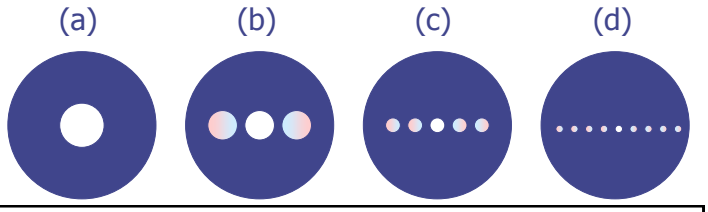
Technical Tidbit

[Diffraction in Optical Microscopy]

Arguably the most powerful tool for failure analysis, the optical microscope can detect many types of defects, including masking problems, process problems, contamination, electrical damage, and packaging problems. However, when light passes through or close to an object, the light can be diffracted. Diffraction, one of the most important concepts in optical microscopy, can cause constructive and destructive interference, changing the nature of the gathered image.

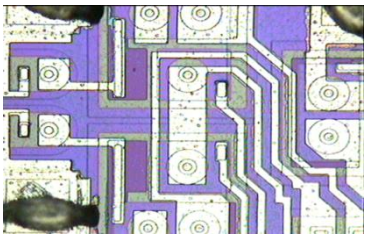
The top diagram shows how diffraction can affect an image. When just the condenser aperture is in place, a white spot is produced. If a 10X objective is placed in the path, two diffraction spectra appear; a 40X objective in place produces four diffraction spectra; and a 60X objective in place produces eight diffraction spectra. With white light, the individual diffraction spectra exhibit a reddish color at one side of the spot and a bluish color at the other side of the spot. The details of a specimen are best covered if both the zeroth order and at least the first order diffraction spectra are captured by the objective.

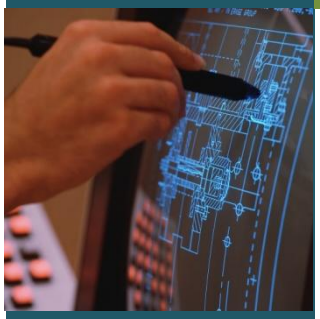
One aspect of diffraction relevant to failure analysis is the color of the oxide. In bright field imaging, the standard viewing mode on most optical microscopes, the image is a product of the differences in reflectivity of the material properties and the constructive and destructive interference of the reflected light itself. The light diffraction produces the colors seen in this image. The color of the oxide can be used to determine the thickness of the oxide by comparing the oxide color to a table called the Pleskin chart, which relates thickness to a particular color.



Above: Line grating diffraction patterns. (a.) Condenser aperture diagram—empty stage, (b.) diffraction spectra from a 10x objective (line grating on microscope stage), (c.) diffraction spectra from a 40x objective, and (d.) diffraction spectra from a 60x objective.

Below: A bright field optical microscope image.





What Our Customers Say:

"Well worth attending. Good course."

"Very pleased indeed with the course -- found it interesting and will find it useful."

"The course… was comprehensive and impressive in its content. Chris was extremely knowledgeable with a clear wealth of relevant experience."

"Extremely comprehensive and an opportunity to ask questions of a very experienced trainer."

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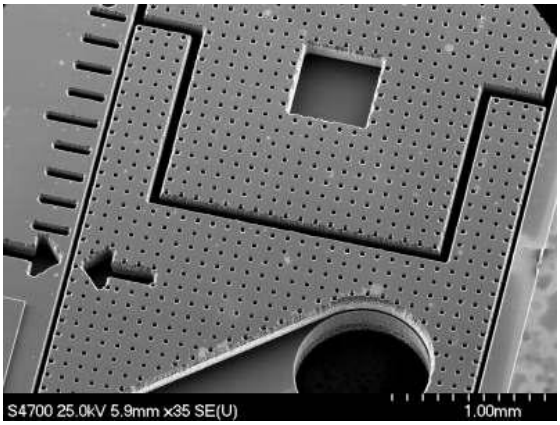
Course Spotlight

[MEMS Technology]

Airbag sensors. Digital Light Processing™ projectors. Inkjet printers. These examples are only a few of the applications for microelectromechanical systems (MEMS), which have quickly become the fastest growing segment of the semiconductor market. MEMS devices, also referred to as microsystems or micro-machines, promise to produce smaller, more reliable systems for a cheaper price—yet can the technology deliver on these promises?



Semitracks' latest two-day course, ***MEMS Technology***, focuses on the design, operation, packaging, reliability, and testing of MEMS devices, with an emphasis on packaging. The large surface area to volume ratio in MEMS devices creates unique challenges—for example, surface effects such as electrostatics and liquid wetting dominate volume effects such as inertia or thermal mass. Yet in spite of these poorly understood properties, MEMS retain the potential to revolutionize the semiconductor market.

Through the course material, participants will learn about:

- **Device Design & Processing.** The course will cover basic wafer processing steps, including deep reactive ion etching (DRIE), wet etching, patterning, chemical mechanical planarization (CMP), and more.

- **MEMS Packaging.** Participants will learn basic packaging concepts for MEMS devices while reviewing assembly and packaging procedures such as structural release, cleaning, encapsulation, and testing. Various challenges associated with packaging and testing these devices will be discussed.

- **MEMS Reliability.** The course will review MEMS reliability issues and associated analysis/simulation techniques. MEMS reliability requires a broad understanding of physics and mechanics in order to handle the challenges during research, development, and productization.

The goal of this course is to give you an overview of MEMS technology and its associated design, manufacture, package, reliability, analysis, and test issues. Follow this link for more detailed information about the course.

Questions & Answers

Q: *Is it possible for conductive die epoxy to become non-conductive? What conditions are necessary for the epoxy to be conductive? Is it conductive in X, Y and Z directions when the grain size of silver is connected in a specific direction?*

A: Conductive epoxy adhesives usually set up their conductivity in a planar manner. Silver additive is normally in a flake format and forms a set of platelets that provide a planar structure. Cure shrinkage of the base epoxy resin compresses the silver particles to make mechanical contact with each other.

As far as losing conductivity, it could result from (1) thermomechanical delamination, (2) poor or no initial curing, or (3) separation of silver through either (a) initial resin bleed or (b) incomplete pre-mixing.

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[Customer Feedback]

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