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Thermal Processing, Issues and Effects, Part 3

By Christopher Henderson

Let's summarize some of the more important second-order effects. For dry oxidation and ultrathin oxides, the Deal-Grove model will significantly underestimate the oxide thickness when it is less than 30 nanometers. Some process engineers will adjust tau to improve the fit, but that is a less than satisfactory answer. Another approach is to use a more sophisticated model. For example, the Massoud model adds an additional term to handle the thin oxide problem. Dopants affect the oxidation process as well. The presence of dopants in the silicon will enhance the oxidation rates. However, there are different mechanisms for different dopant species. For instance, boron mainly affects the diffusion limited growth regime. The pile up in the oxide weakens the oxide structure, enhancing the diffusion of the oxidizing species. Phosphorus mainly affects the oxidation rate limited regime. Researchers believe this may be related to the concentration of silicon vacancies at the surface.

Crystal orientation also affects the oxidation rate. The oxidation rate is higher for the <111> (pronounced "one-one-one") surface than the <100> (pronounced "one-zero-zero") surface. This mainly affects the oxidation rate limited regime, and researchers believe the effect is due to a higher density of exposed silicon atoms.

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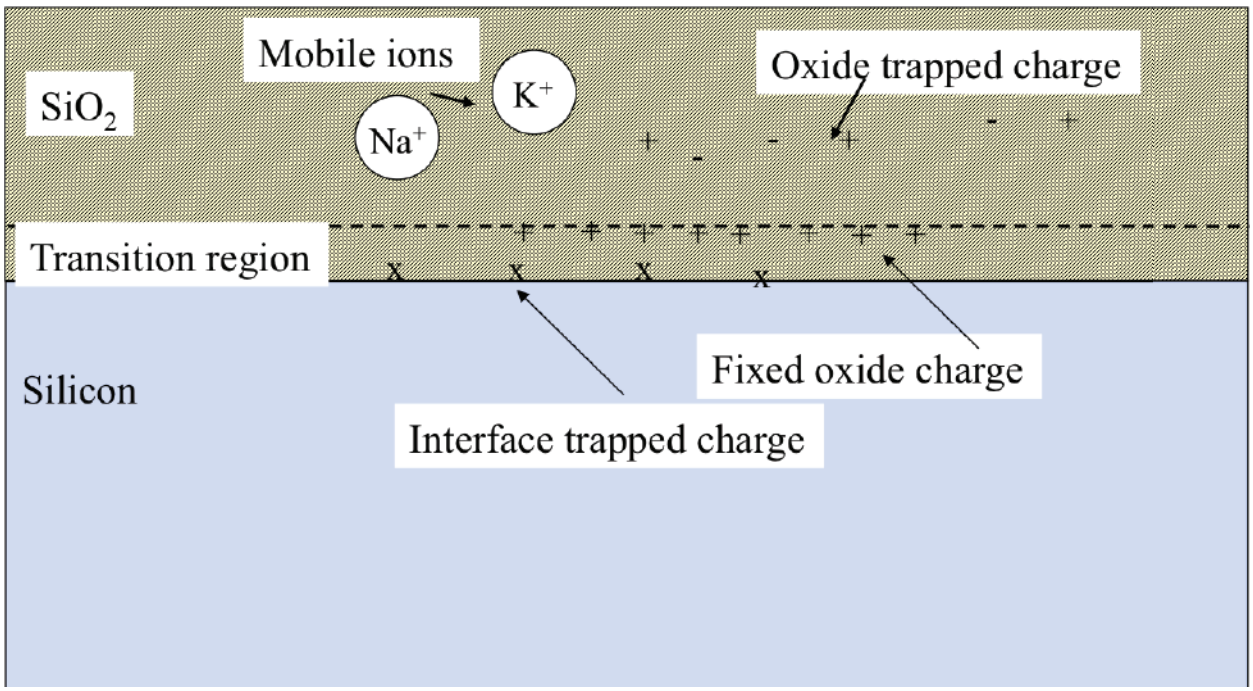
Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

There are four types of charge that can affect the behavior of a transistor or parasitic device. They are mobile ion charge, oxide trapped charge, fixed oxide charge, and interface trapped charge. Fixed oxide charge manifests itself as a sheet of positive charge located within 2 nanometers of the silicon-silicon dioxide interface. It is attributable to incompletely oxidized silicon atoms that have a net positive charge. The charge always remains positive. This charge can be an artifact of the termination of the oxide/annealing cycles, so the best method for reducing this effect is optimizing the oxidation/annealing cycles. Mobile ion charge, usually a positive ion like sodium or potassium in parts per million concentrations can cause measurable instabilities in transistors. It becomes mobile at higher temperatures and in the presence of an electric field. Even parts per million level concentrations can cause measurable instabilities. Process engineers reduce this problem through cleanliness in manufacturing and other methods like gettering and silicon nitride barriers.

Interface trapped charge is also due to incompletely oxidized silicon. The incompletely oxidized silicon produces a dangling bond. It tends to be very close to the interface. The charge may be positive or negative and may change during device operation. Engineers express this interface trapped charge as Dit (pronounced "D-sub-I-T"), or a density per unit energy. Oxide trapped charge occurs when silicon-oxygen bonds are broken due to ionizing radiation, or through exposure to energetic particles during processing, such as plasma etching or ion implantation. This can lead to electrons or holes trapped at defects in the bulk oxide. These bonds can normally be repaired by annealing.



This diagram shows the four different types of charge that can occur in the silicon dioxide and at the silicon/silicon dioxide interface. Mobile ions such as sodium and potassium can be found scattered throughout the silicon dioxide layer. In the presence of an electric field however, they can be attracted to

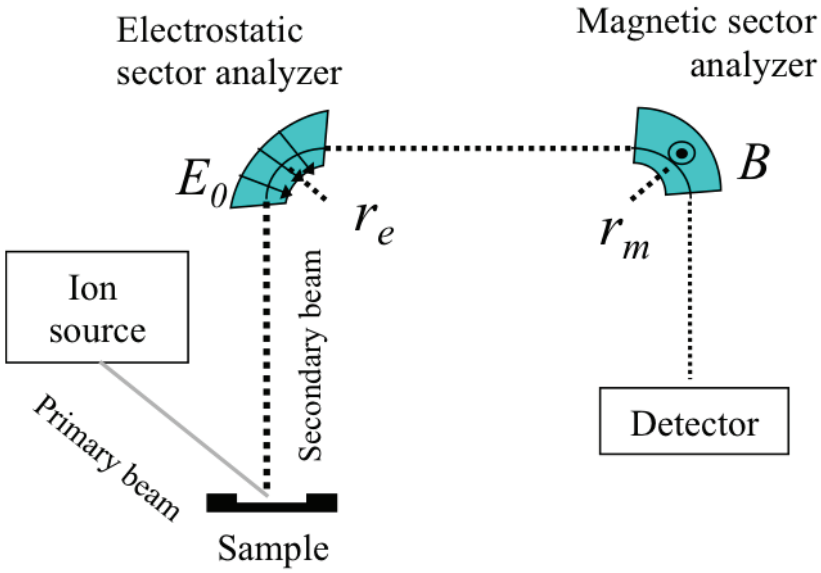
the interface. Oxide trapped charge is found randomly throughout the oxide. If there is an excess of either positive or negative fixed charge, it can affect device operation. Fixed oxide charge tends to occur in the transition region between the silicon and the silicon dioxide. Finally, interface trapped charge occurs right at the silicon/silicon dioxide interface.

In conclusion, we delved into thermal oxidation in more detail. We described the Deal-Grove model constants in more detail and discussed their impacts on the oxidation process. We also discussed second-order effects to the oxidation process. This includes items like dopants and dopant concentrations, the crystal orientation of the underlying silicon, the pressure of the gases used in the process, and any pre-treatment effects. While the Deal-Grove model provides good insight into the basic oxidation process, more accurate modeling that is required for today's nanometer scale devices requires that one understand and account for second-order effects. This means that more sophisticated models might be required.

Technical Tidbit

Mass Spectrometers for SIMS

A number of instruments in the semiconductor industry use mass spectrometers. Engineers and scientists use them for a range of activities, from monitoring gases to understanding the doping profile in a semiconductor material, a technique known as Secondary Ion Mass Spectroscopy (SIMS). Let's talk about one of the more common types of mass spectrometers used for SIMS in more detail.



Currently, the more common type of mass spectrometer used in SIMS is the sector field mass spectrometer. This uses an electrostatic sector analyzer coupled with a magnetic sector analyzer. This concept uses the Lorenz force to bend the ion through the electrostatic and magnetic sectors. The Lorenz force is equal to the Centripetal force, which is given by the equation below.

$$\text{Lorenz' force:} \quad \mathbf{F} = q\mathbf{E} + q(\mathbf{v} \times \mathbf{B})$$

$$\text{Centripetal force:} \quad \mathbf{F} = -\frac{mv^2}{r}\frac{\mathbf{r}}{r}$$

The mass-to-charge ratio can be calculated from the induced radius of curvature, or bend R sub E through the electrostatic analyzer, and the bend R sub M through the magnetic sector analyzer, as we show here.

Electrostatic sector analyzer

$$qE_0 = \frac{mv^2}{r_e}$$

Magnetic sector analyzer

$$qvB = \frac{mv^2}{r_m}$$

$$\frac{m}{q} = \frac{(r_m B)^2}{r_e E_0}$$

One can use an energy-resolving slit to filter out the unwanted ions from the analysis process, because the unwanted ions will be bent to a different degree. Other types of analyzers include the quadrupole mass analyzer, which separates masses by resonant electric fields, and the time-of-flight mass analyzer, which calculates mass based on the time required to traverse a known distance after a given acceleration.

Ask the Experts

Q: I heard the term flying probe tester recently. What does that mean exactly?

A: Flying probe testers is a term used to contrast against bed-of-nails testers. In a flying probe test system, an on-board computer places the needles or probes over the appropriate locations on a Printed Circuit Board to make electrical contact. This allows better utilization of the tester resources, since one only sets down on pads of interest. It also removes the need for fixturing. In a bed-of-nails tester, the probe points are fixed, so one would need a fixture to probe on a particular package type as an example.

Spotlight: Failure and Yield Analysis

OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Your industry needs competent analysts to help solve these problems. ***Advanced Failure and Yield Analysis*** is a four-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a ***Do It Right the First Time*** approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

Participants learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. **The Process of Failure and Yield Analysis.**Participants learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.
2. **The Tools and Techniques.** Participants learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools, light emission, electron beam tools, optical beam tools, decapping and sample preparation, and surface science tools.
3. **Case Histories.** Participants identify how to use their knowledge through the case histories. They learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.
2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.
3. The seminar will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.
4. The seminar offers a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic technology features on semiconductor devices.
6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

One unique feature of this workshop is the video segments used to help train the students. Failure and Yield Analysis is a visual discipline. The ability to identify nuances and subtleties in images is critical to locating and understanding the defect. Many tools output video images that must be interpreted by analysts. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

1. Introduction
2. Failure Analysis Principles/Procedures
    a. Philosophy of Failure Analysis
    b. Flowcharts
3. Gathering Information
4. Package Level Testing
    a. Optical Microscopy
    b. Acoustic Microscopy
    c. X-Ray Radiography
    d. Hermetic Seal Testing
    e. Residual Gas Analysis
5. Electrical Testing
    a. Basics of Circuit Operation
    b. Curve Tracer/Parameter Analyzer Operation
    c. Quiescent Power Supply Current
    d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
    e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
    f. Automatic Test Equipment
    g. Basics of Digital Circuit Troubleshooting
    h. Basics of Analog Circuit Troubleshooting
6. Decapsulation/Backside Sample Preparation
    a. Mechanical Delidding Techniques
    b. Chemical Delidding Techniques
    c. Backside Sample Preparation Techniques
7. Die Inspection
    a. Optical Microscopy
    b. Scanning Electron Microscopy

8. Photon Emission Microscopy
    a. Mechanisms for Photon Emission
    b. Instrumentation
    c. Frontside
    d. Backside
    e. Interpretation
9. Electron Beam Tools
    a. Voltage Contrast
        i. Passive Voltage Contrast
        ii. Static Voltage Contrast
        iii. Capacitive Coupled Voltage Contrast
        iv. Introduction to Electron Beam Probing
    b. Electron Beam Induced Current
    c. Resistive Contrast Imaging
    d. Charge-Induced Voltage Alteration
10. Optical Beam Tools
    a. Optical Beam Induced Current
    b. Light-Induced Voltage Alteration
    c. Thermally-Induced Voltage Alteration
    d. Seebeck Effect Imaging
    e. Electro-optical Probing
11. Thermal Detection Techniques
    a. Infrared Thermal Imaging
    b. Liquid Crystal Hot Spot Detection
    c. Fluorescent Microthermal Imaging
12. Chemical Unlayering
    a. Wet Chemical Etching
    b. Reactive Ion Etching
    c. Parallel Polishing
13. Analytical Techniques
    a. TEM
    b. SIMS
    c. Auger
    d. ESCA/XPS
14. Focused Ion Beam Technology
    a. Physics of Operation
    b. Instrumentation
    c. Examples
    d. Gas-Assisted Etching
    e. Insulator Deposition
    f. Electrical Circuit Effects
15. Case Histories

2015 IEEE International Reliability Physics Symposium

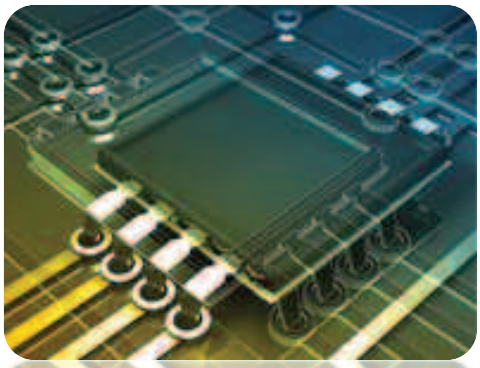
IEEE

April 19-23, 2015
Hyatt Regency Monterey Resort & Spa
Monterey, CA, USA

Registration is available at www.irps.org

Chris Henderson, IRPS Vice General Chair

Chris would be happy to meet with you and discuss any training needs you have. Contact him at henderson@semitracks.com during the symposium!



Upcoming Courses

(Click on each item for details)

Failure and Yield Analysis
April 27 – 30, 2015 (Mon – Thur)
Munich, Germany

Semiconductor Reliability
May 4 – 6, 2015 (Mon – Wed)
Munich, Germany

EOS, ESD and How to Differentiate
May 7 – 8, 2015 (Thur – Fri)
Munich, Germany

Product Qualification
May 18 – 19, 2015 (Mon – Tue)
San Jose, California, USA

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).
To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our web site!
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We look forward to hearing from you!