Issue 27 September 2011

InfoTracks

Semitracks Monthly Newsletter

New Semitracks Blog!

In order to keep our readers better up-to-date and informed, Semitracks Inc. has launched its new blog!

Read more, Page 3

Source and Drain Extensions

By Christopher Henderson

An Introduction to Source/Drain Extensions

In this article we will discuss the technology associated with source/drain regions on transistors, now commonly called source/drain extensions.

The choices for source/drain extensions are primarily based on the needs of the application. Different technologies require different features. For example, memory requires low leakage, long retention times, high density and low costs. Logic requires performance, and therefore higher drive currents. This needs to be balanced against a need for minimizing short channel effects, hot carrier effects, maintaining low resistances and capacitances, and minimizing leakage in low-power devices. Analog requires special attention to reducing the reverse short channel effect, the ability to match transistors to one another, and maintaining low leakage and noise.

Let's begin by discussing the lightly doped drain region or LDD. The LDD provides a region that is lighter doped than main source/drain implants. It helps to reduce the peak-field at the drain boundary, which in turn reduces impact ionization, substrate, and gate currents, and hot-carrier generation. It also reduces gate-induced drain leakage and drain-induced barrier lowering. There is also an improved control of the effective channel length. However, if the LDD is too lightly doped, it merely extends the channel and is ineffective in reducing the peak electric field. The peak field occurs near the light LDD and heavily doped drain boundary, or the N^-/N^+ junction. The optimal LDD extension concentration is in the 10^{18} – 10^{19} atoms per cubic centimeter range.

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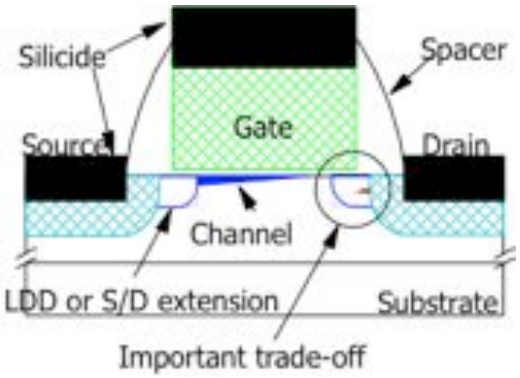


Fig. 1, Cross-section of transistor, showing source/drain regions and extensions.

Another common component of the source/drain region is the angled halo, or pocket implant. This is typically applied to the NMOS transistor. The angled implant locally raises the channel doping below surface next to the source/drain region, leaving most of channel region to be more lightly doped, reducing the variability and the field in the device. Halo implants improve short channel effects and raise the punchthrough voltage while minimizing the impact on the threshold voltage and the body effect where the gate control is weaker. The angled implant can be done before or after the spacer etch. The tilt angle ranges from 7° to 60°, depending on the application. For ultra-short channel transistors, halo implants will require a very low thermal budget, that one would normal achieve with a spike, or flash anneal.

Stay tuned for the conclusion of this article in October!

Ask the Experts

Q: What types of techniques can be used to highlight bond pad cratering?

A: One technique that can highlight bond pads for cratering using an optical microscope is nickel decoration. The aluminum bondpad is etched away, and the chip is placed in a nickel plating solution for several minutes. The nickel will first adhere to the cracks, providing contrast in the optical microscope.

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

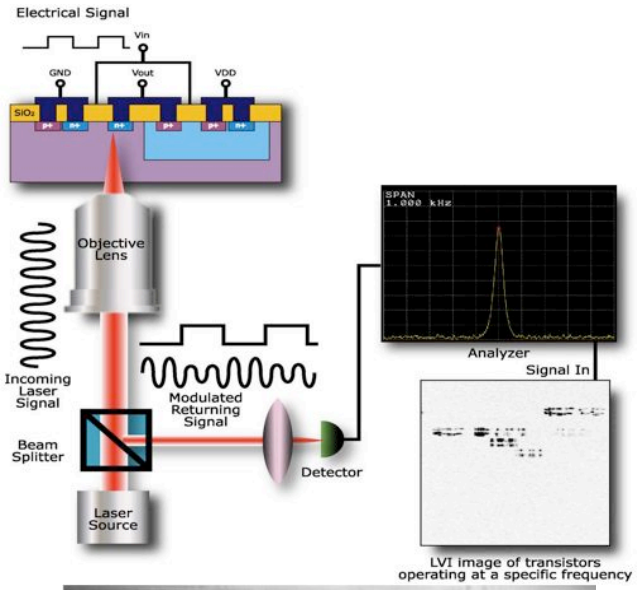
New Semitracks Blog!

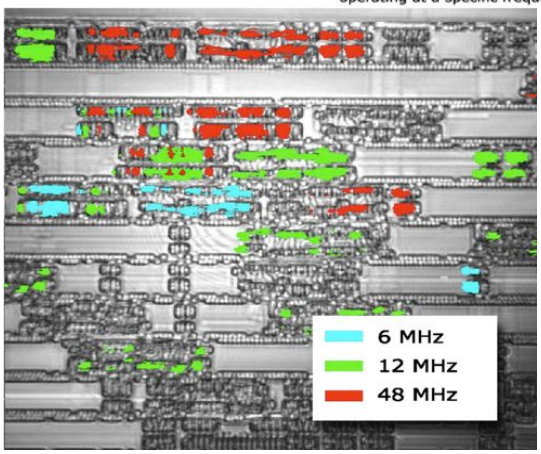
Semitracks has started a blog to keep you up to date on industry developments and items that affect Semiconductor Product Engineering and Reliability. In addition to industry developments, we'll include some short articles on technology items of interest. These may vary from historical items that help place current developments in context, to future developments that are likely to affect the industry. If you have comments or feedback, or topics you would like to see addressed, please feel free to e-mail us at info@semitracks.com.

See it for yourself at:
http://www.semitracks.com/index.php/en/blog

Technical Tidbit: Laser Voltage Imaging

Laser Voltage Imaging (LVI), shows the physical locations of transistors that are active at a specific frequency. LVI can be tuned to frequencies to be traced, and may also be used to show where to get the best signal strength for specific waveform measurements, and to the pixel where the "sweet spot" for probing is found. The Laser Scanning Microscope visually maps locations of transistors. By concentrating on a specific area of the DUT, one can scan for the dominant frequencies. LVI locates the transistors and thus maps circuits operating at those frequencies. LVI also enables signal tracing through circuitry, and even non-periodic signals can be monitored. This approach can also be used with Time-Resolved Light Emission.





Images courtesy DCG Systems, Inc.

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Upcoming Courses

Failure and Yield Analysis

October 3-6, 2011 – San Jose, CA

Semiconductor Reliability

October 11-13, 2011 – San Jose, CA

PV Technology & Manufacturing

October 20, 2011 – Dallas, TX

Failure and Yield Analysis

Oct 31 – Nov 3, 2011 – Singapore

Semiconductor Reliability

November 8-11, 2011 - Singapore

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or e-mail us at info@semitracks.com.

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by email at jeremy.henderson@semitracks.com.

We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our website!

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