Issue 13 July 2010

InfoTracks

Semitracks Monthly Newsletter

Learn to design for reliability.

The three-day Design for Reliability course on August 31-September 2, 2010 in San Jose covers fundamentals of reliability physics and accelerated testing, design-in reliability issues, and mission profiles involved in reliability-oriented designs.

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The Pros and Cons of E-Learning, Part 2

By Chris Henderson

Last month, we discussed several positive aspects of e-learning. However, not everyone's experience with online training is positive. In this issue, we'll discuss ways to combat students' problems with e-learning and improve their learning experience.

Problem # 1: Lack of interactivity with the instructor. E-learning is normally done in two modes: synchronously and asynchronously. Synchronous e-learning occurs when the students listen and watch at the same time the instructor delivers the content, while asynchronous e-learning occurs when the students watch on a delayed basis. Students watching on a delayed basis cannot ask questions and get immediate feedback.

The best solutions for lack of interactivity are to allow e-mail communication, cultivate discussion groups, and post frequently asked questions. While these solutions can partially address the problem, it is difficult to get user-specific feedback and interchange that is rapid.

Synchronous e-learning does allow for immediate feedback and question/answer exchanges. Most of us know these e-learning events as webinars. While webinars are certainly cost-effective, the interaction is somewhat difficult to manage. Speakerphones, background noise, and poor telecommunications infrastructure can lead to feedback, distortion, and dropped words, resulting in a frustrating experience.

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Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

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Newer technologies show promise on this front. One of the most promising technologies is Telepresence. Several manufacturers, including Cisco, Polycom, Halo, and others are rolling out systems and infrastructure for this new, high definition, low latency communication medium. Semitracks is working to implement Telepresence technology for courses and seminars. In our test runs, students have indicated that watching a webinar is almost the same as being in the room with the instructor.

Problem # 2: Watching the computer screen. Numerous studies indicate that watching the computer screen is more tiring than watching a real instructor. Many people get eye strain or get bored and start doing other things. An e-learning presentation is, in many cases, less able to hold someone's attention than a live presentation is. The best method for tackling this problem with asynchronous courses is to "chunk" the courses into short segments – the shorter, the better. At Semitracks, we try to limit online course segments to 30 minutes or less. In fact, more than 50% of our online course segments are 15 minutes or less. Chunking courses reduces fatigue and distraction and makes it easier for students to fit segments into breaks or down times.

Problem # 3: Student interaction. While webinars allow limited interaction, the interaction level is not nearly as high as one can achieve with a face-to-face course. Although lack of real-time interaction is a serious limitation, technologies like Telepresence can combat the problem by allowing users to freely interact in real-time.

Problem # 4: Lack of laboratory and exercise activities. For some areas like laboratory analysis and equipment repair, lack of hands-on applications is a big challenge. However, as simulation development software improves, the problem will ease in the future. Furthermore, since many lab tools and instruments today are driven from a computer interface, some complex tools can be captured using simulation software.

In fact, computer simulations may even have an advantage over hands-on testing. Complex fabrication and analysis tools can be easily damaged, along with the samples or product. To avoid making a costly mistake, it's often better to learn on a simulator, much the way pilots learn to fly an aircraft by first using a simulator. The simulation approach will be needed soon in today's advanced IC foundries where wafer lots can run into the hundreds of thousands of dollars and tools can cost upwards of five million dollars.

Although the developing field of e-learning faces the challenges we've discussed, new technologies are continually emerging to address these problems. E-learning stands at the cutting edge of the market, poised to revolutionize the way we learn. In the next issue, we'll finish our discussion of online learning technology by addressing some of the concerns that people have when considering the switch to online training.

Ask the Experts

Q: You mentioned a couple of techniques, namely shroo and shrunk clock, that people here are not real familiar with. Can you explain these techniques in a little depth, or, even better, show real-world application of them?

A: Shrunk clock is a term occasionally used to refer to the shortening of a clock cycle while performing a speed path test. For example, let's assume an IC is operating at 50MHz. The clock cycle would be 20 nsec. If we increase the frequency to 66MHz, we have in essence "shrunk" the clock cycle to 15 nsec. So, a shrunk clock is another way of stating that we sped up an IC or a path within an IC.

Shroo is a contraction of shmoo and shrunk. Normally, a shmoo plot involves the entire IC. The term shroo refers to a shmoo plot on just a portion of the IC. For example, one can generate a shmoo plot for a particular speed path by changing the speed of the IC on one axis in the shmoo plot and the voltage (or possibly temperature) on another axis.

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Technical Tidbit

I_{DDQ} Circuitry, Part 1

Top: Keithley 236/238.
Bottom: Agilent 4155/4156

Quiescent power supply current (I_{DDQ}) testing is an effective method for identifying defects in CMOS integrated circuits. The technique is especially useful on circuits where bridging shorts, gate oxide shorts, or even open connections exist. The "D's" in I_{DDQ} refer to the drain-power supply connections that were common in early NMOS circuits. IEEE adopted I_{DDQ} as the terminology associated with quiescent power on an MOS integrated circuit in the 1980s, and the term carried into CMOS circuits.

I_{DDQ} is becoming more difficult to use because of the background leakage present in today's nanoscale ICs, but the technique can still be useful if the instrumentation and detection can detect current changes of 10 microamps or less. Because of the complexity in today's ICs, the test must also be fast.

Early on, some companies used commercial source-measurement units for I_{DDQ} tests. Two instruments with the capabilities to use commercial source-measurement units are Keithley and Agilent. The Keithley 236/238 instruments offer reasonable bandwidth and sensitivity to make I_{DDQ} measurements. Depending on the measurement speed, sensitivities down to the microamp level can be achieved. At measurement speeds of 10 kilohertz, sensitivities into tens of microamps can be achieved. The Agilent

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Commercialization Of Micro-Nano Systems 2010

Aug. 29 - Sept. 2, 2010
Albuquerque, NM

COMS brings together leaders from all over the world and every sector of industry; from high tech companies, national labs, regional development and government agencies, investment and consulting groups, market researchers, educators and students; all sharing, learning, and creating partnerships in an open, interactive setting. Find out more.

Semitracks MEMS Packaging & Reliability

Aug. 29, 2010
Albuquerque, NM

As an additional learning opportunity, Semitracks' 2010 MEMS Packaging & Reliability course will be held concurrently with the COMS conference. Find out more.

Course Spotlight: Design for Reliability

While reliability levels are at an all-time high level in the industry, rapid changes may quickly cause reliability to deteriorate. Thus, engineers have to put thought and effort into the reliability of a component during the design phase. Semitracks' three-day Design for Reliability course offers detailed instruction on three main topics:

1. **Fundamentals of Reliability Physics and Accelerated Testing.** Participants learn the fundamentals of various failure mechanisms and the testing used to accelerate those mechanisms.
2. **Design-In Reliability Issues.** Participants learn how the major failure mechanisms manifest themselves at the circuit and chip level. These include time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, etc. They learn the process for converting test structure results into circuit level behaviors.
3. **Mission Profiles.** Participants learn the conversion of transient use-conditions into static equivalents for Design Rule generation and verification.

Click to learn more about our latest course.

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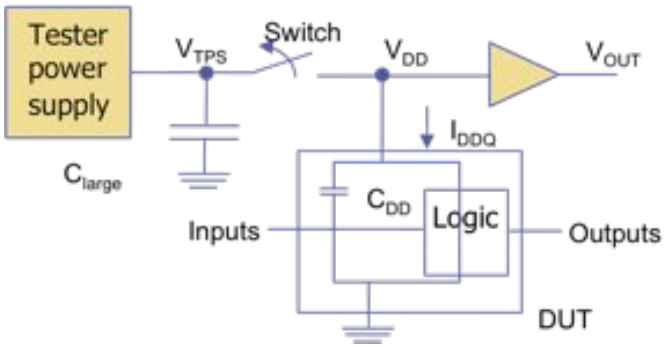
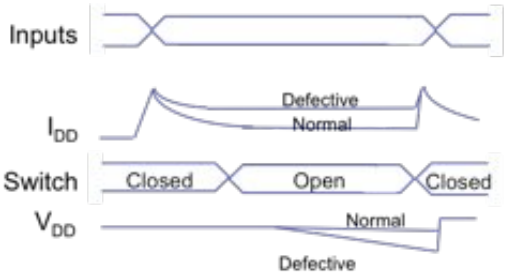
4155/4156 series instruments can also be used for I_{DDQ} measurements. Because of its precision source measurement units, the instrument can make measurements that are very accurate, but not fast. The instrument works well if you intend to only make one to 10 measurements per chip or die site.

Although commercial instrumentation is useful for I_{DDQ} measurements, it is often necessary to make faster measurements in a test environment. One might want to test complex ICs at thousands of vectors and millions of dice or chips in a high-volume production situation. Over the past 25 years, engineers have designed a number of specialized I_{DDQ} circuits, including four we discuss in this article: the Keating-Meyer circuit, QuiC-Mon (a design from Ken Wallquist at Philips Semiconductors), a circuit developed by Wayne Needham at Intel, and a circuit from Ken Ferguson and Brian Gerson at PMC-Sierra.

The image below shows the Keating-Meyer circuit developed by Mike Keating and Dennis Meyer at GenRad Corporation in the 1980s. The

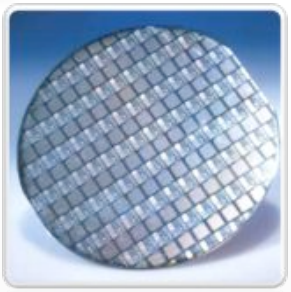


Model of Keating-Meyer technique (above) and timing diagram during I_{DDQ} measurement (below).



external circuit senses current by amplifying small dips in the power supply voltage. The voltage can be measured at test point V_{TPS} for large values or V_{OUT} for small voltages. The capacitance at the output of the tester power supply reduces the voltage drop associated with switching transients. A higher than expected current level appears as a larger than normal voltage drop at V_{DD} or V_{OUT}.

Although the Keating-Meyer circuit allowed for more rapid I_{DDQ} testing, engineers tried improving the circuitry so faster, more precise measurements could be made. In the next installment of this article, we'll discuss the resulting improvements in I_{DDQ} technology.



Upcoming Courses

Wafer Fab Processing
August 9-12 | San Jose, CA

Biotechnology for Electrical Engineers
August 9-11 | San Jose, CA

IC Packaging Design and Modeling
August 9-11 | San Jose, CA

IC Packaging Technology and Metallurgy
August 12-13 | San Jose, CA

Feedback

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Alicia Constant by email at alicia.constant@semitracks.com.

We are always looking for ways to enhance our courses and educational materials.

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