ISSUE
02
JULY
2009

SEMITRACKS
MONTHLY
NEWSLETTER

# INFOTRACKS

## Upcoming Courses

Semitracks continues to expand its courses, with new courses and new locations. We offer live seminars in Europe, North America, and Asia, and our online classes can be accessed anywhere in the world. Click on any course to find out more.

Failure and Yield Analysis

September 8-11, 2009
Munich, Germany

Semiconductor Reliability

September 14-16, 2009
Munich, Germany

MEMS Technology

October 5-6, 2009
Austin, TX, USA

Photovoltaics Overview

October 7, 2009
Austin, TX, USA

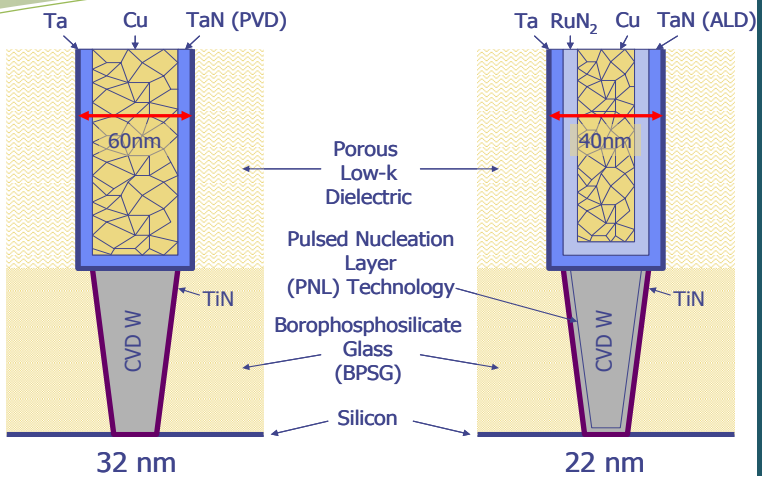
Photovoltaics Technology and Manufacturing

October 8, 2009
Austin, TX, USA

Wafer Fab Processing

October 19-22, 2009
Enschede, Netherlands

For information about online courses, click here.




## [inside this issue]



# Metal Issues Associated With Scaling

By Chris Henderson

As chip technologies continue to scale, the aspect ratio of the metal lines and contacts becomes more challenging. As part of a recent effort, Semitracks has compiled information regarding the width, thickness, materials, and processing steps for the lowest metal layers in the upcoming 32 nm and 22 nm semiconductor technology nodes. The lowest metal layer (metal-1) constitutes the most difficult layer on the IC for probing and obtaining signal information. However, it is one of the most important layers to probe to ensure proper chip functionality and implementation.

At the 32 nm node, the industry is still planning to use tungsten contacts to silicon. The aspect ratio of the contact can be as high as 9-to-1. Although some are working to switch to a lined copper contact to silicon at 22 nm, this is not likely. To accommodate a 22 nm process, tungsten contacts need a scaled titanium nitride liner deposited by Atomic Layer Deposition (ALD) and a scaled tungsten ALD seed process, followed by tungsten Chemical Vapor Deposition (CVD) fill. Although logic devices may have high-aspect-ratio contacts (up to 9-to-1), the stacked capacitor DRAMs push the envelope for this process, with an aspect ratio approaching 20.

Several parameters correlate to the width and thicknesses of metal interconnect. The most critical parameter is resistance. The continued scaling of interconnect reduces the cross-sectional area of the metal, increasing its resistance. This resistance problem actually grows at a rate faster than the rate of scaling because of current limitations with barrier technology.

The extension of the copper/barrier structure to 22 nm will not be simple. The increasing resistance of copper at reduced cross-section, as well as grain boundary and surface scattering effects, will mean that the traditional Ta/TaN/copper structure will likely not scale well to the 22 nm node with its 40 nm metal-1. To date, the industry has not figured out a method to scale the PVD TaN liner thinner than 8 nm. The other leading technique, ALD, does not produce an effective barrier because it does not adhere to copper. This is currently an area of significant work at leading edge manufacturers and equipment suppliers. Engineers are working on a dual material barrier that uses ALD TaN as the first layer, and then ruthenium (Ru) or $RuN_2$ as the second layer. Copper does adhere to Ruthenium. Engineers are also pursuing silver-copper and silver-manganese alloys.

With ionized Physical Vapor Deposition (PVD) processes, the TaN barriers can be scaled to ~8 nm. ALD TaN does not adhere well to copper. Ruthenium is considered a good adhesion layer, though it is a poor copper barrier — so a TaN or TiN barrier would still be required. If it is properly deposited, copper can be directly plated on

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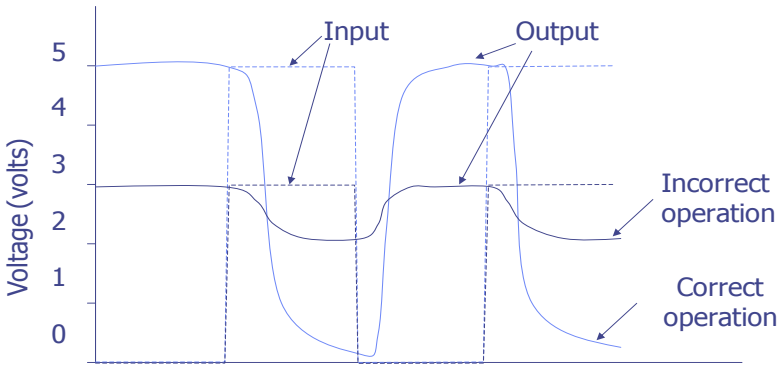
# Technical Tidbit

## Very Low Voltage (VLV) Testing

Very low voltage (VLV) testing, developed by Ed McCluskey and Hong Hao at Stanford University, is based on the theory that defective circuits will exhibit failures more obviously at low power supply voltages. While an IC with a subtle defect might work at its nominal operating voltage of 3.3 volts, it may not work correctly at 1.5 volts. Therefore, the difference in circuit performance between a defective and a defect-free circuit can be enhanced at low voltages, and, as a corollary, a test at low voltages is more likely to detect a problem.

This technique is potentially useful for catching problems related to defects on chips. It may not be as useful for problems related to process variations or design/manufacturing interactions, but this has not been explored in detail.




**NAND gate exhibiting a gate-source resistance in the upper n-channel transistor**

In this graph, we assume a gate-to-source resistance is in the upper n-channel transistor in a two-input NAND gate. When the device operates at 5 volts, the output switches correctly with the input. When the device is operated at 3 volts, the output does not switch correctly. Instead, the voltage remains at a level that would constitute a logical high value to the next input stage. If we assume that the gate-to-source resistance is attributable to an oxide defect, the defect grows worse with time, lowering the gate-to-source resistance until it becomes a logical failure at the regular operating voltage.

McCluskey and Hao did an experiment to try and prove this hypothesis. They tested 148 ICs at 6 volts and 2 volts. All of the ICs passed functional and parametric testing; however, one failed at 2 volts. The majority of these ICs also failed IDDQ testing. The 148 ICs were then burned in at 125°C for one week. After this test, the one IC that failed at 2 volts also failed at 5 volts.

McCluskey and his graduate students performed similar experiments several years later on 9 ICs that failed VLV testing. The 9 ICs were burned in at 125°C for one week and tested again. Two of the 9 failed just 6 hours into the burn-in. Based on the data, the test appears to find problems.

However, the question remains: is VLV more effective than burn-in, and can it replace an expensive test like burn-in? If it did, it would be much more cost effective. A VLV test does not require chambers and can be performed in a manner of seconds. While the test could certainly supplement burn-in, it is probably not a replacement for it.

# Metal Issues Associated With Scaling

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ruthenium. There are many development efforts aimed at bringing a Ru/Cu-based interconnect into production. Both silver (Cu-Ag) and manganese (Cu-Mn) alloys are being considered for improved interconnect reliability. Upon annealing manganese, a self-forming MnO barrier with superior reliability forms. Both alloys have a small negative impact on resistivity.

Another critical parameter is capacitive coupling. Capacitive coupling affects both circuit operation and signal extraction. Researchers are reducing capacitive coupling through the use of dielectric materials with ever lower dielectric constants. To reduce interline capacitance, low-k materials with k in the 2.2–2.5 range will be integrated at the 22 nm node. These materials are likely to be porous low-k materials, such as Hydrogen Silsesquioxane (HSQ) and Methylsilsesquioxane (MSQ), or possibly a polymer dielectric, like cross-linked polyphenylene (SiLK) or Bis-benzocyclobutene (BCB).

Another alternative is air gap approaches, most of which involve thermal decomposition of a porogen material. Low-k materials are thermodynamically unstable and mechanically weak (the lower the dielectric constant, the weaker the material). Plasma damage is a big issue with porogen low-k dielectrics at 22 nm. Furthermore, porogen materials also suffer from water uptake. Scientists at NEC are working on a closed-pore material that may not need the barrier layers that porogens need for protection. Finally, integration with the assembly and packaging processes is critical with all these processes.

The image on the first page shows a likely scenario for the 32 and 22 nm nodes. In the past, the industry had working techniques and processes for nodes 2-3 generations ahead of current production. That is not the case anymore. The 22 nm node is only 2 generations away, and a number of the interconnect processes are still undetermined. It will be interesting to see how this transition unfolds.

## What Our Customers Say:

"The techniques and case studies helped provide ideas when [I faced] issues."

"The time allotted [to the class] was very flexible, and the casual environment led directly to discussion."

"Entertaining and informative. Very insightful."

"Very well tailored to our specific needs."

"This is a very informative course that helped me to understand FA deeper."

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# Announcements

## Circuit Analysis Tools Proposers' Day

The Intelligence Advanced Research Projects Activity (IARPA) will host a Proposers' Day Conference for the Circuit Analysis Tools (CAT) Program on July 24, 2009 in anticipation of the release of a new solicitation in support of the program. The Conference will be held from 8:30am to 4:00pm in the Washington, DC metropolitan area. The purpose of the conference will be to provide information on the CAT Program, to address questions from potential proposers and to provide a forum for potential proposers to present their capabilities for teaming opportunities.

The CAT program is specifically interested in developing tools for integrated circuit analysis at future technology nodes, specifically the 22nm node and beyond. This includes analysis tools capable of working with advanced packages including but not limited to stacked die. These tools and techniques will address fault isolation, circuit edit, logic analysis and image analysis challenges for which there is currently no solution.

This announcement serves as a pre-solicitation notice and is issued solely for information and planning purposes. The Proposers' Day Conference does not constitute a formal solicitation for proposals or proposal abstracts. Conference attendance is voluntary and not required to propose to future solicitations (if any) associated with this program. Further information and registration is available at http://conference.brtrc.com/cat_pd/registration.

# Course Spotlight

## Photovoltaics Technology Now Online!

Every time you fill up your car with gasoline, you feel the impact of increasing oil prices, driving home the need for alternative energy. Solar power—the clean, renewable energy source of the future—is once again being seriously considered for widespread implementation.

Since the 1970s, a number of breakthroughs in photovoltaic technology have made electricity generated from light more feasible and economical. Today, many companies are rapidly developing and introducing technologies to harness power from the sun.

It is becoming difficult to keep track of the developments, let alone to understand them. Semitracks' latest online course, Photovoltaics Technology and Manufacturing, carefully examines a variety of topics, including:

- semiconductor material properties,
- silicon solar cell fabrication,
- high efficiency designs, and more!

This course is critical for every manager, engineer, and technician entering the photovoltaic field, whether they are working directly for a photovoltaic manufacturer or system integrator or selling to PV manufacturers.

For more information on our other courses or online interface, click here.

# Questions & Answers

***Q:*** *Devices are expected to withstand some amount of voltage/current stress; that's why input protection is included in all designs. How can I determine if EOS/ESD damage results from excessive stress conditions, a manufacturing defect, or an abnormal process variation? The question pertains to already damaged units, not virgin units.*

**A:** I would suspect an abnormal process variation if the device fails in a manner (exhibits damage in a location) that is inconsistent with the results from the in-house EOS/ESD testing. For example, the customer return device might have failed due to a gate oxide rupture, but NSC testing on comparison ICs indicates that the ESD clamp always fails. However, this cannot necessarily be determined by examining the damage site. One can envision a defect in the ESD clamp that causes a failure in the customer device. Maybe it simply fails at a lower voltage than it should. Your best bet is to characterize ICs from the same lot, or even from the same wafer, to see if they fail in a manner similar to the returned IC.

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*To post, read, or answer a question, visit http://www.forums.semitracks.com*

# Customer Feedback

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the August newsletter, please contact Alicia Constant at alicia.constant@semitracks.com. We are always looking for ways to enhance our courses and educational materials.