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InfoTracks

Semitracks Monthly Newsletter

Ask the Experts Shout Out

If you have been reading this newsletter for some time, you might have noticed the section on Ask the Experts and wondered: How can I present my question and have it answered? The solution is very simple, just send us an email at info@semitracks.com with the title "Ask the Experts" and your questions will be answered in upcoming newsletters.

Training: The Need is Becoming Critical – Part 3

By Christopher Henderson

Philosophy of Training

An effective training program requires that we start with the end in mind. Therefore, we should ask ourselves what the characteristics of an effective analyst are. Once we understand their characteristics, we can develop an education/training program to develop these characteristics. I have listed some of the characteristics that make a good failure analyst.

- Clear, logical thinking
- Does the job right the first time
- Organized (both in actions and in documentation)
- Has a good understanding of semiconductor technology (design, process, test, packaging, reliability, etc.)
- Understands the information a tool or technique can yield
- Can operate a variety of analysis tools

I have ordered the list in the order of importance for training. The top items on this list are things that are unchanging as technology advances. The bottom items tend to change with respect to time. Techniques change and evolve over time, while the actual tools tend to change most quickly. Ideally, we would like to ensure analysts understand and practice the upper items in the list. Once they understand those upper items, the lower items on the list will become easier to teach. Many analysts (and their managers) become fixated on particular tools or techniques. In a sense, this is putting the cart before the horse. Analysts who spend all their training time learning and re-learning the latest tools and techniques do not gain an appreciation of how their contributions fit into the big picture. Many times, they don't even make the transition to the ability to guide

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SEMITRACKS, INC.
Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

an analysis through from beginning to end.

Education and training for the analyst can be broken down into three areas: analysis process, technology, and technique training. Because failure analysis requires a broad set of skills and knowledge, companies need to be willing to invest more time in education and training than might be required for other areas, such as design, process, and packaging.

Process Training

Clear, logical thinking is essential to the analysis process. We need to understand up-front what the customer wants as an outcome. This will help guide the overall process. One approach to this clear, logical thinking process is outlined by Ferrier in this past year's International Symposium for Testing and Failure Analysis proceedings [1]. There are also a number of philosophical principles that are outlined by Henderson, Cole, Barton and Strizich in the 21st Century Product Analysis Manual [2]. Clear, logical thinking, coupled with an understanding of the technology, allows the analyst to develop a process flow for successfully analyzing the device of interest. Every analyst should be proficient in this area.

The analyst also needs to adopt the attitude that he or she will do it right the first time. Doing the job right the first time may seem to require more time, but the opposite is true. The president of your firm would much rather see 10 yield problems thoroughly addressed and solved, than 50 yield problems partially solved. In the first case, these problems are unlikely to surface again, while in the second case, the problems are likely to resurface in the future and cause more grief. This requires that the analyst, and especially his or her management, put back-pressure on over-demanding customers who want results yesterday. It is hard to apply clear logical thinking to an analysis problem when the customer is breathing down your neck.

The analyst must be organized in their work. Each analyst should maintain a laboratory notebook and document the analysis as it progresses. Most analysts perform more than one analysis at a time. While many analysts can keep the details of a single analysis straight in their minds, six or eight analyses is a different story. Good documentation allows the analyst to quickly generate a report at the end of the analysis. The analyst should generate a written report for every significant analysis finding. These should then be archived in the corporate knowledge based for future reference. Every analyst should be proficient in writing up reports. If an analyst is weak in this area, he or she should receive training.

There is considerable debate in the analysis community as to whether good analysts are born with their abilities (genetic), or successfully learn their skills. While genetics may certainly play a role, we need to be training people in this area.

Technology Training

All analysts should have a basic understanding of the circuit technology they analyze. While many engineers and technicians graduating from college should have a basic knowledge of circuit design and processing, one cannot assume this is so. Analysts have a variety of different educational backgrounds including: electrical engineering, physics, chemistry, and materials science. Because of reorganizations, layoffs, and other events, there may even be analysts with other backgrounds. Even within electrical engineering, some specialized in design, while others specialized in processing. Furthermore, many analysts may have not understood their classes the first time (or paid attention, for that matter). Analysts should be encouraged to take basic semiconductor technology courses to introduce them to the subject or refresh their memories.

By their nature, analysts must be generalists. They need a moderate depth of knowledge in a variety of subjects. To accomplish this, analysts should be encouraged to learn design, processing, test, packaging, and reliability. The more an analyst can understand these fields, the better they will be able to perform their jobs.

Technique/Tool Training

Finally, analysts need to understand the techniques and tools required to successfully analyze the devices manufactured by their companies. First, analysts need to understand the techniques. This would include an understanding of electrical test techniques and methods, package level techniques, delidding/decapping techniques, backside sample preparation techniques, optical and scanning electron microscopy, electron beam techniques, optical beam techniques, thermal detection techniques, scanned probe techniques, the focused ion beam, and analytical characterization techniques. Important, but often overlooked, is the knowledge to choose substitute techniques, implement techniques cost-effectively, and how/when to contract for techniques.

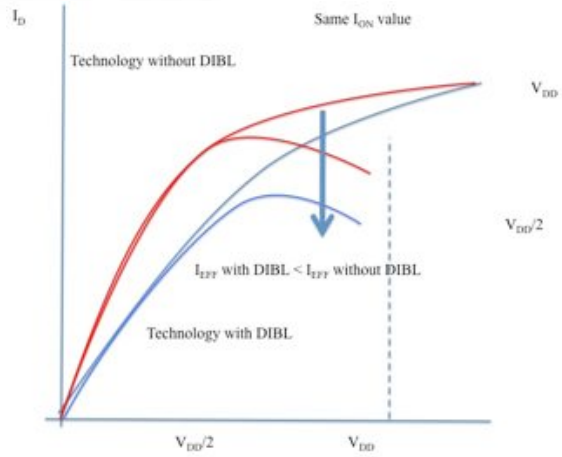
There is a misconception that "hands on" training will solve all of our problems. For example, I can train an analyst to be proficient at running a light emission microscope system, but without further knowledge, the analyst will not know how

Ask the Experts

Q: I was at IEDM last week and heard people talking about the problems with DIBL and how it affects the scaling of transistor. Can you explain what DIBL is and how it is a problem?

A: Drain induced barrier lowering or DIBL is an effect in MOSFETs where the threshold voltage decreases at higher drain voltages. In traditional technologies where the channel length is longer than 50nm, this typically results in an increase in drain current at a given voltage. This graph shows an example of this effect. While this effect may seem to be an advantage at longer channel lengths, since the given current at a particular drain-source voltage (VDS) is larger, it actually becomes a detriment in very advanced technologies.

As engineers continue to scale transistors, they have moved toward a different definition of current in order to estimate performance. Because the transistors in a CMOS gate never reach their peak current (given by ION), engineers instead use an IEFF value which corresponds to 50% of VDD. For a given IOFF and ION level, the transistor with the higher DIBL effect actually exhibits a lower IEFF value. The lower drain current occurs because the DIBL effect is more pronounced at higher drain voltages. Therefore, when one normalizes the ION values with and without DIBL, the net effect is a lower IEFF at 50% of VDD like we show in this graph. This is a fairly new revelation to device engineers, and requires some thinking as to how to address it at the 22nm nodes and smaller.



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properly set up the electrical stimulus to the part, what to do if he or she is not getting results, how to interpret the results, and what to do next. The analyst needs training to understand all of these issues. He or she therefore needs education in design and test, device physics, and failure analysis process. Furthermore, the analyst will need to be retrained when his or her company purchases a new light emission microscope system. Finally, the analyst should know how to perform light emission on a variety of platforms (turn-key systems, charge-coupled device cameras mounted to probe stations, standard optical microscope in a dark room, etc.). This is not adequately accomplished with "hands on" training. The same can be said for processing equipment, test equipment, etc. The process engineer needs to know more than "how to run the CVD system", and the test engineer needs to know more than "how to run the mixed-signal tester.

The Future of Training

As our world moves ever faster, our staff members are in need of "just in time" information. Although it

Course Spotlight: IC Packaging Metallurgy

As component sizes shrink, packaging is coming to the forefront as a key challenge the semiconductor industry faces in the 21st century. **IC Packaging Metallurgy** is a 2-day course that offers detailed instruction on the metallurgy issues associated with today's semiconductor packages.

Learn more at:
http://www.semitracks.com/index.php/courses/public-courses/packaging/ic-packaging-metallurgy

would be nice to provide six weeks of training each year for our people, we do not have the time or the budgets to do so. This is one area where the internet can help. We are developing internet-based course and reference material that can be viewed at any time. The material is broken into small "chunks," allowing them to learn during short breaks (equipment pumping down, data acquisition, lunch, first thing in the morning, end of the day, etc.). The material contains video, graphics and textual data (see Fig. 3). Moreover, the material covers a wide range of subjects, including design, process, packaging, test, reliability and technology, in addition to the subject of analysis.

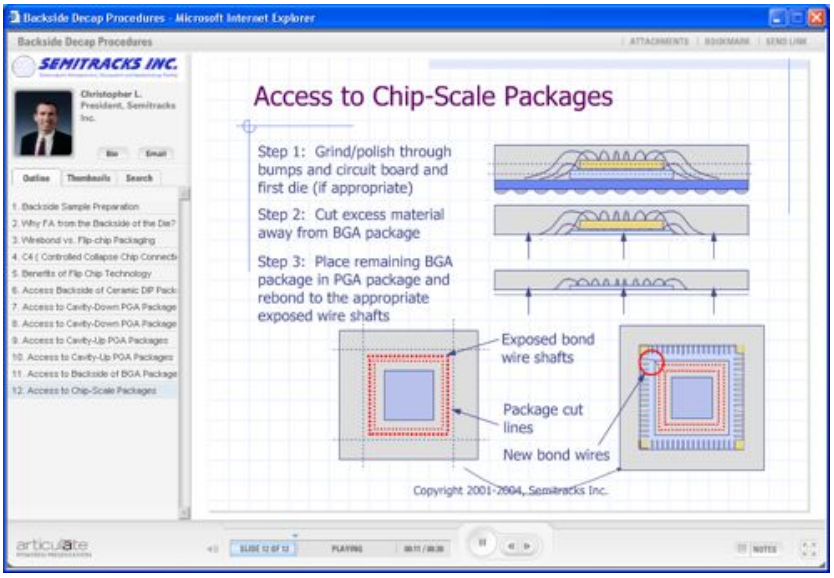

Fig. 3. Screen shot showing an example of internet-based training.

Conclusion

The design, processing, reliability, and analysis of semiconductor devices has grown increasingly complex. We all now require extensive, continuous education to successfully perform their jobs. We should concentrate on clear logical thinking, for this underpins every discipline within semiconductor technology. Our people also require based training for understanding related semiconductor disciplines such as analysis, design, process, technology, packaging, reliability and test. Finally, we need to understand the techniques and tools used for our specialties, with the caveat that an overemphasis on tools can actually reduce the effectiveness of the scientist/engineer/technician. Internet-based training may help alleviate some of the time constraints placed on today's workers. Training and education will play an increasingly critical role in the success of your company.

References

1. S. Ferrier, "A Standardized Scientific Method Formulation for Failure Analysis Application," Proc. Int. Symp. Test. & Failure Analysis (ISTFA), Nov. 2002, pp. 341-348.
2. C. Henderson, E. Cole, D. Barton, M. Strizich, 21st Century Product Analysis Manual, published by Semitracks Inc. 2001.

Upcoming Courses

Failure and Yield Analysis
January 18-21, 2011
Kuala Lumpur, Malaysia

IC Packaging Metallurgy
January 24-25, 2011
San Jose, CA, USA

Semiconductor Reliability
January 24-27, 2011
Kuala Lumpur, Malaysia

Semiconductor Package Design, Simulation and Technology
January 30-February 1, 2011
Tel Aviv, Israel

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or e-mail us at info@semitracks.com.

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by email at jeremy.henderson@semitracks.com.

We are always looking for ways to enhance our courses and educational materials.

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