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INFOTRACKS

YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Semiconductor Cleanroom Technology

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In this month's Feature Article, we will conclude our discussion of filtration as it applies to Semiconductor Cleanroom Technology. The ability to effectively filter particles from the atmosphere is the hallmark of a cleanroom, so we will discuss the specifications of HEPA filters used in semiconductor manufacturing.

HEPA filters, as defined by the United States Department of Energy standard that has been adopted by most American industries, must remove at least 99.97% of aerosols 0.3 microns in diameter. Since 0.3 microns is the most difficult particle size to filter out, filter specification uses this size particle to classify the filter. The filter's minimal resistance to airflow, or pressure drop, is usually specified around 300 pascals, or 0.044 psi, at its nominal volumetric flow rate.

The specification used in the European Union is European Standard EN 1822-1:2019, from which ISO 29463 is derived. This standard defines several classes of filters by their retention at a given MPPS value, or Most Penetrating Particle Size, for EPA, HEPA and ULPA filters. The overall efficiency is sometimes referred to as the "averaged retention", and the efficiency at a specific point is called the "spot retention".

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Today, a HEPA filter rating is applicable to any highly efficient air filter that can attain the same filter efficiency performance standards as a minimum, and is equivalent to the more recent National Institute for Occupational Safety and Health P100 rating for respirator filters. However, the United States Department of Energy has specific requirements for HEPA filters in DOE-regulated applications that may be different than the requirements for semiconductor cleanrooms.
Table 1 shows collection efficiencies for a single fiber. Notice that the collection efficiency for both impaction and interception fall off as the particle size decreases. This is due to the fact that the cross-sectional area of the particles becomes insufficient for the fibers to present a barrier to their movement, or even affect their movement. On the other hand, diffusion collection efficiency increases as the particle size decreases, since the collisions with the air molecules scatter the particulate, increasing their chance of adhering to the fiber mesh.

Efficiency	EN 1822	ISO 29463	Retention (averaged)	Retention (spot)
EPA	E10	—	≥ 85%	—
	E11	ISO 15 E ISO 20 E	≥ 95% ≥ 99%	—
	E12	ISO 25 E ISO 30 E	≥ 99.5% ≥ 99.9%	—
HEPA	H13	ISO 35 H ISO 40 H	≥ 99.95% ≥ 99.99%	≥ 99.75% ≥ 99.95%
	H14	ISO 45 H ISO 50 U	≥ 99.995% ≥ 99.999%	≥ 99.975% ≥ 99.995%
ULPA	U15	ISO 55 U ISO 60 U	≥ 99.9995% ≥ 99.9999%	≥ 99.9975% ≥ 99.9995%
	U16	ISO 65 U ISO 70 U	≥ 99.99995% ≥ 99.99999%	≥ 99.99975% ≥ 99.9999%
	U17	ISO 75 U	≥ 99.999995%	≥ 99.9999%

Table 1- Efficiency of EPA, HEPA and ULPA filters, their associated standards, their ratings, and their averaged and spot retention numbers.

For reference, in Figure 1 we show the sizes of typical particulate matter that might contaminate a cleanroom environment. Particulate matter from smog, rosin smoke, tobacco smoke, oil smoke, and carbon black are the smallest, while particulate matter from the condensation of clouds and fog, spores, pollen, coal dust, and metallurgical dust and fumes are the biggest.

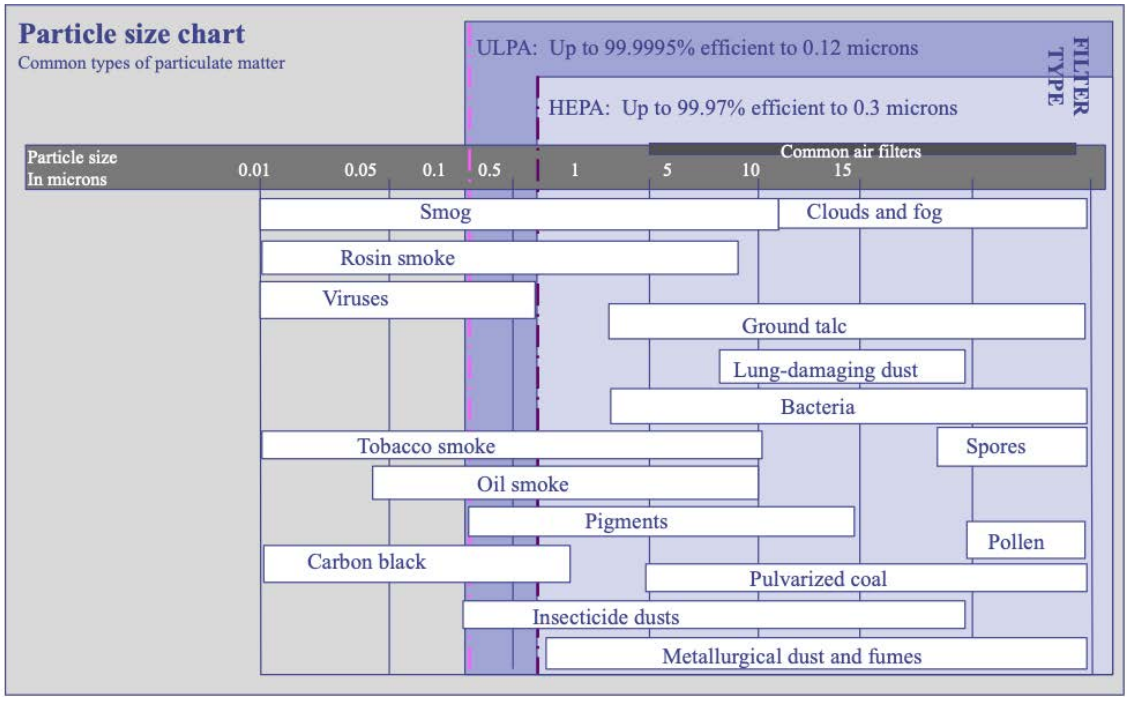

Figure 1- Common particulate matter, as a function of particle diameter, and the range over which HEPA and ULPA filtration is effective (after Sentry Air Systems, Inc.).

Finally, we will briefly discuss the testing of filters. Engineers from the Institute of Environmental Sciences and Technology (IEST) have written a number of recommended practices for testing these filters, including:
IEST-RP-CC001: HEPA and ULPA Filters,
IEST-RP-CC007: Testing ULPA Filters,
IEST-RP-CC022: Testing HEPA and ULPA Filter Media, and
IEST-RP-CC034: HEPA and ULPA Filter Leak Tests.

The most common test is the DOP test. DOP stands for 'dispersed oil particulate.' This is the substance used to create the particulate for testing the filters. The substance is then pressurized and released as a cloud into the air. Traditionally, the DOP substance is oil based and Dioctyl Phthalate has been used. Concerns regarding the carcinogenic properties of this substance have prompted the use of other substances such as Poly Alpha Olefin. For this reason, you may see this test referred to as POA testing.

As an aside, the Institute of Environmental Sciences and Technology (IEST) is a non-profit, technical society where professionals who work with controlled environments associate, gain knowledge, receive advice, and work together to create industry best practices. The organization serves environmental test engineers, qualification engineers, cleanroom professionals, those who work in product testing and evaluation, and others who work across a variety of industries, including: acoustics, aerospace, automotive, biotechnology/bioscience, cleanroom operations/design/equipment/certification, dynamics, filtration, food processing, HVAC design, medical devices, nanotechnology, pharmaceutical, semiconductors/microelectronics, and shock/vibration.

In next month's Feature Article, we will begin the discussion of the storage and delivery of Chemicals and Gases in a Cleanroom.

Technical Tidbit: ATE AC Instrumentation

This month's Technical Tidbit continues a short series on Automated Test Equipment (ATE) Instrumentation. In this month's Tidbit, we continue the discussion of ATE instrumentation by covering Alternating Current (AC) Instrumentation. Test engineers use this type of instrumentation in ATE system to determine AC voltage and current values in the course of testing integrated circuits.

AC Instrumentation provides source and capture test capability with Arbitrary Waveform Generation (AWG) and digitizing to meet the increased test requirements of today's complex circuits. In most modern Mixed-Signal testers, Source Measurement Units can create complex waveforms by combining simple waveforms together. In a Mixed-Signal test system, analog waveforms are turned into digital data for storage. This occurs in an instrument known as a digitizer. Digitizers can selectively capture specific waveform elements to minimize the number of samples for processing and to enhance test throughput.

Figure 1 shows the typical architecture for the AC instrumentation in a Mixed-Signal tester. The first item at the upper left is the Segment Controller. It is a Central Processing Unit, or CPU, that controls the start and stop of a waveform, as well as the type of waveform to be generated. The Segment Controller sends messages to the Signal Source Memory, which is a bank of non-volatile memory that contains a digital representation of the analog waveform to be presented to the Device Under Test, or DUT. The digital representation of the waveform is converted into an analog waveform by a Digital-to-Analog (D/A) Converter. This D/A Converter may also filter the analog waveform to create a smooth, noise-free signal. The conditioned signal is then sent through the Channel Card to set the voltage levels and offsets from other signals, and to potentially provide more filtering. This signal is then presented to the DUT as an AC waveform, sometimes referred to as an AC Source. The outputs from the DUT are captured through a Channel Card as well, which resets the levels and offset voltages, and provides some initial filtering. These signals then run through an Analog to Digital (A/D) Converter, that converts the analog input into a digital representation of the data, where it can then be captured and stored in the Signal Capture Memory. Like the Signal Source Memory, the Signal Capture Memory is also a bank of non-volatile memory. This information can then be processed by a Digital Signal Processor (DSP) or an Array Processor, so that important parameters can be extracted, like frequency, signal-to-noise (S/N) ratios, and Total Harmonic Distortion (THD).

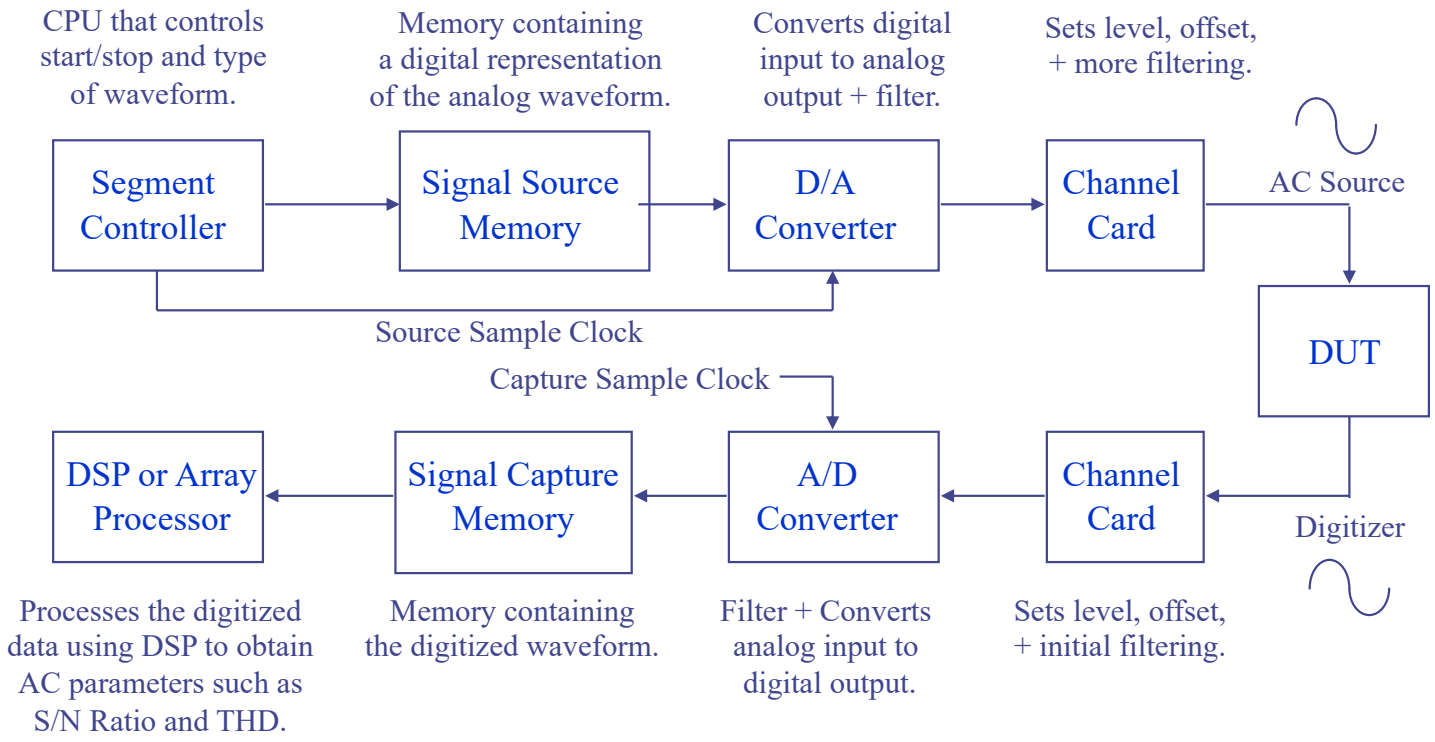

Figure 1- Schematic showing the block diagram of an AC Instrumentation module.

In next month's Technical Tidbit, we will discuss the Digital Subsystem portion of the ATE Instrumentation.

Ask The Experts

Q: I have heard the term "edge bead". To what does this term refer?

A: Thanks for your question. The edge bead is a region where photoresist builds up on the edge of the wafer during the spin coating process. Figure 1 shows the edge bead in a cross-sectional view. The edge bead can lead to problems during subsequent processing, like poor contact between the wafer and a chuck, so the edge bead needs to be removed after the photoresist is processed. The edge bead can be removed using adhesive tape methods, or through a nozzle directing a high purity solvent spray at the edge of the wafer.

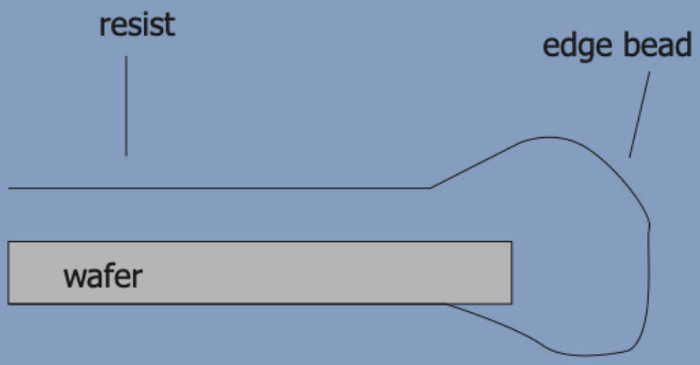

Figure 1- Cross-sectional view of the edge of the wafer and the edge bead structure.

Course Spotlight: IC PACKAGING TECHNOLOGY

OVERVIEW

Integrated Circuit packaging has always been integral to IC performance and functionality. An IC package serves many purposes: 1) pitch conversion between the fine features of the IC die and the system level interconnection; 2) chemical, environmental and mechanical protection; 3) heat transfer; 4) power, ground and signal distribution between the die and system; 5) handling robustness; and 6) die identification among many others. Numerous critical technologies have been developed to serve these functions; technologies that continue to advance with each new requirement for cost reduction, space savings, higher speed electrical performance, finer pitch, die surface fragility, new reliability requirements, and new applications. Packaging engineers must fully understand these technologies to design and fabricate future high-performance packages with high yields at exceptional low-costs to give their company a critical competitive advantage.

IC Packaging Technology is a two-day course that details the vital technologies required to construct IC packages in a reliable, cost effective, and quick time to market fashion. When completed, the participant will understand the wide array of technologies available; how technologies interact; what choices must be made for a high-performance product vs. a consumer device; and how such choices impact the manufacturability, functionality, and reliability of the finished product. An emphasis will be given to manufacturing; processes; and materials selection, tailoring, and development. Each fundamental package family will be discussed, including flip chip area array technologies, Wafer Level Packaging (WLP), Fan-Out Wafer Level Packaging (FO-WLP), and the latest Through Silicon Via (TSV) developments. Additionally, future directions for each package technology will be highlighted, along with challenges that must be surmounted to succeed.

By focusing on current issues in packaging technology, participants will learn why advances in the industry are occurring along certain lines and not others. Participants will learn about semiconductor packaging without having to delve heavily into the complex physics and materials science that normally accompany this discipline. Participants will learn basic, but powerful aspects about the semiconductor packaging. This skill-building series is divided into four segments:

1. **Molded Package Technologies.** Participants will learn the fundamentals of molding critical to leaded, leadless, and area array packaging, enabling them to eliminate problems such as flash, incomplete fill, and wire sweep.

2. **Flip Chip Technologies.** Participants will learn the fundamentals of plating, bumping, reflow, underfill, and substrate technologies that are required for both high performance and portable products.

3. **Wafer Level Packages**. Participants will learn the newest technologies that enable the increasingly popular Wafer Chip Scale Packages (WCSPs) and Fan-Out Wafer Level Packages (FO-WLPs).

4. **Through Silicon Via Packages and Future Directions.** Participants will understand the latest advances in the recently productized TSV technology, as well as future directions that will lead to the products of tomorrow.

COURSE OBJECTIVES

1. The course will supply participants with an in-depth understanding of package technologies, current and future.
2. Potential defects associated with each package technology will be highlighted to enable the participants to identify and eliminate such issues in product from both internal assembly and OSAT houses.
3. Cu and solder plating technologies will be described with special emphasis on package applications in Through Silicon Vias (TSVs) and Cu pillars for FO-WLPs. Emphasis will be placed on eliminating issues such as reliability, non-uniformity, void-free thermal aging performance, and contamination-free interfaces.
4. New package processes employed in TSV production will be described, along with current cost reduction thrusts, to enable the participants to understand the advantages and limits of the technologies.
5. Temporary bonding and wafer thinning processes will be highlighted, as well as the cost reduction approaches currently being pursued to enable wider adoption of TSV packages.
6. The trade-offs between silicon, glass, and organic interposers will be highlighted, along with the processes used for each.
7. Participants will gain an understanding of the surface mount technologies that enable today's fine pitch products.
8. This course will provide detailed references for participants to study and further deepen their understanding.

COURSE OUTLINE

Day 1

1. The Package Development Process as a Package Technology
    a. Materials and Process Co-Design

2. Molded Package Technologies
    a. Die Attach
        i. Plasma Cleans
    b. Wire Bonding
        i. Au vs. Cu vs. Ag
        ii. Die Design for Wire Bonding
    c. Lead Frames
    d. Transfer and Liquid Molding
        i. Flash
        ii. Incomplete Fill
        iii. Wire Sweep
        iv. Green Materials
    e. Pre- vs. Post-Mold Plating
    f. Trim Form
    g. Saw Singulation
    h. High Temperature and High Voltage Materials

3. Fan-Out Wafer Level Packages
    a. Chip First vs. Chip Last Technologies
    b. Redistribution Layer Processing
    c. Through Mold Vias

4. Through Silicon Via Technologies
    a. Current Examples
    b. Fundamental TSV Process Steps
        i. TSV Etching
        ii. Cu Deep Via Plating
        iii. Temporary Carrier Attach
        iv. Wafer Thinning
    c. Die Stacking and Reflow
    d. Underfill
    e. Interposer Technologies: Silicon, Glass, Organic

5. Surface Mount Technologies
    a. PCB Types
    b. Solder Pastes
    c. Solder Stencils
    d. Solder Reflow

Day 2

1. Flip Chip and Ball Grid Array Technologies
    a. Wafer Bumping Processing
        i. Cu and Solder Plating
        ii. Cu Pillar Processing
    b. Die Design for Wafer Bumping
    c. Flip Chip Joining
    d. Underfills
    e. Substrate Technologies
        i. Surface Finish Trade-Offs
        ii. Core, Build-up, and Coreless
    f. Thermal Interface Materials (TIMs) and Lids
    g. Fine Pitch Warpage Reduction
    h. Stacked Die and Stacked Packages
        i. Material Selection for Board Level Temperature Cycling and Drop Reliability

2. Wafer Chip Scale Packages
    a. Redistribution Layer Processing
    b. Packing and Handling
    c. Underfill vs. No-Underfill

Upcoming Courses:

Public Course Schedule:

Advanced CMOS/FinFET Fabrication - September 25-26, 2023 (Mon.-Tues.) | Phoenix, Arizona - $995

IC Packaging Technology - January 23-24, 2024 (Tues.-Wed.) | Phoenix, Arizona - $1,295

Advanced CMOS/FinFET Fabrication - January 29-30, 2024 (Mon.-Tues.) | Phoenix, Arizona - $995

Wafer Fab Processing - February 26-29, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095

Failure and Yield Analysis - March 4-7, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095

Semiconductor Reliability and Product Qualification - March 11-14, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095

Defect-Based Testing - March 20-21, 2024 (Wed.-Thurs.) | Munich, Germany - $1,195

Webinar Schedule:

IC Packaging Design and Modeling - September 18 - 21, 2023 (Mon. – Thurs.) | - $600

Have an idea for a course? If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please email us at info@semitracks.com

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!