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Hybrid Microcircuit Packaging Part II

By Christopher Henderson

Conductors are used for a variety of purposes in hybrid microcircuits. In addition to the usual function of interconnects, they also form terminals and electrodes. The table in Figure 8 lists some of the more commonly-used conductors in hybrid microcircuits.

Commonly Used Conductors and Their Uses in Hybrid Microcircuits		
Conductor	Symbol	Use
Gold	Au	Wire, plating, thick films, thin films, filler in epoxy conductive adhesives for device attachment
Gold-platinum	Au-Pt	Thick film solderable conductors
Gold-palladium	Au-Pd	Thick film solderable conductors
Gold-silver	Au-Ag	Thick film solderable conductors
Gold-silicon	Au-Si	Eutectic attachment of devices of ohmic contact
Gold-germanium	Au-Ge	Eutectic attachment of devices of ohmic contact
Silver	Ag	Lower-cost conductor, thick film plating, thin film, EMI, filler for epoxy conductive adhesives
Silver-palladium	Ag-Pd	Thick film (low silver migration)
Silver-platinum	Ag-Pt	Thick film (low silver migration)
Copper	Cu	Thick film (low cost), thin film, foil and plating for printed circuit boards, wire, filler for epoxy conductive adhesives
Aluminum	Al	Wire, thin film metallization for devices
Tungsten	W	Thick film conductors for co-fired tape substrates and packages
Molybdenum-manganese	Mo-Mn	Thick film conductors for co-fired tape substrates and packages
Nickel	Ni	Barrier metal, low conductivity metal, plating
Tin-lead alloys	Sn-Pb	Solder for attachement of components, plating for circuit boards
Indium and alloys	In	Low-temperature solder for attachment of devices and components
Tin-silver alloys	Sn-Ag	Low-temperature solders

Figure 8. Conductors.

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Adhesives also play a big role in hybrid microcircuit assembly. There are two basic types of adhesives: thermoplastic and thermosetting. These terms are discussed in more detail elsewhere on this site. Adhesives can be cured with heat, light, microwave energy, and even moisture. In hybrid microcircuits, adhesives can serve one or more purposes such as mechanical attachment, electrical connection, assistance in the removal of heat, and as a buffer layer to absorb stress. They are typically used for die, substrate or lid attachment, or surface mounting. Adhesives usually come as a pre-form, or a shape that is specially formed to be the size of the area required (Figure 9).

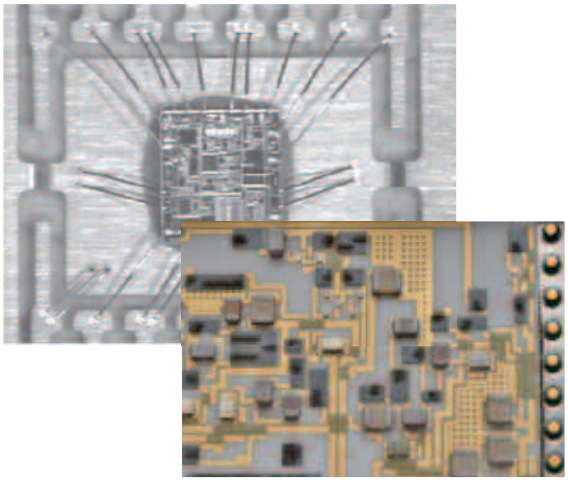


Figure 9. Adhesives.

Hybrid microcircuit packages (Figure 10) can be used in systems in an unencapsulated or encapsulated manner. In an unencapsulated system (a), the components and the surface of the substrate are exposed. This solution is fine if the microcircuit will be used in a protected, controlled environment. One can protect the hybrid with a polymer (b). This can be useful for mechanical protection from dust or foreign objects, but it doesn't protect against moisture or corrosive environments. For more robust environmental protection and for use in a wider temperature environment, ceramic (c) or metal (d) packages are more appropriate. These packages can also be made hermetic, to seal out moisture and other contaminants.

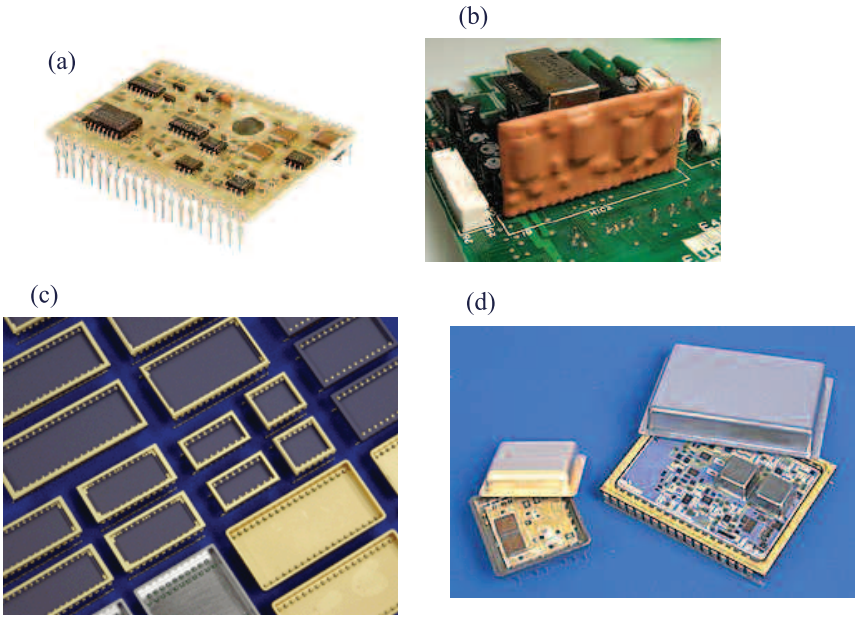
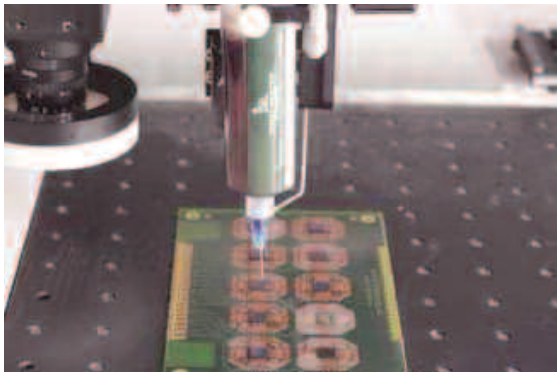


Figure 10. Packages.

The last item to discuss in relation to hybrid microcircuit packaging is die attach. A common die attach material is gold-silicon eutectic (Figure 11-a). It provides a stable mechanical and electrical connection that works at high temperatures. Silver-filled epoxy is the most common die attach method. It is low cost and easy to process, but it does have some reliability issues like poor electrical connectivity. Silver-glass adhesives are a potential substitute for gold-silicon eutectic, as they have high thermal conductivity and a coefficient of thermal expansion (CTE) close to that of silicon. A fourth die attach material is solder. Solders provide better thermal conductivity. The first three alloys listed in the table (b) are the most widely used in die attach. Sn5Pb85Sb10 is used for the second of two steps in soldering operations, where one of the first three alloys is used in a first step. By controlling the reflow profile, the first solder joint is not disrupted. No completely satisfactory nontoxic lead-free alloy is available at this time to fill the roles of the first three alloys listed in the table. Au80Sn20 would be useful, but is prohibitively expensive. Others—such as Sn95Sb5—are just slightly too low in liquidus temperature. In any case, high-Sn alloys tend to be brittle, exhibit poor thermal cycling behavior and are susceptible to the Kirkendall effect in devices operating at elevated temperature. Bismuth is available and inexpensive but is the least metallic of all the metals. It offers relatively poor ductility and thermal and electrical conductivity. It is questionable whether Bi/Ag alloys will find wide application, despite having a suitable liquidus temperature.



(a)

Alloy	Solidus (°C)	Liquidus (°C)
Sn5Pb95	308	312
Sn10Pb88Ag2	267	290
Sn5Pb92.5Ag2.5	287	296
Sn5Pb85Sb10	245	255
Sn65Ag25Sb10	233	233
Sn95Sb5	235	245
Bi97.4Ag2.6	262	262
Bi89Ag11	262	400
Au80Sn20	280	280

Die attach solder alloys

(b)

Figure 11. Die attach.

In conclusion, we briefly discussed hybrid microcircuit packaging. There are several elements that comprise a hybrid microcircuit beyond the semiconductor devices. They include the thick and thin film materials used on the substrate, the substrate itself, the resistors, capacitors, adhesive materials to bond the substrate to the package, the passive elements to the substrate, and the lid seal. We also covered the packages themselves as well as the die attach material. Hybrid microcircuits are likely to be used for some time into the future as they fulfill an important niche in high-reliability electronics.

Technical Tidbit

Randomized Block Experiments

An extension of the ANOVA method is to use the process to examine an experimental design with blocking. Blocks might represent different batches of wafers, or a product run through different factories, or material run over different periods of time in the same factory. In a blocked design the idea is to quantify the effect of the different treatments, or methods, and the blocking scheme. In a randomized block design, the setup will eliminate variations between the batches. One can then test if the methods are effective by checking to see if the means are equal. One can also look at the residuals, or what remains after the grand average, methods and block effects are taken into account. Put another way, one can use residuals to identify relationships between the means and the variances.

	Method and Resulting Yield (%)				
	A	B	C	D	Block Average
Batch 1	92.3	94.3	98.2	96.4	95.3
Batch 2	94.1	87.4	96.5	87.8	91.5
Batch 3	89.7	93.2	94.9	90.2	92.0
Batch 4	91.2	96.5	93.3	90.4	92.9
Batch 5	86.7	91.9	94.5	92.2	91.3
Treatment Average	90.8	92.7	95.5	91.4	92.6

Figure 1. Example.

Probably the best way to understand this is to show an example. Let's assume that we have 5 batches of a new chip design that we plan to run through 4 factories, to comply with multi-sourcing requirements for our customer. We'll refer to these factories as Factory A, Factory B, Factory C, and Factory D. We then look at the yield associated with those factories and group them in the table like we show here. We then

generate averages associated with the Blocks (or batches in this case) and the Treatments or Methods (the factories in this case). Those averages are also shown here in this table.

Anova: Single Factor		alpha =0.05				
SUMMARY						
Groups	*Count*	*Sum*	*Average*	*Variance*		
A	5	454	90.8	7.83		
B	5	463.3	92.66	11.493		
C	5	477.4	95.48	3.622		
D	5	457	91.4	10.26		
ANOVA						
Source of Variation	*SS*	*df*	*MS*	*F*	*P-value*	*F crit*
Between Groups	64.8855	3	21.6285	2.60545099	0.08764007	3.23887152
Within Groups	132.82	16	8.30125			
Total	197.7055	19				

Figure 2. Example (cont.).

We then perform an ANOVA single factor analysis. We use an alpha value of 0.05, which corresponds to a 95% confidence level in our F-distribution. This analysis yields the results shown here on this slide. Notice that our F statistic, or F-ratio, is 2.605. This value is less than F-crit, which for 19 degrees of freedom (the sum of the between groups and the within groups degrees of freedom) and an alpha value of 0.05, is 3.24. This implies that the null hypothesis is true, or in this case, the yields are not statistically different, which would further imply that our four factories are manufacturing essentially identical product. Furthermore, since the P-value is greater than 0.05, that further confirms that our four factories are manufacturing essentially identical product.

In the ANOVA data, we assumed a single factor, or that our batches were identical. Now let's assume that the batches are actually wafers from different suppliers we intend to use. In order to account for this additional variable, we perform a two-factor ANOVA without replication. We do it without replication since there is just one value we're examining, the yield. This table shows the results.

Anova: Two-Factor Without Replication						
SUMMARY	*Count*	*Sum*	*Average*	*Variance*		
Batch 1	4	381.2	95.3	6.54		
Batch 2	4	365.8	91.45	20.75		
Batch 3	4	368	92	6.12666667		
Batch 4	4	371.4	92.85	7.41666667		
Batch 5	4	365.3	91.325	10.8558333		
A	5	454	90.8	7.83		
B	5	463.3	92.66	11.493		
C	5	477.4	95.48	3.622		
D	5	457	91.4	10.26		
ANOVA						
Source of Variation	*SS*	*df*	*MS*	*F*	*P-value*	*F crit*
Rows	42.638	4	10.6595	1.41839835	0.28670237	3.25916673
Columns	64.8855	3	21.6285	2.87798008	0.08015854	3.49029482
Error	90.182	12	7.51516667			
Total	197.7055	19				

Figure 3. Example (cont.).

Again, notice that our F ratios are less than the F-crit values, so the implication is that the manufacturing methods are statistically the same. Also, notice that the p-value for the rows is much greater than 0.05. It is important though, not to read too much into this.

1. The p-value is not the probability that the null hypothesis is true, or the probability that the alternative hypothesis is false.
2. The p-value is not the probability that the observed effects were produced by random chance alone.
3. The 0.05 significance level is merely a convention.
4. The p-value does not indicate the size or importance of the observed effect.
5. In the absence of other evidence, the information provided by a p-value is limited.

Ask the Experts

Q: Does a Defect Density of 3 defects/cm2 mean that a chip that is 1cm2 will not yield (*i.e.,* the yield will be zero)?

A: No that is not true. Defects are typically randomly dispersed, so a defect density of 3 defects/cm^2 is the average. There will be 1cm2 areas with 2, 1, or even no defects, and other 1cm^2 areas with more than 3 defects. So there will be some yield. It will not be very large, but there will be some yield.

Spotlight: Defect-Based Testing

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's application-specific ICs and microprocessors can contain upwards of 100 million transistors. Traditional testing relies on the stuck-at-fault (SAF) to model defect behavior. Unfortunately, the SAF model is a poor model for defects. Other models and strategies are required to catch killer defects on integrated circuits. As transistor sizes decrease, the types and properties of the killer defects change. This has created a number of challenges related to the testing of components. ***Defect-Based Testing*** is a two-day course that offers detailed instruction on the electrical behavior and test strategies for integrated circuits. We place special emphasis on electrical behavior, fault models, and test techniques. This course is a must for every manager, engineer, and technician working in IC test, IC design, or supplying test hardware and software tools to the industry.

By focusing on the fundamentals of circuit behavior and the impact of defects on circuit behavior, participants will learn how to design, write, and implement test strategies to catch defects. Our instructors work hard to explain semiconductor test without delving heavily into the complex algorithms and computer science that normally accompany this discipline.

Participants learn basic but powerful aspects about defect-based testing. This skill-building series is divided into four segments:

1. **Electrical Behavior of Defects.** Participants study the electrical behavior of defects. They learn how open circuits, resistive vias, shorts, and transistor variations affect the electrical behavior of the individual transistor as well as gate elements and larger blocks.
2. **Fault Models for Defect-Based Testing.** Participants learn about the historical underpinnings of the stuck-at-fault (SAF) model. They also learn about other testing models, including IDDQ testing, at-speed testing, and delay testing.
3. **Production Test Methods.** Participants learn about standard digital testing, SAF testing, IDDQ, timing, low voltage tests, and other types of stress tests. They explore the strengths and weaknesses of each test type.
4. **The Economic and Quality Impact of Defect-Based Testing.** Participants learn how defect-based testing can actually improve test economics. They also study the impact to quality and reliability.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of defect-based testing and its technical issues.
2. Participants will understand the basic concepts of test economics, yield, test time and the cost of test. They also learn how defect-based testing can reduce the possibility of failures in the field.
3. The seminar will identify underused test techniques like IDDQ and Very Low Voltage (VLV) test techniques that can successfully find defects that are difficult to catch using conventional test techniques.

4. The seminar offers the opportunity to discuss specific test problems with our expert instructors.
5. Participants will be able to identify basic and advanced principles for defect-based test.
6. Participants will understand the difficulties in extending IDDQ testing to leading edge products and how to overcome some of these limitations.
7. Participants will become familiar with Design for Test (DFT) and Automatic Test Pattern Generation (ATPG) tools used for defect-based testing.
8. The seminar will introduce fundamental and advanced concepts related to extending defect-based testing to future designs.
9. Participants will learn what tools are available today to implement defect-based testing.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on defect-based testing. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field.

COURSE OUTLINE

Day 1

1. What is Defect-Based Testing?
   a. Introduction
   b. Terminology
   c. Existing test techniques
2. CMOS IC Defect Mechanisms and Detection Techniques
   a. Normal transistor and gate behavior
   b. Sources of random and systematic defects
   c. Types of Defects and How to Detect Them
      i. Bridging defects
      ii. Resistive defects
      iii. Open circuit defects
      iv. Delay defects
3. Fault Models for Defect-Based Test
   a. Stuck-at-fault (SAF)
   b. Delay fault

Day 2

   c. Leakage fault
   d. Methods for implementing fault models
   e. Existing software tools

4. Production Test Methods
   a. Functional testing (At-speed testing)
   b. IDDx Testing
   c. Timing Test
   d. Low Voltage Testing
   e. Stress Testing
5. Defect-Oriented test Economics and Product Quality
   a. Test set reduction
   b. Effectiveness in catching defects
   c. Yield and fallout
6. Case Histories

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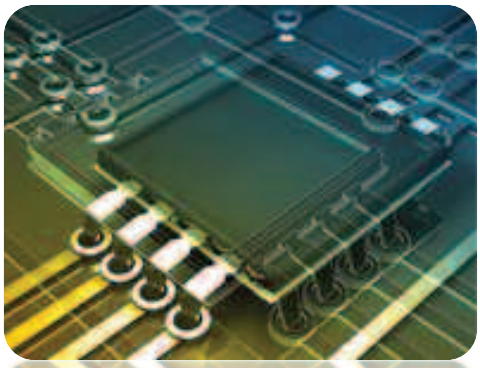
Semiconductor, Microelectronics, Microsystems and Nanotechnology Training

5608 Brockton Court NE
Albuquerque, NM 87111
Tel. (505) 858-0454
Fax (505) 858-9813
e-mail: info@semitracks.com



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San Jose, California

Introduction to Processing
January 5 – 6, 2017 (Thur – Fri)
Shanghai, China