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Substrate Materials II

By Christopher Henderson

There are other package substrate and dielectric isolation materials in use. One important material is polyimide. Manufacturers use this material extensively in redistribution layer and bump processes. It is easy to deposit, has a high glass transition temperature, a reasonable dielectric constant, and can be easily patterned. However, it does have a high coefficient of thermal expansion. Another important material is benzocyclobutene. It is also easy to deposit and has a low dielectric constant, making it good for high frequency applications. We discuss materials properties of these materials and others a little later in this presentation. However, it also has a high coefficient of thermal expansion. Another material in use is bismaleimide-triazine, or BT. It is also easy to process and has a low dielectric constant, and it has a relatively low CTE of 14 parts per million per degree centigrade.

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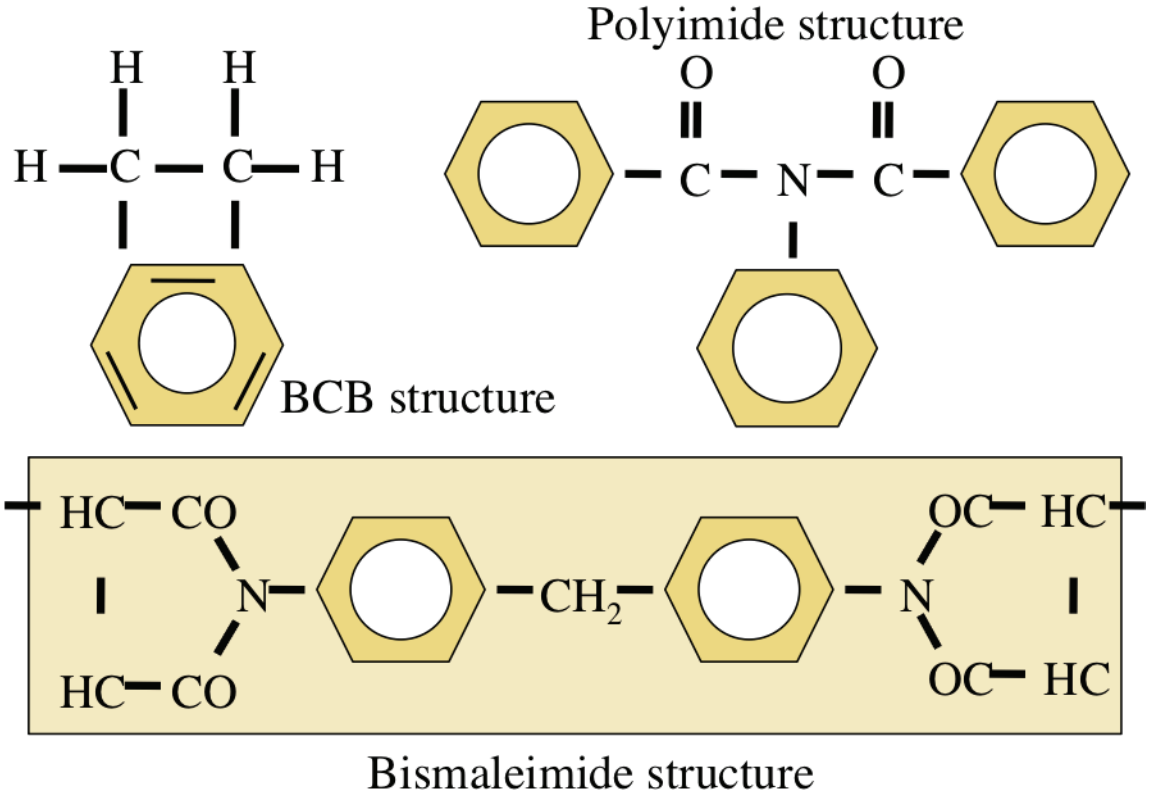
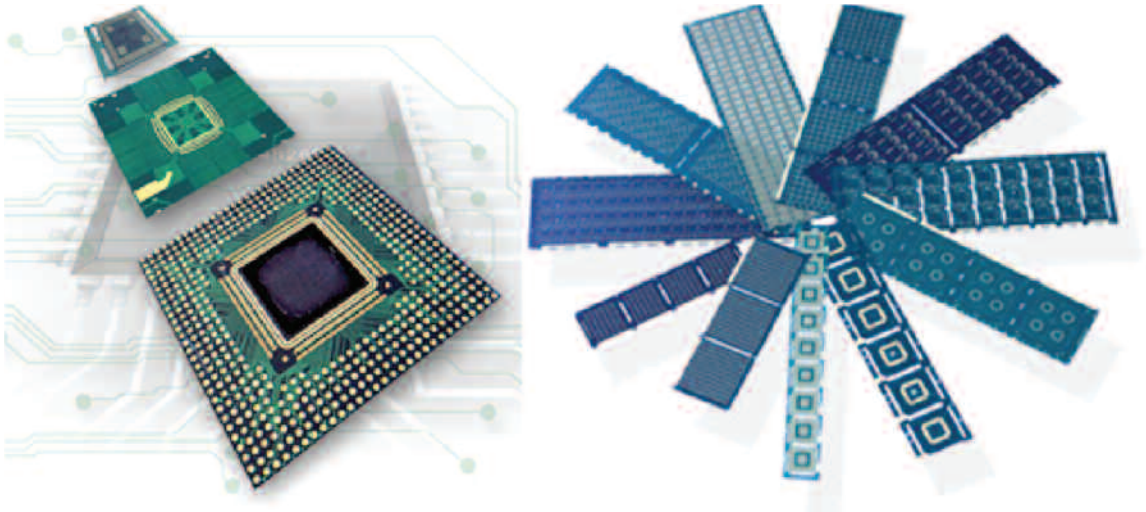
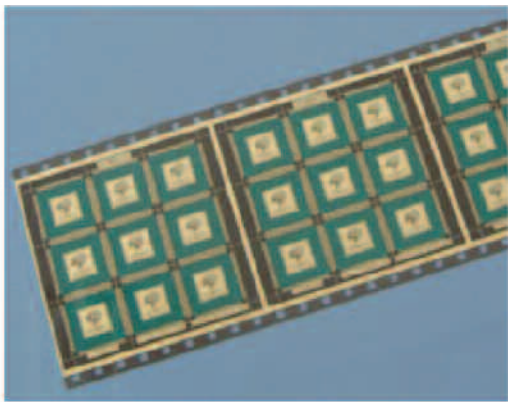


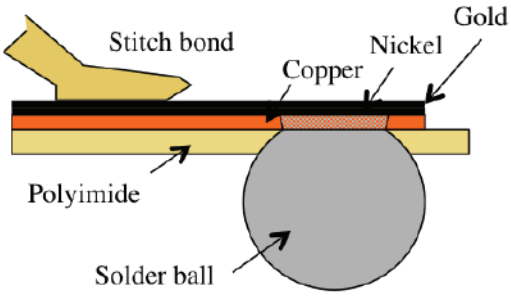
Bismaleimide structure

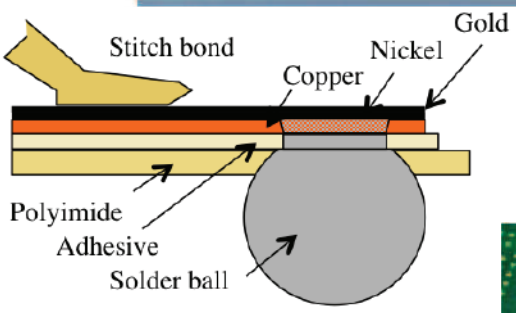
BT epoxy resin is used commonly with laminates. Engineers can create build-up layers and plated through holes on the finished laminate. BT resin epoxy laminates make an excellent choice for BGA substrates since the BT epoxy allows for higher frequencies, and the higher glass transition temperature allows for higher temperature use. Furthermore, BT substrates can be processed in strip format for high volume manufacturing.



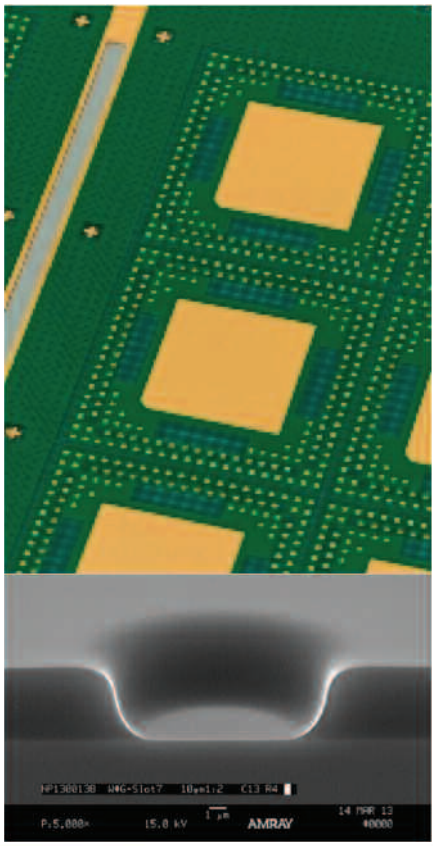
Polyimide can be used not only for isolation in redistribution layer technology, but also as a substrate material. DuPont makes polyimide materials that go by the trademarks Kapton and Pyralux that can be used for flexible substrates. Amkor also uses polyimide in one of their BGA packaging processes. fleXBGA is Amkor's term for their fine pitch BGA substrate technology. They process this as either a 2-layer tape without adhesive and wet-etched holes, or a 3-layer tape with adhesive and punched holes for connections to the solder bumps.







BCB polymers are also used for microelectronic packaging and interconnect applications. During the 1990s, they gained commercial status in applications including the fabrication of gallium arsenide integrated circuits, bumping and redistributing GaAs chips, and for planarization and isolation in flat-panel displays. More recently, Dow Chemical and others have developed techniques to B-stage or partial cure the BCB material, and then spin deposit it onto a wafer or other substrate. Engineers then use the BCB as an isolation layer between dice in a multi-die package, as an isolation layer for interconnect in a redistribution layer, and other configurations. One can etch BCB with dry etch techniques, or one can formulate photosensitive BCB resins for lithography applications.



Technical Tidbit

Bend Test

Another common Board Level Reliability (BLR) test is the Bend Test. The Monotonic Bend Test is a 4-point bend of the test board to failure, with an examination of how the board fails. This test can be useful to assess the impact of the backgrinding roughness. The Cyclic Bend Test is a 3-point test to introduce non-uniform strain distribution. One can also run the Cyclic Bend Test as a 4-point test to provide uniform strain distribution and better repeatability. IPC 9702 describes the Monotonic Bend Test, while JEDEC JESD22-B113 describes the Cyclic Bend Test.

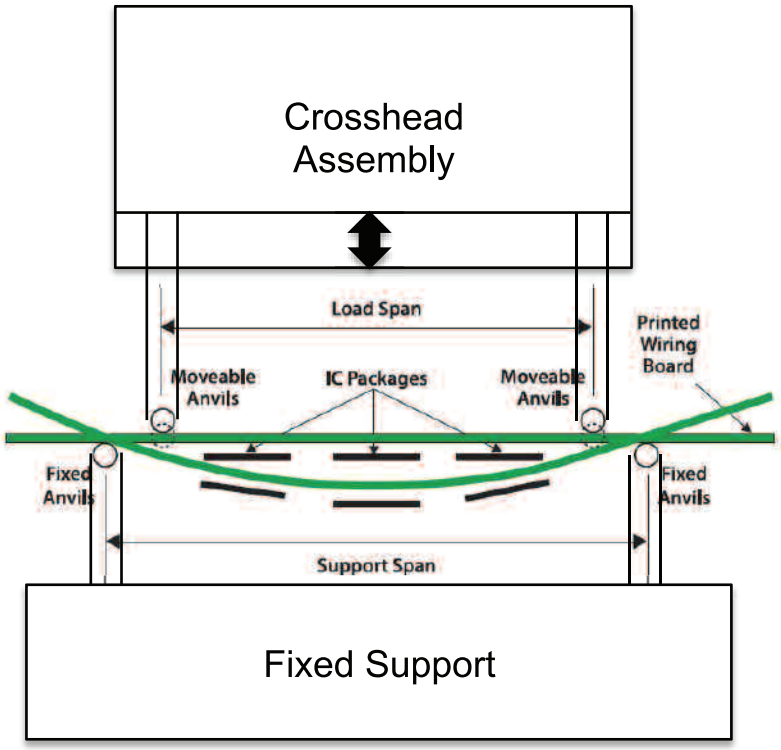


Figure 1. Diagram showing the 4-point bend test apparatus.

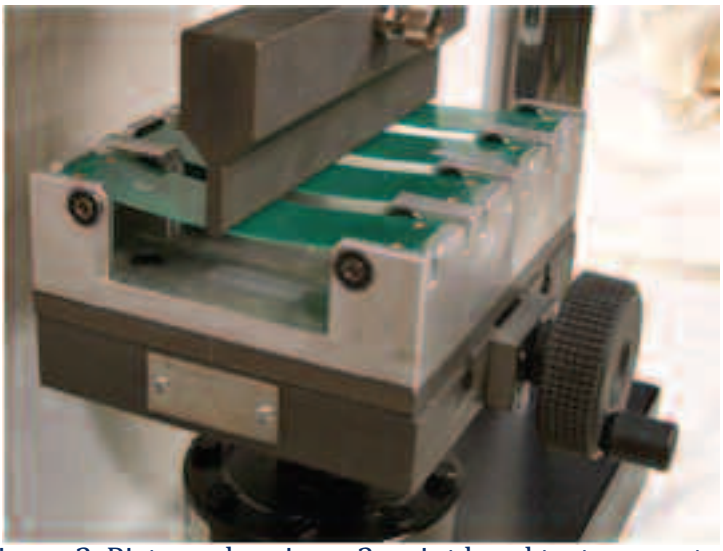


Figure 2. Picture showing a 3-point bend test apparatus.

Unlike other product qualification tests, BLR is a test to failure. In order to establish confidence in the distribution parameters, engineers will typically test to 50% failure. However, it is not necessary to get to 50% cumulative failures if one can establish slope and intercept. The test cycle time varies from job to job. Once the engineer obtains the data, they perform a Weibull analysis on the data to determine β (the characteristic lifetime) and η (the Weibull slope or spread in the data). Once the engineer calculates these values they can estimate the time to an arbitrary failure rate (typically one of interest to the customer), generate life estimates, and perform warranty analysis. Engineers analyze the failures to determine the failure mode and mechanism associated with the failures, and then performs root cause analysis to see if we need to make changes to our products, changes to the specifications, or changes to our customer application notes.

Ask the Experts

Q: Why do we use different materials in Solid Immersion Lenses (SILs)?

A: It has to do with the wavelengths we want to pass through the SIL. For example, a Si SIL works well for longer wavelengths like 1300nm (used for techniques like TIVA/OBIRCH), a GaAs SIL works well for mid-wavelengths like 1064nm (used for techniques like LADA), and a GaP SIL works well for shorter wavelengths (like those down in the visible range).

Spotlight: Semiconductor Reliability

OVERVIEW

Semiconductor reliability is at a crossroads. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. Analysis and experimentation is now performed at the wafer level instead of the packaging level. This requires knowledge of subjects like: design of experiments, testing, technology, processing, materials science, chemistry, and customer expectations. While reliability levels are at an all-time high level in the industry, rapid changes may quickly cause reliability to deteriorate. Your company needs competent engineers and scientists to help solve these problems. ***Semiconductor Reliability*** is a three- to five-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, using semiconductor components, or supplying tools to the industry.

Participants learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions and their parameters.
2. **Failure Mechanisms.** Participants learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die level and at the package level. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, etc.
3. **Qualification Principles.** Participants learn how test structures can be designed to help test for a particular failure mechanism.
4. **Test Strategies.** Participants learn the basics on how to test test structures, design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.
2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.
3. The seminar will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.
4. The seminar offers a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic test structures and how they are used to help quantify reliability on semiconductor devices.
6. Participants will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

One unique feature of this workshop is the video segments used to help train the students. Reliability Analysis is a visual discipline. The ability to identify nuances and subtleties in graphical data is critical to locating and understanding the defect. Some tools output video images that must be interpreted by engineers and scientists. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

Day One (Lecture Time 8 Hours)

1. Introduction to Reliability
    a. Basic Concepts
    b. Definitions
    c. Historical Information
2. Statistics and Distributions
    a. Basic Statistics
    b. Normal Distribution
    c. Lognormal Distribution
    d. Weibull Distribution
    e. Exponential Distribution
    f. Which Distribution Should I Use?
    g. Data Handling

Day Two (Lecture Time 8 Hours)

3. Die-Level Failure Mechanisms
    a. Time Dependent Dielectric Breakdown
    b. Hot Carrier Damage
    c. Negative Bias Temperature Instability
    d. Electromigration
    e. Stress Induced Voiding

Day Three (Lecture Time 8 Hours)

4. Package Level Mechanisms
    a. Ionic Contamination
    b. Moisture/Corrosion
    c. Thermo-Mechanical Stress
    d. Thermal Stress/Cycling
5. Use Condition Mechanisms
    a. Electrical Overstress/ESD
    b. Radiation

Day Four (Lecture Time 8 Hours)

6. Test Structures and Test Equipment
    a. Test Structures
        i. Parametric Test Structures
        ii. Reliability Test Structures
        iii. Self-Stressing Test Structures
    b. Test Equipment
        i. Packaged Part Testing
        ii. Wafer Level Testing
7. Developing Screens, Stress Tests, and Life Tests
    a. Burn-In
    b. Life Testing
    c. HAST
8. Package Attach (Solder) Reliability
9. Board Level Reliability Mechanisms
10. Calculating Chip and System Level Reliability
11. Future Reliability Challenges

ISTFA 2015
International Symposium for Testing and Failure Analysis

November 1-5, 2015
Oregon Convention Center
Portland, OR, USA

Registration is available at
http://www.asminternational.org/web/istfa-2015

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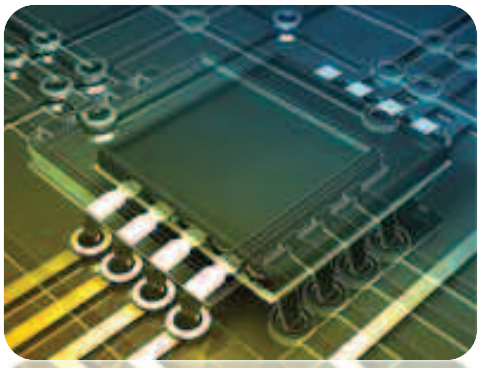
Semitracks will be attending and will be available for meetings. Please contact us at info@semitracks.com to schedule a meeting.



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If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).
To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our web site!
http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Semiconductor Reliability
January 11 – 13, 2016 (Mon – Wed)
San Jose, California, USA

Failure and Yield Analysis
January 18 – 21, 2016 (Mon – Thur)
San Jose, California, USA

Failure and Yield Analysis
May 17 – 20, 2016 (Tue – Fri)
Munich, Germany

EOS, ESD and How to Differentiate
May 23 – 24, 2016 (Mon – Tue)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 30 – June 02, 2016 (Mon – Thur)
Munich, Germany