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Semitracks Monthly Newsletter

Thermal Processing Part II - Oxidation and Kinetics

By Christopher Henderson

Last month we introduced Thermal Processing as a whole, touching briefly on each process. In this newsletter, we will discuss oxidation and kinetics. The fact that silicon readily forms an oxide on its surface has been a key property in the use of silicon in the semiconductor industry. Thermal oxidation is still an important step in many semiconductor and integrated circuit processes. Engineers still use thermal oxidation for most pad oxides and gate oxides, even in a modern integrated circuit process.

Let's discuss some important physical properties of thermally grown silicon dioxide. Most of these properties make the silicon-silicon dioxide system the best material system for semiconductor devices. First, thermal silicon dioxide is amorphous, that is, non-crystalline. Figure 1 shows the bonding structure:

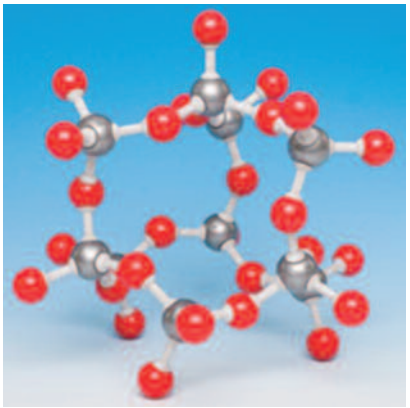

Figure 1. Bonding structure for silicon dioxide.

Silicon dioxide forms a tetrahedral structure with the silicon atom at the center of 4 oxygen atoms. The tetrahedra have no long-range order, whereas in crystalline silicon dioxide, or fused silica, there is

In this Issue:

Page 1	Thermal Processing Part II - Oxidation and Kinetics
Page 4	Technical Tidbit
Page 5	Ask the Experts
Page 6	Spotlight
Page 10	Upcoming Courses

long range order. Thermally grown silicon dioxide is dense, and non-porous, making it a good protection layer during subsequent processing. It is a dielectric, which makes it a good isolation layer. Thermal silicon dioxide exhibits a high electric field breakdown strength, making it one of the best choices for the controlling gate layer in a CMOS transistor. It is not water soluble, so it makes an excellent masking layer. It is chemically stable, which minimizes long-term reliability issues. It has a very high melting point, making it useful for high temperature processing steps. It adheres tightly to the silicon surface, which helps to minimize traps and delamination problems. It creates a stable interface with the silicon that also greatly aids in reliability. It passivates the silicon surface, preventing surface current leakage. And finally, silicon dioxide's properties are radically changed by presence of impurities. For example, if we add boron or phosphorus, we can reduce the reflow temperature of the oxide and modify the etch rate due to different bonding in the tetrahedral structure.

Let's begin with a qualitative view of the reaction kinetics for thermal oxidation. We know that the reactions occur at the silicon-silicon dioxide interface, so this means that the oxidant must diffuse through existing oxide to the interface. Therefore, the thicker the oxide, the more diffusion plays a role. The oxide grows out from the interface, and the interface moves into the silicon as the silicon is consumed like we show in figure 2.

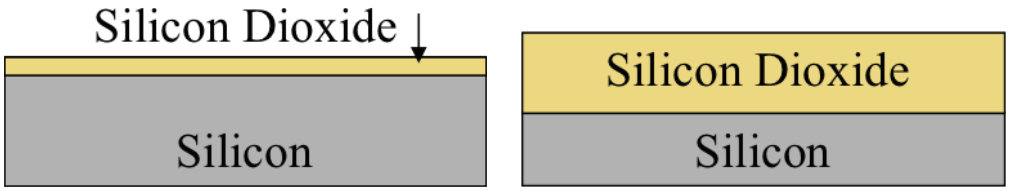

Figure 2. Growth of silicon dioxide: early in the process (left), later in the process (right).

Based on the atomic structure and density of the two materials, to grow 10 nanometers of oxide, we consume 4.4 nanometers of silicon. The oxidation rate is a strong function of the temperature. At room temperature for example, the oxide growth on bare silicon reaches only about 1 nanometer in thickness. Scientists and engineers refer to this as a native oxide. There are two regimes of thermal oxidation: linear and parabolic. In the linear regime, the rate is constant with time since the oxidation is reaction rate limited. In the parabolic regime, the rate decreases with time, since the oxidation process is diffusion-rate limited.

Process engineers use three types of thermal oxidation steps: dry oxidation, wet oxidation, and chlorine-based oxidation. With dry oxidation, the basic reaction is silicon plus oxygen gas produces silicon dioxide. With wet oxidation, silicon plus water vapor produces silicon dioxide and hydrogen gas. This is also called "steam oxidation" or "pyrogenic oxidation". The oxidation rate for wet oxidation is much faster than with dry oxidation, since the OH- (pronounced "O-H-minus") radical from the water molecule diffuses through the silicon dioxide faster than oxygen does. Table 1 shows some of the properties of the oxide given a dry oxidation or a wet oxidation process. In general, oxides grown with a dry oxidation

process exhibit better electrical properties, but these oxides take much longer to grow and require higher temperatures.

Parameter	Dry oxidation	Wet oxidation
Oxidation rate	slow	fast
Density	high	lower
Dielectric strength	high	lower
Dielectric breakdown voltage	high	lower
Etch rate in HF	lower	higher
Application	most oxides	very thick oxides

Table 1. Parameters affecting oxide growth.

A chlorine-based oxidation is a variant of a dry oxidation. Process engineers add chlorine in gaseous form through molecules like dichloroethane or oxalyl (pronounced "oxa-lil") chloride. These types of gas are known as precursors. In this process, the precursor plus oxygen creates free chlorine. This approach can improve the quality of critical oxides like the gate oxide. It can help reduce mobile ion charge, fixed oxide charges, and improve dielectric breakdown strength. Engineers used chlorine-based oxidation extensively before the introduction of nitrided gate dielectrics. This approach also increased the dry oxidation rate, which could lower the thermal budget. Today, engineers mainly use this technique to create a trench liner that can getter, or trap, metals from the chemical mechanical polishing process.

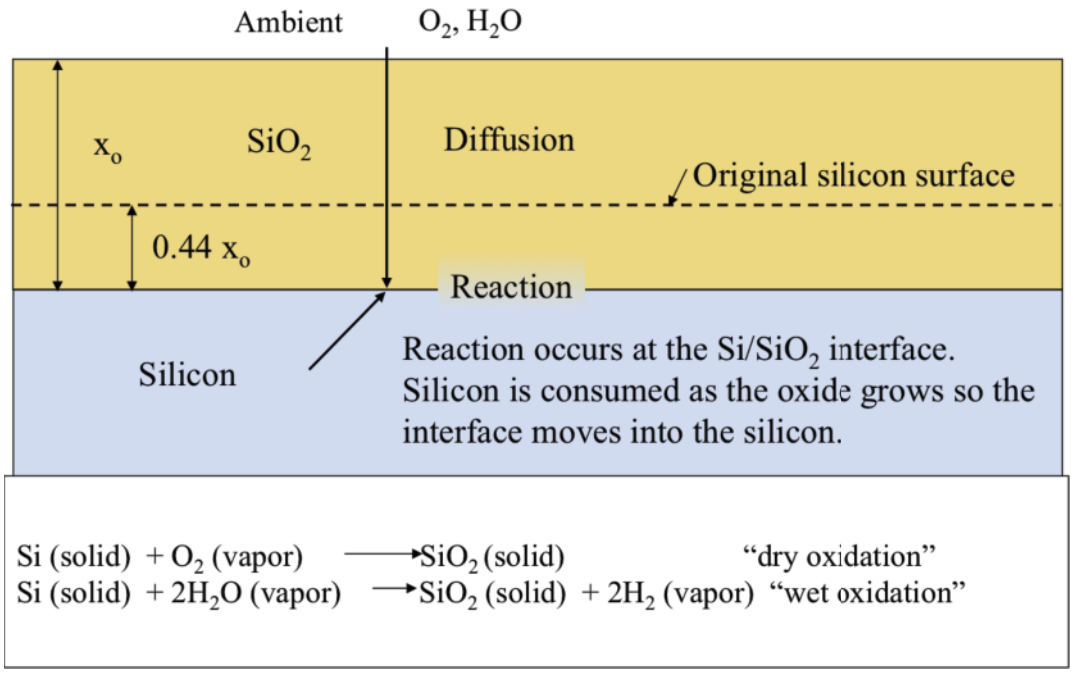

Figure 3. Diagram showing oxide growth process.

Figure 3 shows the oxidation process more closely. Oxygen from the oxygen or steam in the furnace diffuses through the oxide, reaching the silicon surface. Once at the silicon surface, the oxygen or steam reacts with the silicon, producing silicon dioxide. The reaction consumes the silicon, so the silicon/silicon dioxide interface moves into the silicon. As the oxide grows, the original silicon surface is at a point that is 44% of the thickness of the oxide. The reactions for both an oxygen-generated oxide and a steam-generated oxide are shown at the bottom. The steam reaction creates hydrogen gas. Hydrogen is a fast diffuser in silicon dioxide, so it rapidly diffuses out of the oxide.

Technical Tidbit

Leakage in Reverse Biased Junctions

Leakage in reverse biased junctions is an important concept to understand. It plays a key role in the types of applications and use conditions for which we can use silicon circuits. Junction leakage is primarily the result of thermally generated carriers in the depletion region. As carriers are generated, they will be subject to the electric fields present in the depletion region. This will cause electrons to travel toward the N-doped material, since it is positively biased, and holes to travel toward the P-doped material, since it is negatively biased. Figure 1 shows the carrier generation process, and Figure 2 shows the carrier movement after generation. Since leakage current is thermally generated it is exponential with temperature. Leakage currents will double about every eight or ten degrees Celsius in silicon. Silicon "goes intrinsic" at temperatures just above 400C, meaning that the thermally generated carriers actually outnumber doping-generated carriers. Germanium exhibits weaker bonding than silicon and therefore leaks significantly more. For most circuit applications silicon ICs are good to about 150C whereas germanium would only be good to maybe 100C.

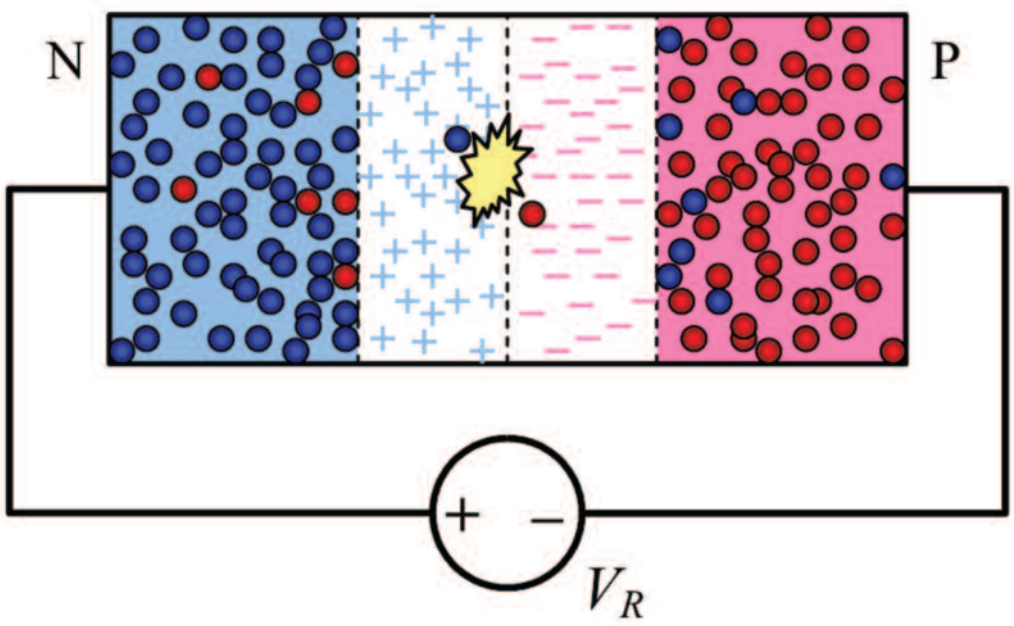

Figure 1. Diagram showing carrier generation.

Not only can heat be a source of carriers, but other mechanisms can generate these carriers. For example, light can do this. If one places an exposed reverse-biased pn junction under a probe station with the lights on, one can see the increase in leakage in the junction. The energetic photons from the light inject enough energy to create some number of electron-hole pairs. Another mechanism that can produce this effect is ionizing radiation.

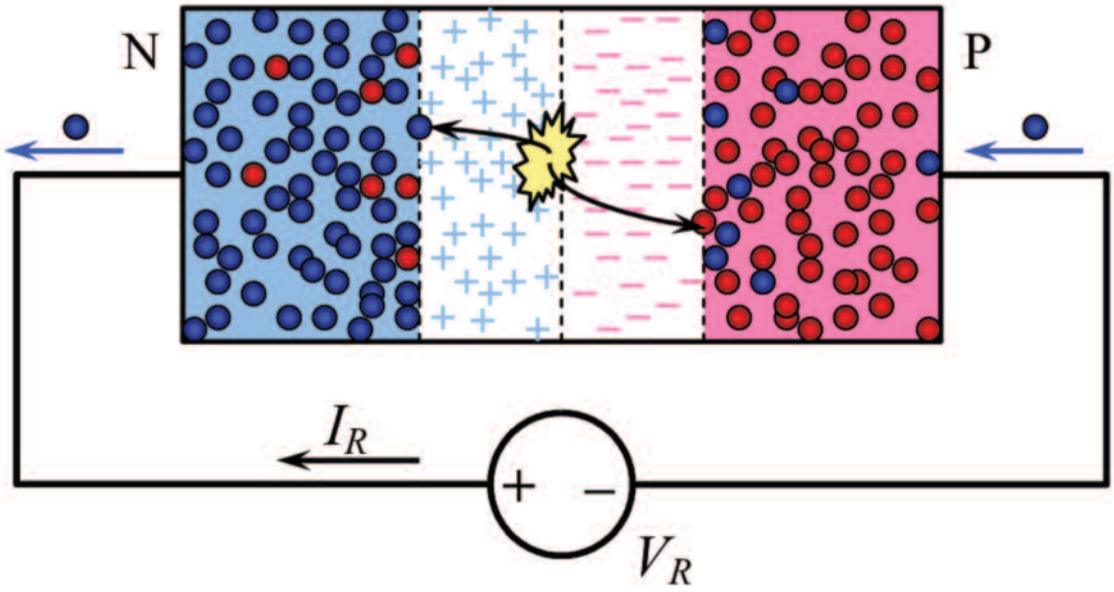

Figure 2. Diagram showing movement of the carriers once they are generated.

The junction leakage is basically independent of the reverse bias. In other words, it does not increase as the electric field increases, but rather remains relatively constant. Temperature is the main effect.

Ask the Experts

Q: What is the near-threshold voltage computing?

A: Near-threshold voltage computing is a technique for operating transistors at lower voltages to try and minimize the power-switching product. As one operates at lower voltages, the switching speed goes down, but the power goes down even more so. This effect ends as the power supply approaches the sum of the n-channel and p-channel threshold voltages of the transistors though. Researchers are looking into applications for this technique as it may facilitate low levels of processing while saving power.

Rob Aitken of ARM discusses this technique in more detail in this presentation:

Part I https://www.youtube.com/watch?v=Ersdl81yTnM

Part II https://www.youtube.com/watch?v=lvfu54_JwEg

Spotlight: Product Qualification

OVERVIEW

Package reliability and qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can also involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. In particular, the proliferation of new package types can create difficulties. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. Customers expect fast, smooth qualification, but incorrect assumptions, use conditions, testing, calculations, and qualification procedures can severely impact this process. Your company needs competent engineers and scientists to help solve these problems. ***Product Qualification*** is a two-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor technology and product qualification. This course is designed for every manager, engineer, and technician concerned with qualification in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

Participants learn to develop the skills to determine the best process for qualification, how to identify issues and how to resolve them.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions and relationship to qualification.
2. **Failure Mechanisms.** Participants learn how product qualification and failure mechanisms relate to one another. We provide an overview of these mechanisms. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, EOS, ESD, latchup, drop tests, etc.
3. **Qualification Principles.** Participants learn how test structures can be designed to help test for a particular failure mechanism.
4. **Test Strategies.** Participants learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to qualify today's components.
2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.
3. The seminar will identify major failure mechanisms; explain how they are observed, how they are modeled, and how they are handled in qualification.

4. The seminar will discuss the major qualification processes, including JEDEC JESD47, AEC Q-100, MIL-STD, and other related documents.
5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.
6. Participants will be able to knowledgeably implement additional tests that are appropriate to assure the reliability of a component.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

COURSE OUTLINE

1. Introduction to Reliability
   a. Basic Concepts
   b. Definitions
   c. Historical Information
2. Statistics and Distributions
   a. Basic Statistics
   b. Distributions (Normal, Lognormal, Exponent, Weibull)
   c. Which Distribution Should I Use?
   d. Acceleration
   e. Number of Failures
3. Overview of Die-Level Failure Mechanisms
   a. Time Dependent Dielectric Breakdown
   b. Hot Carrier Damage
   c. Negative Bias Temperature Instability
   d. Electromigration
   e. Stress Induced Voiding

4. Overview of Package Level Mechanisms
    a. Ionic Contamination
    b. Moisture/Corrosion
    c. Thermo-Mechanical Stress
    d. Interfacial Fatigue
    e. Thermal Degradation/Oxidation
    f. Solder Joint Reliability
5. Overview of Board Level Reliability
    a. Solder Joint Reliability
    b. EOS/ESD/LatchUp
    c. Single Event Effects

Day Two (Lecture Time 8 Hours)

6. Test Structures and Test Equipment
7. Developing Screens, Stress Tests, and Life Tests
    a. Burn-In
    b. Life Testing
    c. HAST
    d. JEDEC-based Tests
    e. Exercises
8. Developing a Qualification Program
    a. Process
    b. Standards-Based Qualification
    c. Knowledge-Based Qualification
    d. MIL-STD Qualification
    e. JEDEC Documents (JESD47H, JESD94, JEP148)
    f. AEC-Q100 Qualification
    g. When do I deviate? How do I handle additional requirements?
    h. Exercises

Semitracks will exhibit at this year's International Symposium for Testing and Failure Analysis. Please stop by and see us (booth 725). Call us at 1-505-858-0454 or email us at info@semitracks.com to schedule.

40th Annual International Symposium for Testing and Failure Analysis

Conference and Exposition

November 9 – 13 • Houston, Texas
Stop by and see us!
For more information on the symposium, visit
http://www2.asminternational.org/content/Events/istfa
Please feel free to contact us to set up an appointment while you are there!

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).

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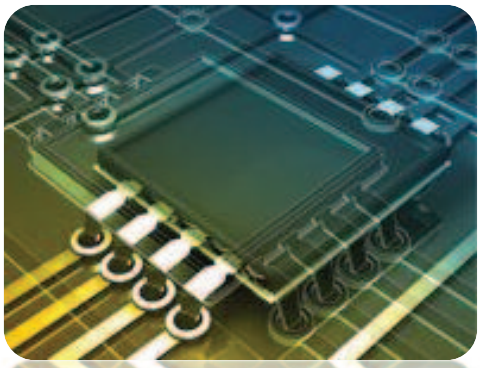

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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To post, read, or answer a question, visit our forums.
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Upcoming Courses

(Click on each item for details)

Product Qualification

January 26 – 27, 2015 (Mon – Tue)
San Jose, California, USA

Wafer Fab Processing

January 26 – 29, 2015 (Mon – Thur)
San Jose, California, USA

EOS, ESD and How to Differentiate

January 28 – 29, 2015 (Wed – Thur)
San Jose, California, USA