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INFOTRACKS

YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Semiconductor Cleanroom Technology

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In this month's Feature Article, we will continue our discussion of Semiconductor Cleanroom Technology by introducing the topic of storage and delivery of Process Chemicals and Gases in a Cleanroom. When constructing a new cleanroom facility, one must pay close attention to the type and volume of Process Chemicals and Gases that one plans to use in the fabrication process. This will play a key role in locating the Chemical and Gas storage areas, planning and implementing the delivery system, and determining safety requirements. We will discuss these topics further in this article.

Let's begin by discussing Process Chemicals. This includes chemicals like the RCA Clean, photoresists, developers, and wet etchants. These Chemicals require exceptionally high purity. For example, at the 28 nm technology node and below, engineers use SEMI Grade 4 or VLSI Grade, which typically corresponds to less than 0.1 parts per billion trace metals. Furthermore, the tools that utilize these Chemicals may also have point-of-use ultra-filtration. There are two main methods of supply: bulk Chemical delivery and point-of-use chemical generation. With bulk chemical delivery, the Chemicals are pumped to the process tools from bulk tanks. These systems use continuous re-circulation and filtration, but the delivery system is a large potential source of contamination due to bacterial growth, and organic

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- Advanced CMOS/FinFET Fabrication

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carbon. With point-of-use Chemical generation, ultra-pure anhydrous gases are mixed with ultra-pure water at the point-of-use. One can achieve a much higher level of chemical purity, and it reduces handling logistics. These systems can be quite expensive though. Here, the contamination concerns include particles and metallics, like the transition metals, such as iron, nickel, chromium, gold, and copper; and the alkali metals like sodium, potassium, calcium and magnesium.

Most specialty chemicals do not require fab-wide distribution, since they are used in smaller quantities. However, they still require proper storage and disposal in the fab environment. First and foremost, Chemicals need to be labeled properly. The transportation and storage of chemicals is based on hazard levels. The graphic on the left of Figure 1 shows the National Fire Protection Agency, or NFPA labels that are used in conjunction with the transportation and storage of Chemicals. This is the oldest standardized method for identifying chemicals. Today, however, these are primarily used for quick identification by emergency personnel, should a leak, fire or explosion occur in the fab environment. The more current approach to labeling is to use the Globally Harmonized System, or GHS labels. We show an example of a GHS label on the right of Figure 1. The GHS requirements are prevalent across various industries to meet global regulatory labeling and tracking challenges. Although it is common, there is some confusion about what GHS is exactly. Very briefly, GHS allows companies across the globe to have one common, coherent framework for classifying and communicating information related to chemicals. GHS requirements apply to both labels and safety data sheets. Each chemical type will have a storage requirement based on its label. The storage requirements might include engineering barriers to protect against explosion or fire, as well as barriers to protect against exposure to toxic chemicals. There may also be personnel access restrictions and procedural restrictions to provide additional safety and protection.

Figure 1- (Left) NFPA Label, and (right) GHS label.

The next topic is Process Gases. Today, most fab processing is performed with Gases rather than chemicals. This includes Gases for thermal oxidation, chemical vapor deposition, and dry etching. There are two main categories of Gases: Bulk Gases and Specialty Gases. Bulk gases include Gases like nitrogen, oxygen, hydrogen and argon. These are produced on-site or at a nearby Gas plant, like we show in the image on the left side of Figure 2. They are piped directly to the process tools. Specialty Gases are delivered to gas cabinets in pressure vessels, or gas bottles, like we show in the image on the right side of Figure 2. Most etch gases are

delivered this way. The contaminants of concern include particles, metallics, and water. The purity level is usually specified as a percentage, for example 99.9999% pure. The piping to the process tools is critical as contaminants can be introduced through poor or improper welding, or contaminated plumbing materials. Some tools may also have point-of-use ultra-filtration, like we mentioned with chemicals.

Figure 2- (Left) Gas plant, and (right) Specialty Gases.

Table 1 shows a list of major Gases used in a cleanroom environment. We show the primary applications; source of the gases; typical volumes of the Gases needed in advanced processes in normal cubic meters per hour; and the type of supply system for the Gas. We show values for two different types of fabs: a 3-dimensional NAND flash memory cleanroom facility with 300,000 wafer starts per month, or 300 kwspm, and a leading-edge foundry cleanroom facility with 60,000 wafer starts per month. Gases that are common in our atmosphere, like nitrogen, oxygen, and argon, can be generated by air separation techniques at the central utility plant itself, or they can be piped in from a remote location where the air separation facility resides. For lower volume fabs, these Gases can also be delivered through bulk delivery and stored in a tank onsite. Other Gases that require extraction, chemical synthesis, or capturing by-products from reactions, are typically delivered using ISO containers.

Gas	Nitrogen (N_2)	Oxygen (O_2)	Argon (Ar)	Hydrogen (H)	Helium (He)	Carbon Dioxide (CO_2)	Bulk specialty Gases
Primary Application	Inerting and purging	Oxidation reactions for deposition and etch	Plasma and high-temperature inerting	Annealing, epitaxy, deposition, and etch	Cooling, plasma, and carrier gas	Cleaning, immersion lithography, DI water conditioning	Deposition, etch, epitaxy, chamber cleaning
Sources	Air separation	Air separation	Air separation	Hydrocarbon steam reforming or electrolysis	Extraction from natural gas deposits	By-product from production of ammonia, others	Chemical synthesis
Typical supply volume (Nm^3/h)[1]							
3D NAND (300 kwspm)[2]	80,000 – 100,000	2000 - 3000	50 - 100	200 - 400	50 - 150	25 - 50	Varies
Leading-edge foundry (60 kwspm)[2]	30,000 – 50,000	200 - 300	150 - 250	500 – 1,500	25 - 50	100-200	Varies
Supply systems							
On-site generation or pipeline	X	X	X	X			
Bulk delivery + tank	X	X	X	X		X	
ISO container					X	X	X

Table 1- List of major Gases used in a cleanroom environment.
Notes: [1] Normal cubic meters per hour, [2] 000's of wafer starts per month

Gas storage onsite often involves the storage of Gases in liquid form, since the liquid form of the Gas occupies much less volume. These liquids can be placed in the storage tank through either a top or bottom fill valve, depending on the type of Gas. These tanks are essentially just large "Dewar" vessels having an inner vessel that contains the cryogenic liquid encased in an outer shell with a high vacuum between the inner vessel and the outer shell. Vacuum is the best possible insulation to maintain the liquid at cryogenic temperatures. Cryogenic tanks are typically filled from the top using the blow down method. The blow down method is when the pressure of the tank is reduced by blowing out the head pressure of the tank in order to fill it. However, blowing down a tank wastes Gas, and in turn, costs money. But the most critical problem is that top filling also requires taking the tank offline, or not to be used while it is being filled because the tank can't maintain its pressure, which would cause the fab cleanroom facility using the tank to shut down and stop their operation during filling. The bottom fill method keeps the pressure up, allowing the user to keep the fabrication equipment online and running. Some systems are designed to maintain the required pump pressure to keep operating. In these systems, the top and bottom filling method does not require a tank to be blown down, and therefore, prevents loss of the Gas during the filling process. Cryogenic tanks also include an ambient air vaporizer. Ambient air vaporizers are designed especially for maintaining pressure in bulk cryogenic liquid tanks. Cryogenic liquid from the bottom of the bulk storage tank feeds the Gas vaporizer which returns vapor to the top of the tank. The low pressure drop through the vaporizer will ensure tank pressure is maintained during draw-off operations. These Gas vaporizers use natural convection of air to vaporize liquefied Gases. Finned aluminum tubes absorb heat from the ambient air and transfers that heat to produce Gas. We show a diagram of this configuration in Figure 3.

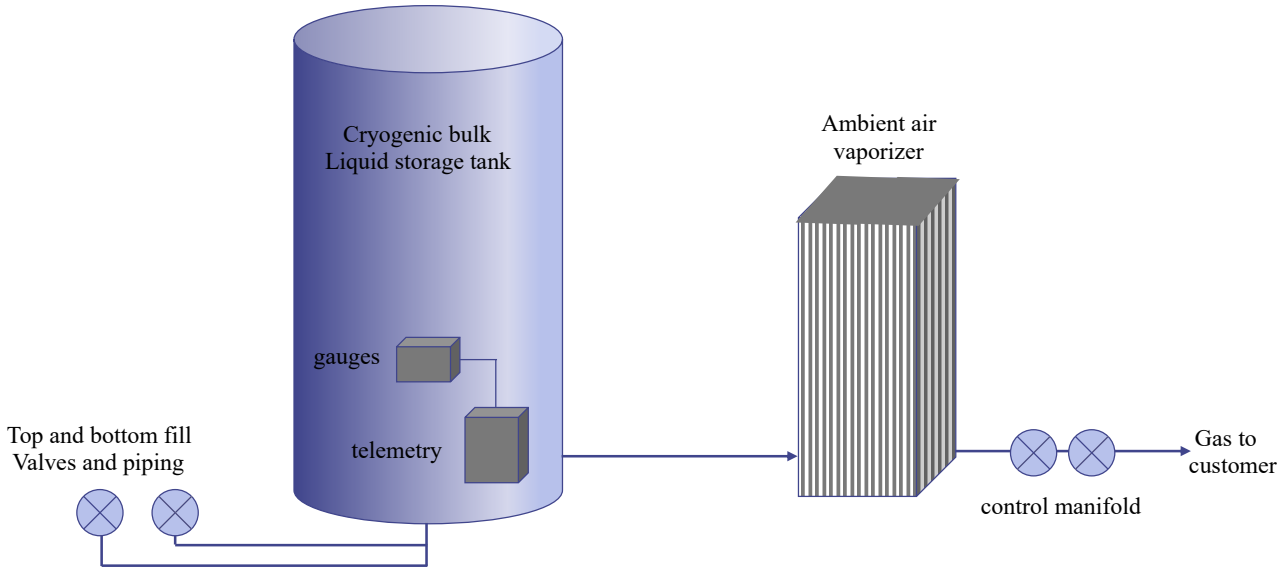

Figure 3- Typical Gas Storage and Delivery configuration for a cleanroom facility.

In next month's Feature Article, we will continue our discussion of the storage and delivery of Process Chemicals and Gases in a Cleanroom by discussing the individual Gases typically used in a Semiconductor Cleanroom environment.

Technical Tidbit: ATE High Speed Digital Instrumentation

This month's Technical Tidbit concludes our short series on Automated Test Equipment (ATE) Instrumentation. In this month's Tidbit, we will introduce ATE High Speed Digital instrumentation. Test engineers use this type of instrumentation in an ATE system to supply a variety of patterns, as well as voltage and current values to a Device Under Test (DUT) in the course of testing integrated circuits.

Digital instruments have dedicated hardware functionality for source and capture of digital data, including digital data representations of analog waveforms. Digital instruments can generate and receive these data types at multiple voltage levels, under different timing conditions, and be controlled on device pins that are input only, output only, I/O (input and output), single-ended or differential.

Figure 1 shows a block diagram of a typical High-Speed Digital, or HSD, subsystem. The backplane, shown on the left, serves as the core of an HSD instrument. The pattern generator hardware connects directly to the backplane. The Large Vector Memory (LVM) typically holds the patterns, while the Small Vector Memory (SVM) holds the Opcodes for the Alternate Data Source Selection sub-block. The SVM also communicates with the Memory Test Option (MTO) sub-block, communicating instructions to the sub-block. The SVM also communicates with the Digital Signal Source Capture, or DSSC, module. Each pin will typically have a Per Pin Measurement Unit, or PPMU, that can detect voltage and current values at a given pin. It is typically switched into the circuit near the Pogo pins on the tester. Digital testers typically include hardware to drive voltage values to measure the input high level voltage and the input low level voltage, denoted as VIH and VIL respectively. Digital testers also typically include load circuit hardware to source or sink current to measure output high level leakage current and output low level leakage current, denoted as IOH and IOL respectively. The detector allows the measurement of both output high level voltage and output low level voltage, denoted as VOH and VOL respectively. Finally, the data from the detector is collected in the History Random Access Memory, where it can be then sent to the main computer through the backplane.

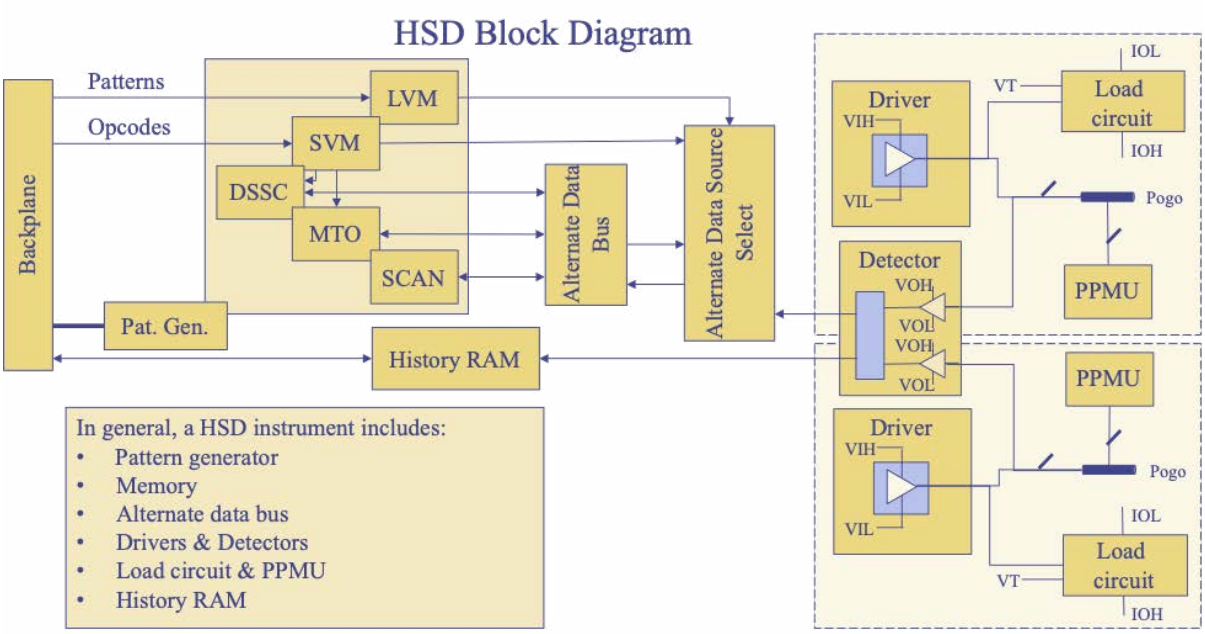

Figure 1- Block diagram of a High-Speed Digital (HSD) subsystem.

This concludes our short series on ATE instrumentation. Stay tuned for other topics in future issues.

Ask The Experts

Q: In your class on IC Packaging Design and Modeling, you mentioned that there are software products used in reliability stress testing. Do these software products use Failure Modes and Effects Analysis (FMEA) as a type of solution for stress testing?

A: Thanks for your question. There are elements of Design and Process FMEA within reliability work, but there is also an increasing use of use-condition models and warranty requirements. This tends to be the case with high-volume, high-value products, like microprocessors, Graphical Processing Units (GPUs), etc. There is not as much cost benefit for lower-value products to do this though.

Course Spotlight:ADVANCED CMOS/FINFET FABRICATION

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" Advanced CMOS/FinFET Fabrication is a 1.5-day course that offers detailed instruction on the processing used in a modern integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By concentrating on the latest developments in CMOS and FinFET technology, participants will learn why FinFETs are fast becoming the technologies of choice at feature sizes below 20nm. Our instructors work hard to explain semiconductor processing without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants learn basic but powerful aspects about CMOS fabrication and FinFET technology. This skill-building series is divided into four segments:

1. Front End Of Line (FEOL) Overview. Participants study the major developments associated with FEOL processing, including Ion Implantation, Rapid Thermal Annealing (RTA) for implants and silicides, and Pulsed Plasma Doping. They also study alternate substrate technologies like SOI as well as High-k/Metal Gates for improved leakage control.

2. Back End Of Line (BEOL) Overview. Participants study the major developments associated with BEOL processing, including copper metallization and Low-k Dielectrics. They learn about why they're necessary for improved performance.

3. FinFET Manufacturing Overview. Participants learn how semiconductor manufacturers are currently processing FinFET devices and the difficulties associated with three-dimensional structures from a processing and metrology standpoint.

4. FinFET Reliability. They also study the failure mechanisms and techniques used for studying the reliability of these devices.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of Bulk technology, SOI technology and the technical issues.

2. Participants will understand how Hi-K/Metal Gate devices are manufactured.

3. Participants will also understand how FinFET devices are manufactured.

4. The seminar provides a look into the latest challenges with copper metallization and Low-k dielectrics.

5. Participants will understand the difficulties associated with non-planar structures and methods to alleviate the problems.

6. Participants will be able to make decisions about how to evaluate FinFET devices and what changes are likely to emerge in the coming years.

7. Participants will briefly learn about IC reliability and the failure modes associated with these devices.

8. Finally, the participants see a comparison between FinFETs and new alternatives (such as Gate All Around (GAA) structures and nanosheets).

COURSE OUTLINE – Lecture Time 12 Hours

1. Advanced CMOS Fabrication – Introduction

2. Front End Of Line (FEOL) Processing
   a. SOI and FD-SOI
   b. Ion Implantation and Rapid Thermal Annealing
   c. Pulsed Plasma Doping
   d. Hi-K/Metal Gates
   e. Processing Issues
      i. Lithography
      ii. Etch
      iii. Metrology

3. Back End Of Line (BEOL) Processing
   a.Introduction and Performance Issues
   b.Copper
      i.Deposition Methods
      ii.Liners
      iii.Capping Materials
      iv.Damascene Processing Steps
   c.Lo-k Dielectrics
      i.Materials
      ii.Processing Methods
   d.Reliability Issues

4. FinFET Manufacturing Overview
   a.Substrates
      i.Bulk
      ii.SOI
   b. FinFET Types
   c.Process Sequence
   d.Processing Issues
      i.Lithography
      ii.Etch
      iii.Metrology

5. FinFET Reliability
   a.Defect density issues
   b.Gate Stack
   c.Transistor Reliability (BTI and Hot Carriers)
   d.Heat dissipation issues
   e.Failure analysis challenges

6. Future Directions for FinFETs
   a.Comparison of FinFETs and other Techniques (GAA, Nanosheets) – Are FinFETs a better choice?
   b.Scaling

Upcoming Courses:

Public Course Schedule:

IC Packaging Technology - January 23-24, 2024 (Tues.-Wed.) | Phoenix, Arizona - $1,295

Advanced CMOS/FinFET Fabrication - January 29-30, 2024 (Mon.-Tues.) | Phoenix, Arizona - $995

Wafer Fab Processing - February 26-29, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095

Failure and Yield Analysis - March 4-7, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095

Semiconductor Reliability and Product Qualification - March 11-14, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095

Defect-Based Testing - March 20-21, 2024 (Wed.-Thurs.) | Munich, Germany - $1,195

Have an idea for a course? If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please email us at info@semitracks.com

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!