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Semitracks Monthly Newsletter

Photonics Device Fundamentals

By Christopher Henderson

In this month's feature article, we will continue our series on photonics device fundamentals. This is the third in a series of four articles. This month we discuss the behavior of the pn junction diode.

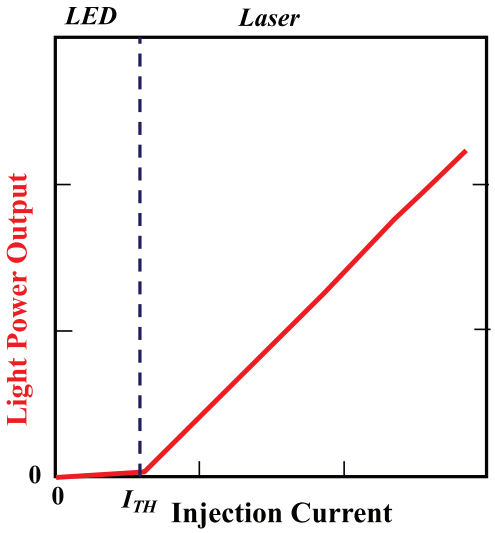


Figure 18. Optical emission vs. injection current.

This graph in Figure 18 shows the optical emission versus the injection current in both LED and laser diode devices. In the LED operating range, the light power output is quite limited. However,

In this Issue:

once the current exceeds the threshold current, the light output increases significantly. Lasing action begins above the threshold due to the stimulated emission.

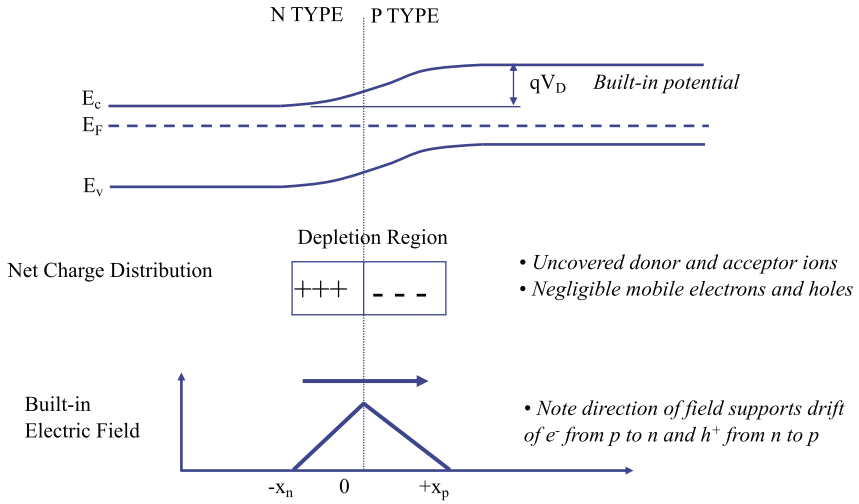


Figure 19. Illustration of pn junction with no external bias.

As a review, let's begin by discussing the pn junction with no external bias. We show the energy band diagram for the pn junction here in Figure 19. The difference in the conduction band height from the n-type to the p-type material represents the built-in potential of the junction. At the interface between the n- and p-type semiconductor there will be a depletion region, where there is fixed positive and negative charge in the dopant atoms, and negligible free carriers. The separation of the fixed positive and negative charge leads to a built-in electric field. The direction of the electric field vector will be from left to right in this configuration, supporting the drift of electrons to the left, and the drift of holes to the right.

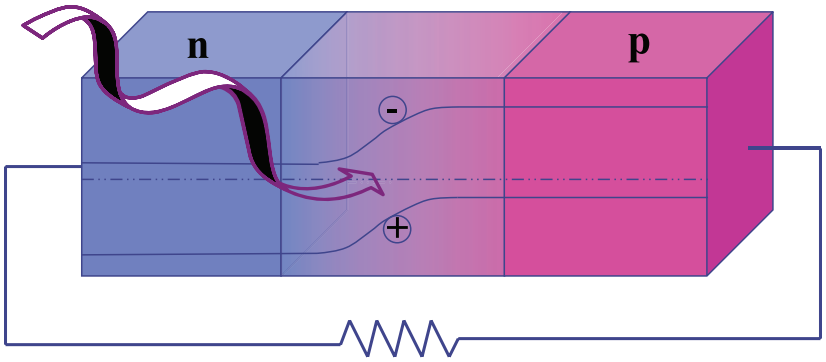


Figure 20. Energy from light causes separation of holes and electrons.

One important aspect of the pn junction is that it creates a separation of holes and electrons. The band structure ensures energy separation and the built-in field forces a physical separation of the carriers. When light hits the junction, it can create an electron-hole pair, where the electron will go to the left, and the hole to the right in this pn junction orientation in Figure 20.

$$J_n = qn_{p0}\left[\exp\left(\frac{qV_{app}}{kT}\right) - 1\right]\sqrt{\frac{kT\mu_n}{q\tau_n}}$$

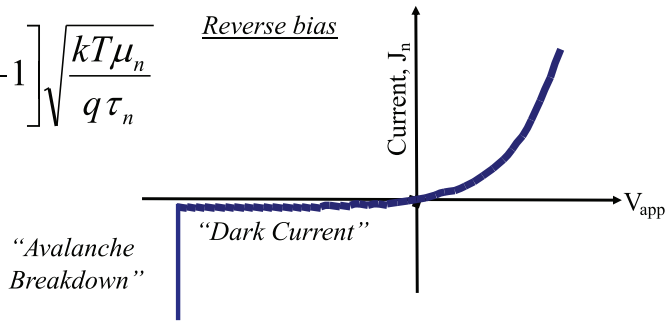
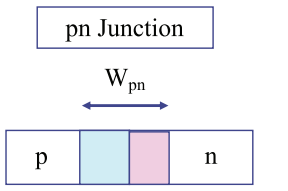


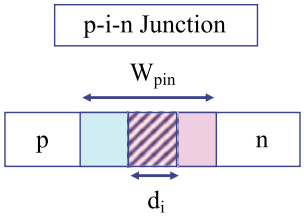
Figure 21. Ideal diode electron current equation.

Here in Figure 21, we show the ideal diode electron current equation. In the forward bias condition, the current density is exponentially related to the forward voltage across the junction. In the reverse bias condition, the current density is related to the temperature, the mobility, the lifetime and the doping concentration on the more lightly-doped side of the pn junction in the silicon. If the electric field is high enough, the pn junction enters a region called avalanche breakdown. We will discuss that property shortly, as this condition can be used for a few optoelectronics applications.



Pin Has Larger Depletion Region
(improves quantum efficiency)

$$\frac{W_{pin}}{W_{pn}} = \sqrt{1 + \frac{d_i}{W_{pn}}}$$



Pin Has Smaller Capacitance
(improves frequency response)

$$\frac{C_{pin}}{C_{pn}} = \frac{W_{pn}}{W_{pin}}$$

Figure 22. Intrinsic layer improves key quantities.

As shown in Figure 22, one improvement to the pn junction diode is the p-i-n diode (also denoted as pin diode). The pin diode has an intrinsic region in between the p and n regions. This increases the size of

the depletion region, which in turn improves the quantum efficiency of the diode. Furthermore, the larger depletion region produces a smaller junction capacitance, which improves the frequency response.

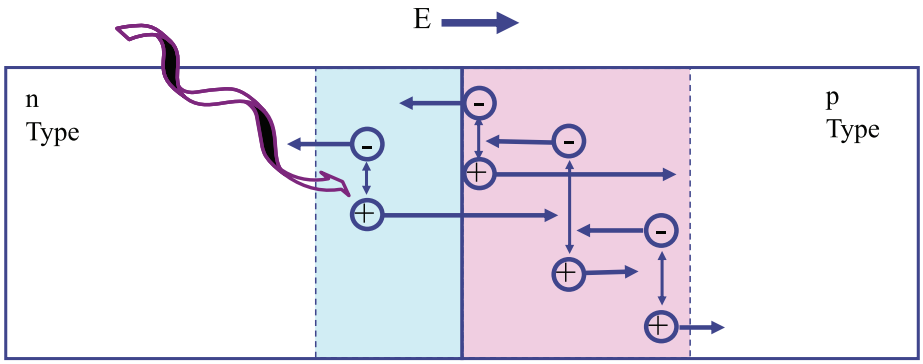


Figure 23. Illustration of avalanche multiplication.

Avalanche multiplication can be used for increasing the sensitivity of a detector. If we bias the transistor such that the electric field is high enough to initiate the avalanche multiplication process, then an incoming photon can trigger the initial carriers, kicking off the avalanche process, like we show here in Figure 23. However, if the applied field is too high, then avalanche multiplication can lead to junction breakdown and possible damage.

Next month, we will continue with part four in the series.

Technical Tidbit

Environmentally Friendly Cleaning Techniques

In this month's technical tidbit, we will briefly cover environmentally friendly wafer cleaning techniques. One of the big problems with cleaning wafers is the amount of chemicals one needs to use.

Figure 1. Ozonated De-ionized Water Cleaning System.

As the semiconductor industry comes under increasing pressure from environmental regulations, researchers have also been developing etches that are more 'environmentally friendly.' One such cleaning method is to use ozonated de-ionized water. This cleaning procedure eliminates the need for ammonium hydroxide, hydrochloric acid, and hydrogen peroxide, which in turn reduces environmental hazards. The biggest drawback to this etch is that it is not as aggressive in removing contaminants. Figure 1 shows an image of an ozonated de-ionized water cleaning system. Another class of techniques that is becoming more important is vapor phase cleaning. The benefit of vapor phase cleaning is that one can drastically reduce chemical use, since a given volume of a gaseous phase requires much less chemical than the liquid phase. One chemical that is used quite often in vapor phase cleaning is anhydrous hydrofluoric acid. Engineers also use hydrofluoric acid and water vapor for cleaning as well. Vapor phase cleaning works well for silicide layers. It also works well as an etch for the sacrificial oxide layer just prior to gate oxide growth.

Figure 2. Cryo-aerosol Cleaning Tool.

Dry cleaning is also gaining popularity in semiconductor manufacturing. In dry cleaning, one uses high velocity ice particles to dislodge particles on the surface. Materials such as dry ice and frozen argon are used. The aerosol removes the particles on the surface through the expansion and/or contraction of the aerosol particles. Cryo-aerosol cleaning helps eliminate hazardous chemicals altogether. Figure 2 shows a state-of-the-art cryo-aerosol cleaning tool made by Eco-Snow Systems.

Ask the Experts

Q: I read about the "Origin of 0/77" with some interest; however, I got confused because as far as I know my company never uses a sample size of 77 for either stress-based and non-stress-based qualifications—in fact, the sample size could be in the thousands. Does 0/77 apply only when stress is going to be applied? Could you please provide some clarification as to what this sample size of 77 means in theory and practice?

A: For many of today's ICs, a sample size of 77 units is not going to be sufficient to demonstrate really low defect levels (down in the single DPPMs, for instance). Quite often, you will see people use larger sample sizes, such as 231, 1000, 1669, or other values. The larger the number, the higher the confidence one can have in the results. JEDEC tests use the sample size of 77 units to ensure you have qualification lots that fit into certain criteria. This sample size is enough to ensure that lots with greater than 3% defects will be rejected from the testing conditions. What you don't want to happen is a situation during qualification testing where you choose, let's say, 10 samples, and it turns out they're all good, when in reality there are an unacceptable number of bad devices within the wafer lot.

Spotlight: Advanced CMOS/FinFET Fabrication

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?"

Advanced CMOS/FinFET Fabrication is an online course that offers detailed instruction on the processing used in a modern integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

What Will I Learn By Taking This Class

By concentrating on the latest developments in CMOS and FinFET technology, participants will learn why FinFETs and FD-SOI are fast becoming the technologies of choice at feature sizes below 20nm. Our instructors work hard to explain semiconductor processing without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants learn basic but powerful aspects about FinFET technology. This skill-building series is divided into four segments:

1. Front End Of Line (FEOL) Overview. Participants study the major developments associated with FEOL processing, including ion implantation, Rapid Thermal Annealing (RTA) for implants and silicides, and Pulsed Plasma Doping. They also study alternate substrate technologies like SOI as well as High-k/Metal Gates for improved leakage control.
2. Back End Of Line (BEOL) Overview. Participants study the major developments associated with BEOL processing, including copper metallization and Low-k Dielectrics. They learn about why they're necessary for improved performance.
3. FinFET Manufacturing Overview. Participants learn how semiconductor manufacturers are currently processing FinFET devices and the difficulties associated with three-dimensional structures from a processing and metrology standpoint.
4. FinFET Reliability. They also study the failure mechanisms and techniques used for studying the reliability of these devices.

COURSE OBJECTIVES

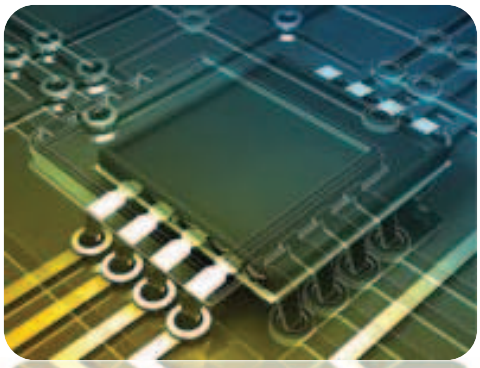
1. The seminar will provide participants with an in-depth understanding of SOI technology and the technical issues.
2. Participants will understand how Hi-K/Metal Gate devices are manufactured.
3. Participants will also understand how FinFET devices are manufactured.
4. The seminar provides a look into the lastest challenges with copper metallization and Low-k dielectrics.

5. Participants will understand the difficulties associated with non-planar structures and methods to alleviate the problems.
6. Participants will be able to make decisions about how to evaluate FinFET devices and what changes are likely to emerge in the coming years.
7. Participants will briefly learn about IC reliability and the failure modes associated with these devices.
8. Finally, the participants see a comparison between FD-SOI (the leading alternative) and FinFETs.

COURSE OUTLINE

1. Advanced CMOS Fabrication – Introduction
2. Front End Of Line (FEOL) Processing
    a. SOI and FD-SOI
    b. Ion Implantation and Rapid Thermal Annealing
    c. Pulsed Plasma Doping
    d. Hi-K/Metal Gates
    e. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology
3. Back End Of Line (BEOL) Processing
    a. Introduction and Performance Issues
    b. Copper
        i. Deposition Methods
        ii. Liners
        iii. Capping Materials
        iv. Damascene Processing Steps
    c. Lo-k Dielectrics
        i. Materials
        ii. Processing Methods
    d. Reliability Issues
4. FinFET Manufacturing Overview
    a. Substrates
        i. Bulk
        ii. SOI
    b. FinFET Types
    c. Process Sequence
    d. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology

5. FinFET Reliability
   a. Defect density issues
   b. Gate Stack
   c. Transistor Reliability (BTI and Hot Carriers)
   d. Heat dissipation issues
   e. Failure analysis challenges
6. Future Directions for FinFETs
   a. Comparison of FD-SOI and FinFETs – Are FinFETs a better choice?
   b. Scaling



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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.

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To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Semiconductor Reliability / Product Qualification
April 6 – 9, 2021 (Tue – Fri)
Munich, Germany

Wafer Fab Processing
April 6 – 9, 2021 (Tue – Fri)
Munich, Germany

Failure and Yield Analysis
April 12 – 15, 2021 (Mon – Thur)
Munich, Germany

IC Packaging Technology
April 19 – 20, 2021 (Mon – Tue)
Munich, Germany

Advanced CMOS/FinFET Fabrication
April 22, 2021 (Thur)
Munich, Germany