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Evaporation

By Christopher Henderson

This short section will discuss a historical technique for metal deposition known as evaporation. We present this topic mainly for completeness, although some experimental processes might utilize this method of deposition even today.

Evaporation was the earliest method for depositing metal conductors on semiconductor devices. Evaporation is a highly directional process; the evaporated atoms travel in a straight line to the wafer surface. This can lead to problems such as step coverage. Evaporation also produces small grain sizes. This is a concern with regard to both stress induced voiding and electromigration. Atom movement occurs more readily along grain boundaries; therefore, the smaller the grain sizes, the more grain boundaries are present, and greater the potential for atom movement, which is the physical process associated with electromigration and stress voiding.

There are two types of evaporation systems used in semiconductor applications: the filament evaporation system and the electron beam evaporation system (Figure 1). In a filament-based evaporation system, the filament is heated to boil off the material. The evaporated material will coat the wafers, and everything else inside the chamber. In an electron beam evaporation system, an electron beam gun accelerates electrons toward the evaporation target. The electrons impart energy to the target in the form of heat. As the target heats up, the material is

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evaporated. Like the filament evaporation system, the material will deposit on the wafers and everything else in the chamber.

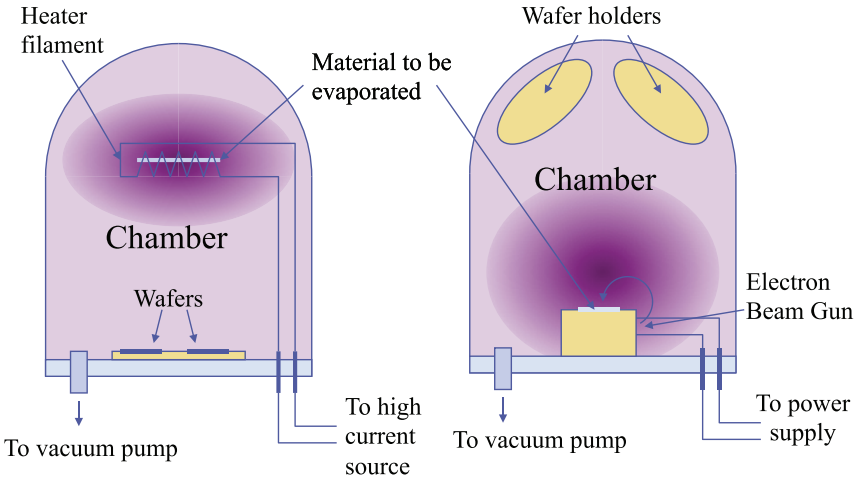
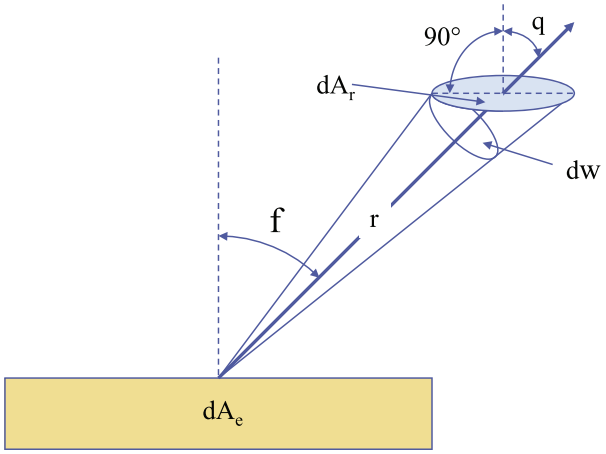


Figure 1. Filament and electron beam evaporation systems.

Deposition in an evaporation system is heavily dependent on the angle of deposition (Figure 2). Since the atoms that comprise the thin film travel in a straight line, the deposition rate is a function of the cosine of the angle. The larger the angle, the slower the deposition process will be. For this reason, most evaporation systems are constructed such that each wafer is perpendicular to the target.



Angular relationship between the substrate and source. Areas of the source and the substrate are dA_e and dA_r. dW is the solid angle of the cone shown.

Figure 2. Cosine law of deposition and relationship between source and substrate.

Evaporation systems suffer from several different problems. First, the deposition rate and film thickness cannot be precisely controlled. As we discussed earlier, the cosine law means that one cannot achieve a uniform thickness. Second, evaporation is not a suitable method for depositing compounds. Most aluminum metal systems have a few percent copper added to increase resistance to

electromigration. Third, step coverage can be rather poor due to the line of sight path that the atoms travel. Some systems alleviate this problem by moving and rotating the wafers during the evaporation process; however, this increases the mechanical complexity of the system and decreases its reliability. Finally, one can damage the wafers from radiation associated with the electron gun. The high accelerating voltage can cause threshold voltages to shift on sensitive MOS devices.

The scanning electron microscope image in Figure 3 shows an example of evaporated metal. We removed the overlying dielectric with a wet chemical etch to help delineate the grain boundaries. Note that the grains are quite small. Also note that there are significant gaps in the grain boundaries in this segment of metal. This is caused by a failure mechanism known as stress induced voiding, or stress migration. This phenomenon is more common in evaporated metal, since the smaller grains provide numerous grain boundaries through which the aluminum atoms can migrate. This is another disadvantage of evaporated metal: it suffers from reliability issues. As such, the semiconductor industry has mostly moved away from this deposition.

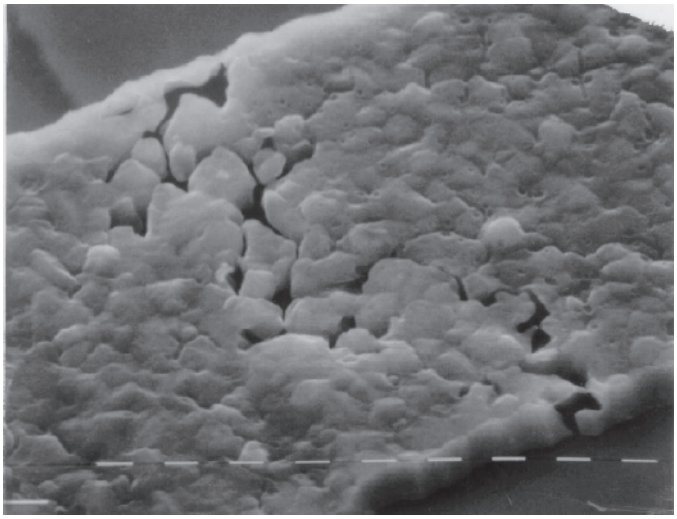


Figure 3. Scanning Electron Microscope (SEM) image of evaporated aluminum metal.

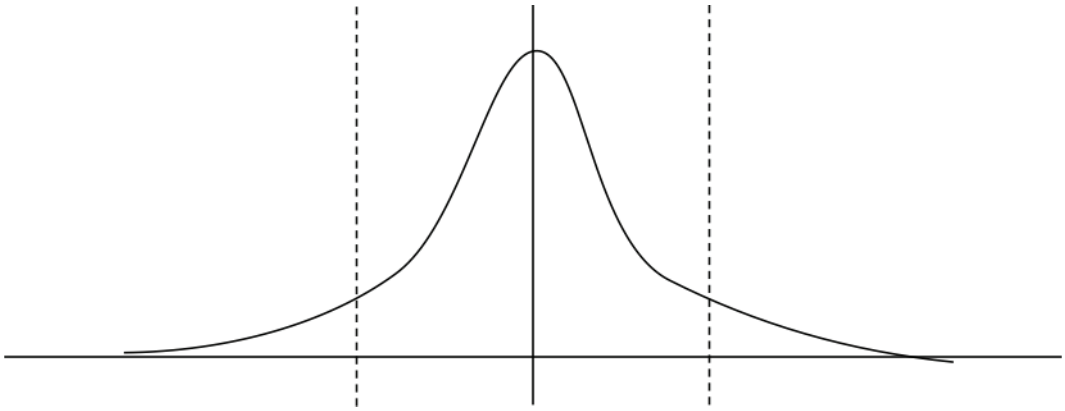
In conclusion, we discussed evaporation. This is a technique for depositing some metal layers on semiconductors. Historically, the semiconductor industry used evaporation to deposit aluminum interconnects during the 1970s and 1980s. Metal evaporation suffers some several deposition and reliability problems, including step coverage, thickness control, and stress voiding or stress migration. As such it is no longer in general use in the semiconductor industry. A few research projects use evaporation as a technique to deposit conductors. For example, some compound semiconductor research efforts might use evaporation to put down gold or other metals. However, we are unlikely to see a resurgence in this technique.

Technical Tidbit

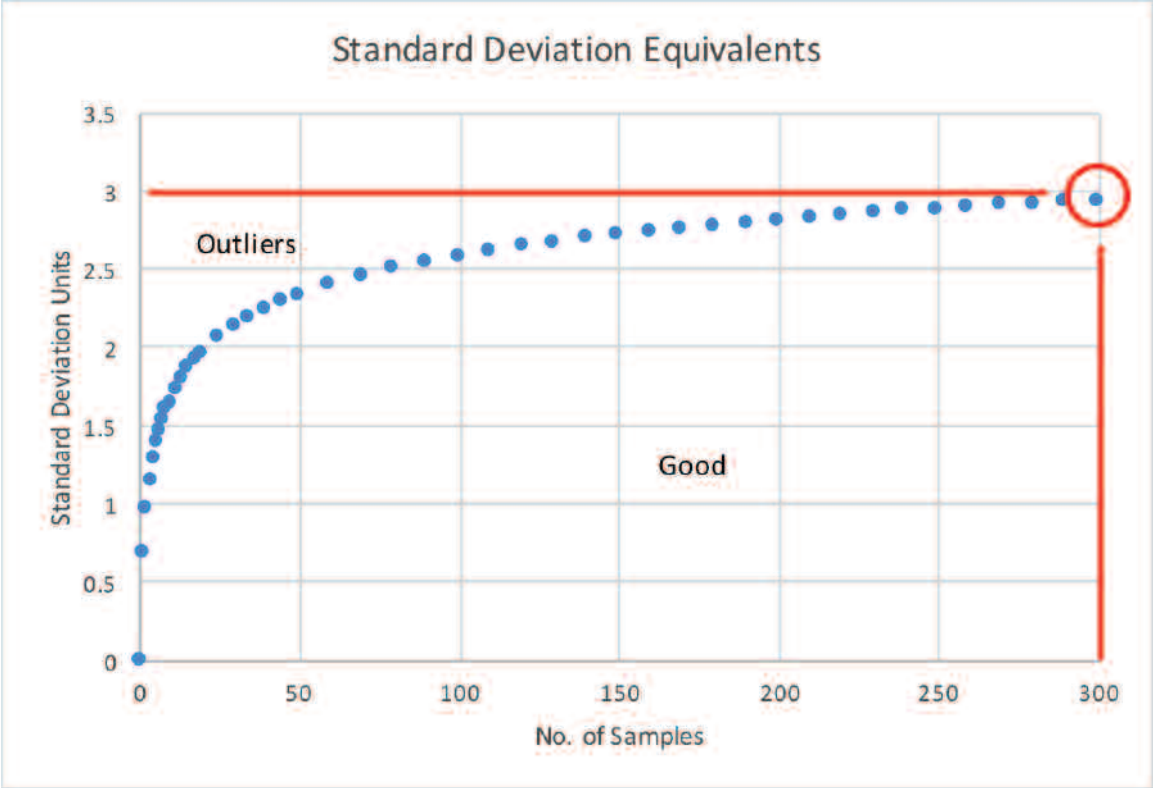
Chauvenet's Criteria

There is a not-so-widely known theorem in statistics called Chauvenet's theorem that we use in the semiconductor industry to identify outliers. Although it is not widely known, it forms the underlying basis of the more widely used criteria for Statistical Yield Limits (SYL) and Statistical Bin Limits (SBL).

The basic problem to solve is how to identify an outlier data point from a set of data. The point could be part of the distribution, or it may be outside of it. We need a formalized way to discern this, rather than trying to "eyeball" the value on a histogram or other plot, or some other form of guessing. The concept behind Chauvenet's theorem is to treat the data set as following a normal distribution with each data point consisting of a value Z, where Z is the distance in standard deviation units (sigma) from the mean (mu). X represents the actual data value. Once we know this, we can apply Chauvenet's criteria: If the expected number of measurements at least as bad as the suspect measurement is less than ½, then the suspect measurement should be rejected. This can be written as the term 1-(½)n, where n is the number of samples.



Chauvenet's criteria can be graphed as a plot of standard deviation units as a function of the number of samples. Notice that one requires about 300 samples to determine if an outlier is outside of 3 standard deviation units.



A particular application of this theorem sometimes goes by the name 3 Sigma Distribution. It is commonly used in the semiconductor industry to identify outliers during wafer probe testing. The 300 wafer number allows the engineer to detect wafers or wafer lots that lie outside of the 3 sigma limits for tests like Statistical Yield Limit (SYL) or Statistical Bin Limit (SBL).

Ask the Experts

Q: Is there a maximum fluorine level allowed for bondpads?

A: There is an unofficial spec limit of 6 at% using Auger Electron Spectroscopy that has been in use since the early 1980s (J.F. Gives et.al., Proc ECC 1982, pp.266) (J. Nesheim et.al., ISHM 1984, pp. 70 – 78) (J. Pavio et.al., ISHM 1984, pp. 428 – 432). One can also use EDX and XPS as ways to check for fluorine, but you need to remember that the interaction volumes are different, and so the results would be different depending on the analytical tool.

Spotlight: Defect-Based Testing

OVERVIEW

A modern semiconductor manufacturing process is one of the most difficult and complex processes to successfully control. There are thousands of variables that must all be tightly controlled in order to have a chance a repeatedly manufacturing a chip within a tight tolerance so that it can be successfully used in an electronics system. Furthermore, a modern semiconductor manufacturing process generates an incredible volume of data. This requires that engineers be able to not only choose the right data to examine, but also examine it in such a way as to understand the behavior of the process. We do this through statistical process control. This course is designed specifically for engineers who work in semiconductor manufacturing operations. We provide numerous real-world examples from semiconductor operations such as wafer fabrication, assembly, test, and reliability.

WHAT WILL I LEARN BY TAKING THIS CLASS

By focusing on tried and true methods for SPC, participants will learn the appropriate methodology to successfully identify problems, characterize them, and determine the root cause of failure.

Participants learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into four segments:

1. **SPC Foundational Elements.** Participants learn about the foundational elements of statistical process control, including: basic statistics, methods to visualize data, process capability, and basic problem solving.
2. **Process Monitoring Techniques.** Participants learn the various techniques for monitor a semiconductor process. They discuss on-wafer measurements like thin film measurements, defects, and electrical measurements.
3. **Process Control.** Participants learn about the various control charts and how to identify key variables in process control charts. They also discuss the fundamentals of process control and the various control methods.
4. **Design of Experiments.** Participants learn about Analysis of Variance (ANOVA) and other DOE methods like Factorial and Taguchi methods.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the tools, techniques and methods used in SPC.
2. Participants will be able to identify the different methods to visualize data related to SPC.
3. The seminar will identify the advantages and disadvantages of the various control charts that are used for SPC.
4. The seminar offers a variety of example problems, so the engineer can gain an understanding of the types of issues they might expect to see in their job assignment.
5. Participants will be able to set up a design of experiments to gather more data related to a particular problem.
6. Participants will understand the types of data on might gather, related to SPC.
7. Participants will be able to set up a control chart and monitor it for excursions and analyze the results.

COURSE OUTLINE

Day 1 (Lecture and Lab Time 8 hours)

1. Wafer Fab Related SPC
   a. Statistical Process Control
      i. Control Chart Basics
      ii. Control Charts for Variables
      iii. Moving Average Charts
      iv. X and R, S
      v. How to Monitor a Control Chart
      vi. Multiple Equipment same process control charts
      vii. Multivariate Control
      viii. Distributions
      ix. Cusum Charts
   b. Process control index Cpk and Ppk
   c. Defect Density & Yields
   d. Wafer Acceptance Test parameters
      i. Sort yield & Defect Density
      ii. Set outlier limit
      iii. Statistical Bin Limits methodology
   e. Design of Experiments
      i. Randomized Block Experiments
      ii. Two Way Designs
      iii. Student T-test
      iv. Analysis of Variance (ANOVA)
      v. ANOVA Table
      vi. Taguchi Methods
2. Assembly and Packaging Related SPC
   a. Variables
   b. Control Charts for Variables
   c. Process Capability Index (Cpk) - Review
   d. Multiple Equipment
   e. DOE Bonding optimization

Day 2 (Lecture and Lab Time 8 hours)

1. Test Related SPC
   a. Gauge Repeatability & Reproducibility Principles
   b. Test Limits
   c. SBL Setting
   d. Tester correlations
   e. Average Outgoing Quality
   f. Sample Size, AOQ, LTPD, etc.
   g. Confidence interval
   h. Exercises with Marvell-supplied data

2. System Level Test Related SPC
   a. Reliability Statistics
   b. Distributions
      i. Normal Distributions
      ii. Lognormal Distributions
      iii. Weibull Distributions
      iv. Exponential Distribution
   c. Gathering Accelerated Testing Data
   d. PPM and FITS Calculation
   e. Exercises with Marvell-supplied data
3. Reliability Statistics
   a. Gathering Accelerated Testing Data
   b. In-class Exercise: Determining Time to Failure
   c. Using the Poisson Distribution to Estimate PPM, FITS
   d. In-class Exercise: PPM and FITS Calculation
4. Field Returns and SPC
5. Wrap-Up Discussion

International Symposium for Testing and Failure Analysis

November 6-10, 2016
Fort Worth Convention Center
Fort Worth, TX, USA

Registration is available at
http://www.asminternational.org/web/istfa-2016

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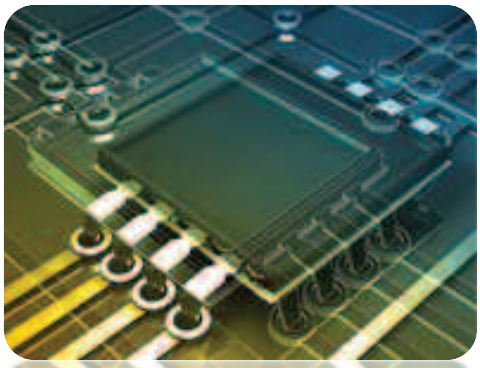

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.

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Upcoming Courses

(Click on each item for details)

Failure and Yield Analysis
Jan 30 – Feb 2, 2017 (Mon – Thur)
Portland, Oregon, USA

Advanced CMOS/FinFET Fabrication
Feb 7, 2017 (Tue)
Portland, Oregon, USA

Semiconductor Statistics
Feb 8 – 9, 2017 (Wed – Thur)
Portland, Oregon, USA

Defect Based Testing
May 3 – 4, 2017 (Wed – Thur)
Munich, Germany

Failure and Yield Analysis
May 8 – 11, 2017 (Mon – Thur)
Munich, Germany

Semiconductor Reliability and Qualification
May 15 – 18, 2017 (Mon – Thur)
Munich, Germany

Semiconductor Statistics
May 22 – 23, 2017 (Mon – Tue)
Munich, Germany