Issue 64 October 2014

InfoTracks

Semitracks Monthly Newsletter

Thermal Processing Part III - Oxidation and Kinetics

By Christopher Henderson

Last month we explored the topic of oxidation and kinetics in thermal processing. We'll continue our discussion this month. There are three steps in the oxidation model. The first step is the gas transfer of oxygen from the ambient environment to the gas/oxide interface. The second step is the diffusion of oxygen across the oxide layer. The third step is the chemical reaction that occurs at the silicon surface. The equations for each step are shown here.

$$F_1 = \left(h_G / HkT\right)\left(C^* - C_O\right)$$

$$F_2 = D\left(C_O - C_i\right) / X_O$$

$$F_3 = k_S C_i$$

F1 is the gas transport equation, F2 is the oxide diffusion equation, and F3 is the oxygen/silicon reaction equation. H sub G is the mass transfer coefficient in gas, and H is Henry's law constant. C star is defined as H times p sub G, where p sub G is the partial pressure of the oxidizing species in the bulk of the gas. D is the diffusivity of the oxidizing species in SiO2 and k sub s is the chemical surface reaction rate constant for oxidation.

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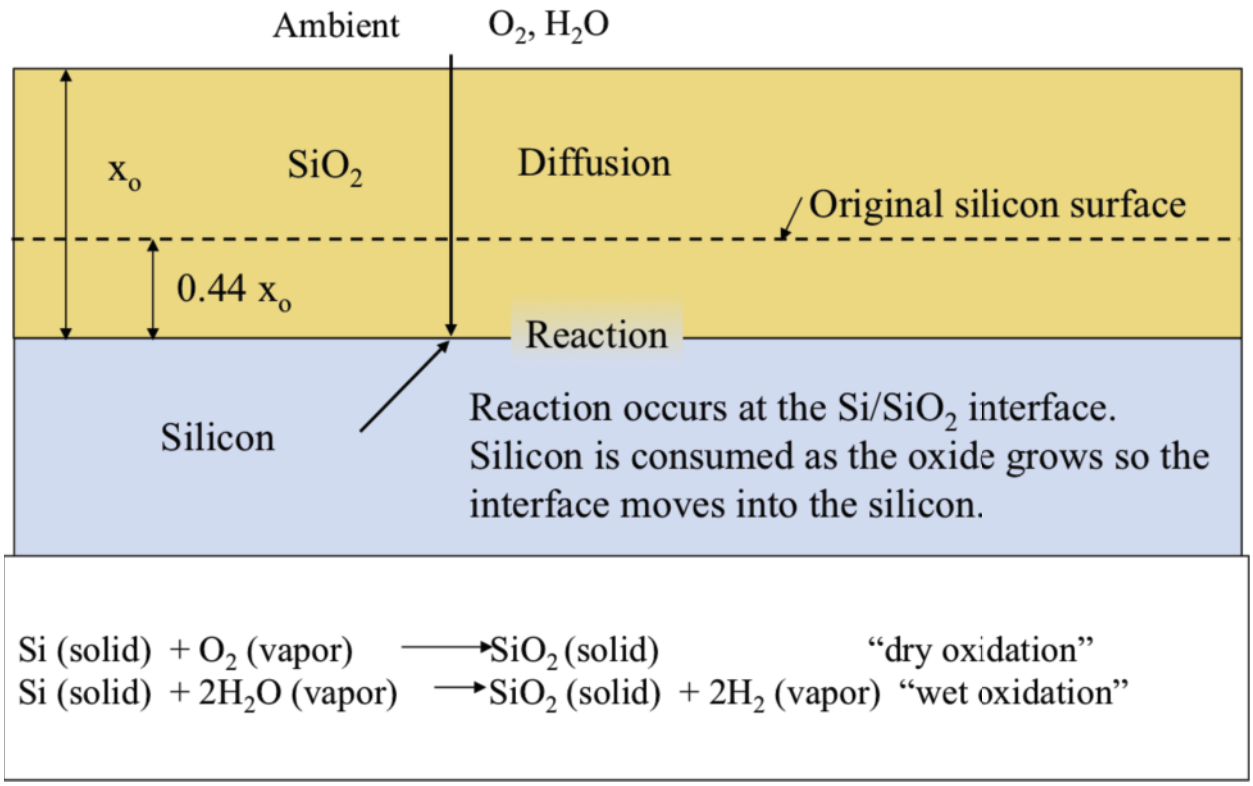
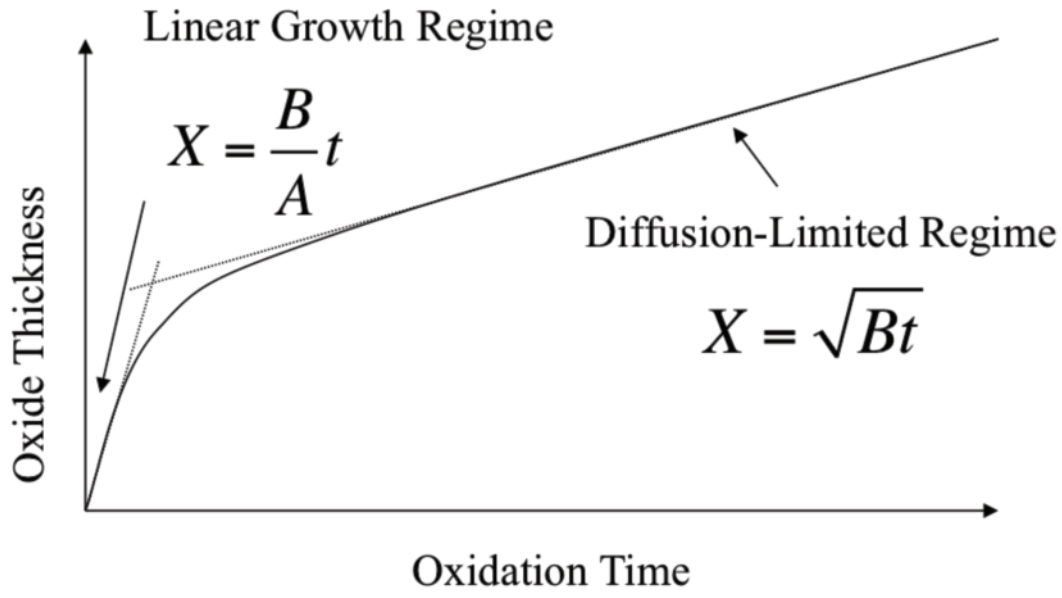
In the steady state condition F1 should equal F2 which should also equal F3. When the equations are set equal to one another, one can solve for the concentration at the surface of the oxide and the concentration at the interface between the silicon and the silicon dioxide. When the diffusion constant D is very small, the flux of oxygen through the silicon dioxide is small compared to the reaction rate at the interface. This is known as the diffusion rate controlled case, indicated by the line shown here.



When the diffusion constant D is very large, an ample supply of oxygen can reach the interface. This is a reaction rate controlled case, indicated by the line shown here.

If one solves for equation F3 (the reaction rate at the silicon/silicon dioxide surface) after applying the appropriate boundary conditions, one can obtain a solution for X, or the thickness of the oxide. This is a somewhat complicated differential equation boundary value problem, so we will not work it here. Basically, the thickness can be described under two different conditions: one where the time scale is quite long, and one where the time scale is short. The short time scale describes the initial growth region, or the reaction rate limited case, and the long time scale describes the diffusion limited case. For short times where t plus tau is much less than A squared over 4B, X sub O equals B over A times the quantity t plus tau, where B over A is called the linear rate constant. For very long times where t is much greater than A squared over 4B, X sub O squared equals B times t, where B is called the parabolic rate constant. These

are the fundamental pieces of the Deal-Grove oxidation model, which we will cover next. The graph here shows the composite of the two growth regimes, where oxide thickness is plotted against oxidation time.



Scientists have studied thermal oxidation for many years. Bruce Deal and Andrew Grove developed the first model to explain thermal oxidation in the mid-1960s while working at Fairchild Semiconductor. Here we show the basic model, where x is the oxide thickness, B is the parabolic rate constant, B over A is the linear rate constant, and tau is a factor to account for oxide present at the start of the oxidation.

$$x_{ox}(t) = \frac{A}{2}\left[\left(1+\frac{(t+\tau)}{\left(A^2/4B\right)}\right)^{1/2}-1\right] \quad \Rightarrow \quad \frac{x_{ox}^2}{B}+\frac{x_{ox}}{B/A}=t+\tau$$

Deal and Grove developed their model to agree with the two regimes, the linear growth regime and the parabolic growth regime. In the linear growth regime, the rate of the oxidation reaction dominates. This regime occurs while the oxide layer is still thin, and diffusion of oxygen to the surface is unimpeded. So if B is much greater than B over A, the Deal-Grove equation reduces to this formula.

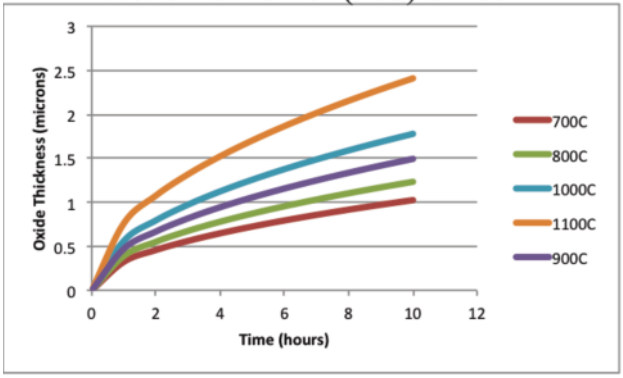
$$x_{ox} \cong \left(B/A\right)\left(t+\tau\right)$$

In the parabolic growth regime, the diffusion of oxygen to the silicon-silicon dioxide interface is increasingly limited. This regime occurs when the oxide increases beyond 500 angstroms. So in this case, if B over A is much greater than B, the Deal-Grove equation reduces to this formula.

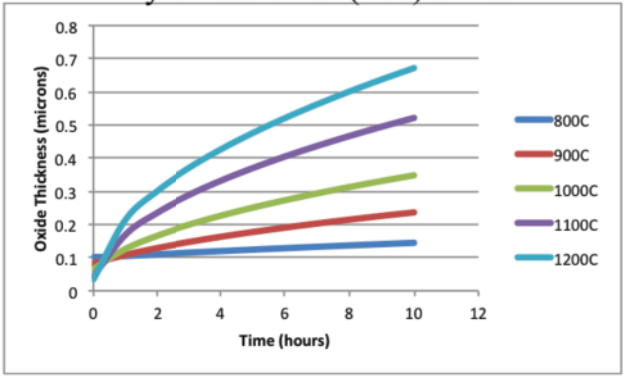
$$x_{ox}^2 \cong B(t+\tau)$$

These graphs show the Deal-Grove oxidation model applied to both wet oxidation and dry oxidation examples at various temperatures. We show the experimentally-derived constants in the tables below the graphs. Notice that the Deal-Grove model shows a clear oxidation rate driven regime as well as a diffusion rate limited regime.

Wet oxidation of (100) Silicon



Dry oxidation of (100) Silicon



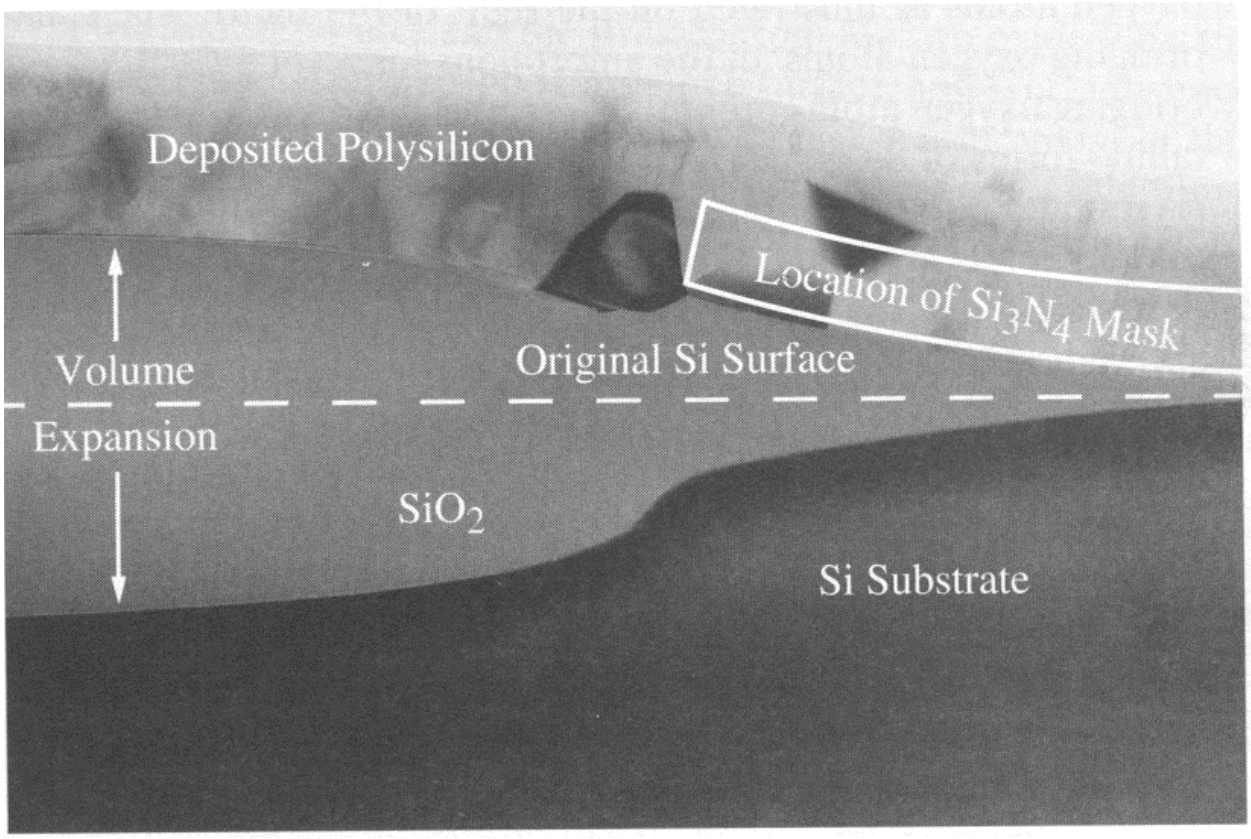
Oxidation Temperature	B	B/A	tau
1200	0.82	8.6	0
1100	0.58	2.76	0
1000	0.316	0.75	0
920	0.223	0.24	0
800	0.152	0.08	0
700	0.105	0.027	0

Rate constants

Oxidation Temperature	B	B/A	tau
1200	0.045	0.667	0.027
1100	0.027	0.178	0.067
1000	0.0117	0.042	0.37
920	0.0049	0.013	1.4
800	0.0011	0.0018	9
700	0.0003	0.00015	81

Rate constants

This image shows a cross-section of the silicon dioxide growth in a LOCOS (pronounced "low-cos") technology. In a LOCOS technology, process engineers grow a thermal oxide that serves as the isolation between transistors. A silicon nitride mask prevents the oxidation in the active region areas. Notice that the silicon dioxide has consumed a portion of the silicon, expanding down into the silicon itself. The original silicon surface is shown by the dotted line. There is even some growth of the oxide beneath the edge of the silicon nitride mask.



In conclusion, we discussed thermal oxidation and the kinetics of the reaction. While thermal oxidation is primarily driven by temperature, there are two regimes that also control the growth of the oxide: the oxidation rate-limited, or linear regime, and the diffusion rate-limited, or parabolic regime. Deal and Grove developed a model for thermal oxidation in the mid-1960s, and that model is still the prevailing model to explain and understand the first-order effects associated with oxidation.

Technical Tidbit

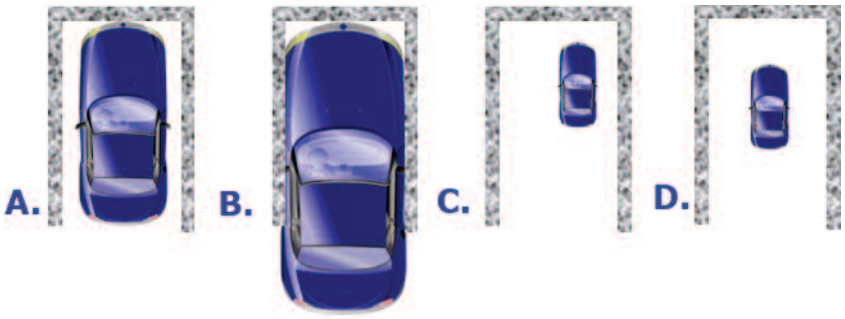
Process Capability Index

Process Capability Index, or Cpk, is an important topic for Product and Manufacturing Engineers to know. Cpk is an index in the form of a simple number which measures how close a process in running to its specification limits relatively to the natural variability of the process. The Cpk index is part of a series of indices that measure how much natural variation a process experiences relative to its specification limits and permits the engineer to compare different processes to one another with respect to their overall control. The larger the index number, the less like any particular data point will be outside the specification limits. However, a large index is not necessarily a good thing, so engineers may tighten the limits if there is a large Cpk. If Cpk is too large, one never sees an indication that prompts action to fix or optimize the process.

Calculations	Description
$\hat{C}_p = \frac{USL - LSL}{6\hat{\sigma}}$	Estimates what the process is capable of producing if the process mean were to be centered between the specification limits. Assumes process output is approximately normally distributed.
$\hat{C}_{p,lower} = \frac{\hat{\mu} - LSL}{3\hat{\sigma}}$	Estimates process capability for specifications that consist of a lower limit only (for example, strength). Assumes process output is approximately normally distributed.
$\hat{C}_{p,upper} = \frac{USL - \hat{\mu}}{3\hat{\sigma}}$	Estimates process capability for specifications that consist of an upper limit only (for example, concentration). Assumes process output is approximately normally distributed.
$\hat{C}_{pk} = \min\left[\frac{USL - \hat{\mu}}{3\hat{\sigma}}, \frac{\hat{\mu} - LSL}{3\hat{\sigma}}\right]$	Estimates what the process is capable of producing, considering that the process mean may not be centered between the specification limits. (If the process mean is not centered, $\hat{C}_p$ overestimates process capability.) $\hat{C}_{pk}<0$ if the process mean falls outside of the specification limits. Assumes process output is approximately normally distributed.
$\hat{C}_{pm} = \frac{\hat{C}_p}{\sqrt{1+\left(\frac{\hat{\mu}-T}{\hat{\sigma}}\right)^2}}$	Estimates process capability around a target, T. $\hat{C}_{pm}$ is always greater than zero. Assumes process output is approximately normally distributed. $\hat{C}_{pm}$ is also known as the Taguchi capability index.
$\hat{C}_{pkm} = \frac{\hat{C}_{pk}}{\sqrt{1+\left(\frac{\hat{\mu}-T}{\hat{\sigma}}\right)^2}}$	Estimates process capability around a target, T, and accounts for an off-center process mean. Assumes process output is approximately normally distributed.

This table describes the process capability indices and the equations to calculate them. Although there are a number of indices, Cpk is the most popular. Process capability indices assume that one is dealing with normally distributed data, and that may not always be the case. It's important to remember though that some data might have an upper bound, but no lower bound, or vice-versa. An example of this might be quiescent power supply current (IDDQ), or maximum frequency (Fmax). IDDQ typically has an upper bound, but no lower bound, whereas Fmax typically has a lower bound, but no upper bound.

Let's use a car and a garage as an analogy. The garage will define the specification limits, and the car will define the output of the process. We show four scenarios with cars and garages. If my car is only a little bit smaller than the garage, then I need to park it right in the middle of the garage (center of the specification) if you want to get all of the car in the garage. This is similar to a Cpk of 1. It is a marginal outcome. If my car is wider than the garage, it does not matter how I try to center it, because it will not fit. This is similar to a Cpk of less than 1. It is an unacceptable outcome. If my car is a lot smaller than the garage, it doesn't matter if I park it exactly in the middle, because it will fit and have plenty of room on either side. This is similar to a Cpk of greater than 1. If I can always park my smaller car in the center and with little variation, then this is equivalent to the highest Cpk value, or a value that is much greater than 1. Cpk describes the relationship between the size of the car, the size of the garage and how far away from the middle of the garage I parked the car.



So what is an acceptable value? Clearly, values that are below 1 will be unacceptable, and a value of 1 will be marginal, but what about larger values?

Cpk Value		Acceptance
<1.00	$<3\sigma/3\sigma$	Unacceptable
1.00	$3\sigma/3\sigma$	Marginal
1.33	$4\sigma/3\sigma$	OK
1.67	$5\sigma/3\sigma$	Good
2.00	$6\sigma/3\sigma$	Excellent
>2.00	$>6\sigma/3\sigma$	

In general in semiconductor manufacturing, we would like to see values equal to or greater than 2.00. This would constitute excellent process capability. A value of 1.33 would be acceptable, and a value of 1.67 would be good. These numbers will obviously vary depending on the process and the type of testing performed to generate the data. Some procedures like trim tests will have lower Cpks, but that is not necessarily a problem, as the purpose of trimming is to improve Cpk.

Ask the Experts

Q: How do you adequately protect high speed signal interfaces like LVDS interfaces from ESD and EOS?

A: This is a difficult task. The problem is that high speed signal interfaces require high performance transistors, which are small and sensitive to overstress. This means that to protect them from overstress events, particularly overstress events like charged device model ESD pulses, one must place resistors on the gates of the input transistors, or in series with the output. Unfortunately, this will slow down the operation of the circuits. This places the designer between a rock and a hard place. If one really needs a combination of high speed with additional protection, then one may need to consider other interface schemes that are not direct electrical connections, like optical connections or RF energy connections.

Spotlight: IC Packaging Design and Modeling

We have had some interest in running our IC Packaging Design and Modeling Course in the near future. We show the course overview and outline below. Please contact us at info@semitracks.com or 1-505-858-0454 if you are interested in attending this course. We can also run this course as an in-house course in certain instances as well.

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The industry is also pushing to use semiconductor devices in an increasing array of applications. To accomplish this, the industry is also driving prices down. This has created a number of challenges related to the packaging of these components. ***IC Packaging Design and Modeling*** is a 3-day course that offers detailed instruction on the design and modeling of IC packages. We place special emphasis on package interactions with the die. This course is a must for every manager, engineer, and technician working in IC packaging, using IC components in high performance applications or non-standard packaging configurations, or supplying packaging tools to the industry.

By focusing on the fundamentals of packaging design and modeling, participants will learn why advances in the industry are occurring along certain lines and not others. Our instructors work hard to explain semiconductor packaging without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor packaging. This skill-building series is divided into four segments:

1. **Packaging Design Overview.** Participants learn the fundamentals of packaging design. They learn why modeling has become critical to semiconductor packaging for today's designs.
2. **Mechanical Simulations.** Participants learn the fundamentals of displacement, strain, stress, and energy. They learn how to leverage St. Venant's Principle and apply fracture mechanics to a problem.
3. **Thermal Simulations.** Participants learn heat transfer modeling. They also learn about steady-state and transient thermal modeling. The instructor also explains industry standard and compact thermal models.
4. **Modeling Semiconductor Packages.** Participants learn about the software used for modeling a variety of aspects of semiconductor packaging. They see a number of examples using current modeling tools used by Package Design experts.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of semiconductor packaging design and its technical issues.

2. The participant will understand the basic concepts behind thermal and mechanical simulations of packages.
3. The seminar will identify the key issues related to the continued growth of the semiconductor industry. This includes the need for high power dissipation, and designs that can mitigate the increasing fragility of the die because of low-k dielectrics.
4. The seminar offers a wide variety of sample modeling problems that participants work in class to help them gain knowledge of the fundamentals of packaging modeling.
5. The participant will be able to identify basic and advanced principles for mechanical stress and thermal diffusion.
6. The participant will understand how package reliability, power consumption and device performance are inter-related.
7. The participant will be able to make decisions about how to construct and evaluate new packaging designs and technologies.
8. The participant will also be introduced to wafer-level simulations, which are increasingly necessary with the advent of low-k dielectrics.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, problem solving, and question/answer sessions, participants will learn practical information on semiconductor packaging and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field.

COURSE OUTLINE

1. Package Design Principles
   a. Background
   b. ITRS Roadmap Issues
   c. JEDEC Standards for Packaging
   d. Semiconductor Package Designs: What is a Good Packaging Design?
   e. Modeling Software
2. Assembly and Packaging Processes
   a. Assembly and Packaging Processes
   b. Selecting Package Materials
   c. Advanced Packaging
   d. Stacked Die & Stacked Packages
   e. Through Silicon Via (TSV) Interconnects
3. Stress Simulations
   a. Solid Mechanics Concepts
      i. Basics of Displacement, Strain, Stress and Energy
      ii. Leveraging St. Venant's Principle
      iii. Applying Fracture Mechanics

   b. Manufacturability
      i. Thermomechanical Modeling Metrics
      ii. To Model or Not to Model
      iii. Assembly Process Simulations
4. Thermal Simulations
   a. Heat Transfer Principles
   b. JEDEC Thermal Test and Simulations
   c. Steady-State and Transient Thermal Modeling
   d. Application-Specific Thermal Simulations
   e. Using Compact Thermal Models
5. Reliability and Coupled Mechanics
   a. Thermomechanical Reliability
      i. Solder Joint Reliability (SJR)
      ii. Single Chip & Multiple Chip Package SJR
      iii. Solder Joint Shape Predictions
   b. Coupled Mechanics
      i. Moisture Diffusion
      ii. Plastic Package “Popcorn” Cracking
6. Wafer-Level Simulations
   a. Venturing into New Territory (Submodeling)
   b. Chip-Package Interactions
      i. Interfacial Fracture Mechanics
      ii. Bridging IC Interconnect and Package Gaps
   c. Microelectromechanical Systems (MEMS)
      i. Device Operations
      ii. MEMS Packaging
7. Drop Tests SimulationsIC Packaging Design and Modeling Course Outline- 2
   a. Drop Test & Structural Dynamics
   b. Solder Selection & Performance
      i. Leaded Solders
      ii. Lead-Free Solders
      iii. Surface Finishes, Solder Pastes, & Metallization
   c. Package Design Effects
      i. Stand-Off Heights
      ii. Ball Array Pattern
      iii. Single Chip & Multiple Chip Packages

Semitracks will exhibit at this year's International Symposium for Testing and Failure Analysis. Please stop by and see us (booth 725). Call us at 1-505-858-0454 or email us at info@semitracks.com to schedule.

40th Annual International Symposium for Testing and Failure Analysis

Conference and Exposition

November 9 – 13 • Houston, Texas
Stop by and see us!
For more information on the symposium, visit
http://www2.asminternational.org/content/Events/istfa
Please feel free to contact us to set up an appointment while you are there!

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).

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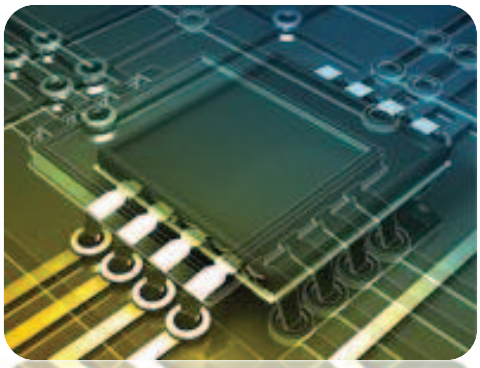

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our web site!

http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Product Qualification

January 26 – 27, 2015 (Mon – Tue)
San Jose, California, USA

Wafer Fab Processing

January 26 – 29, 2015 (Mon – Thur)
San Jose, California, USA

EOS, ESD and How to Differentiate

January 28 – 29, 2015 (Wed – Thur)
San Jose, California, USA