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Electron Energy Loss Spectroscopy

By Christopher Henderson

Electron Energy Loss Spectroscopy or EELS (pronounced "eels") is a technique that has been around for some time, but is increasingly used for analysis of fab-related defects. The spatial resolution and sensitivity of the technique allow engineers to examine nanometer-scale defects and anomalies, which is far beyond what one can achieve with Energy Dispersive Spectrometry (EDS). EELS can be performed with the appropriate detector on an electron beam system that can transmit electrons through a sample, such as a scanning transmission electron microscope or a standard transmission electron microscope. EELS operates on the fact that electrons will lose energy as they are transmitted through a sample. The energy loss is specific to different elements, allowing the analyst to obtain information similar to that of energy dispersive x-ray analysis. EELS is more sensitive to light elements that EDS, making it useful for examining oxide and nitride layers, as well as other light elements such as lithium and boron. EELS can generate information in the form of spectra and elemental maps, just like EDS.

The EELS detection system is quite a bit different than the EDS detection system (see Figure 1). The transmitted electrons travel through the sample to the detector, which is mounted beneath the sample. The electrons are focused through an aperture at the entrance to the detector. A magnetic prism bends the electrons toward the energy-selecting slit. The amount of bend is dependent on the energy of the electrons after they exit the sample. The faster they

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travel, the less they are bent. The electrons are then focused through a quadrupole-sextupole lens arrangement, and then sent to a CCD camera for imaging. This detection system is very sensitive to small changes in electron energy, making it ideal for distinguishing elements. The detection system has the spatial resolution of the TEM, and is sensitive to most elements in the parts per million range.

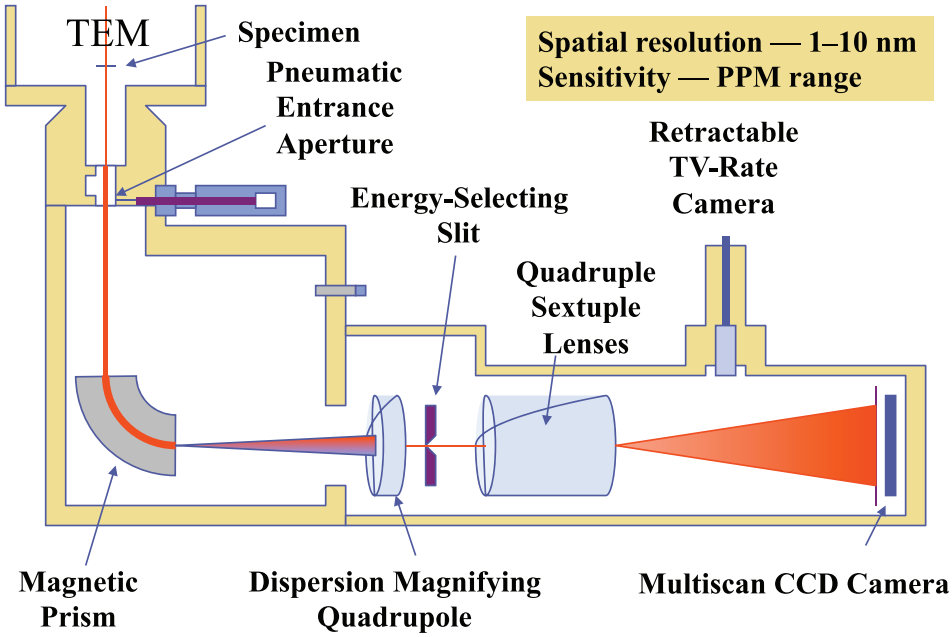

Figure 1. Schematic of an Electron Energy Loss Spectrometer.

An EELS spectrum looks somewhat different than an EDS spectrum (see Figure 2). This graph shows a typical EELS spectrum. The values on the x-axis represent the energies lost by the electrons after they interact with the sample. Notice that there is a large peak at zero electron volts. These are zero loss electrons. These are ballistically transported electrons or elastically scattered electrons that retain their primary energies as they travel through the sample. There is a minor peak between 50 and 100 volts. These are low loss electrons, or electrons that interact with weakly bound outer shell electrons. This includes plasmons or resonance of valence electrons. The larger peaks at higher energies, like the one at 150 electron volts and the other at 330 electron volts, are high loss electrons. These are electrons that interact with inner shell electrons, causing excitation into an unoccupied shell above the Fermi level. They result is characteristic elemental energy loss edges. For example the K and L edges are excited by the 1s and 2s-2p electrons respectively. Sometimes, minor perturbations can be seen on the major peaks. These minor bumps can give the analyst insight into the bonding of the elements in the sample. Each element has a specific energy-loss and near-edge structure, or ELNES, which can be used to determine the valence state and nearest neighbor co-ordination of the atom analyzed. Bond lengths and co-ordination of molecular groups can be determined using extended energy loss structures, or EXELFS, which extend beyond the energy-loss edge maxima.

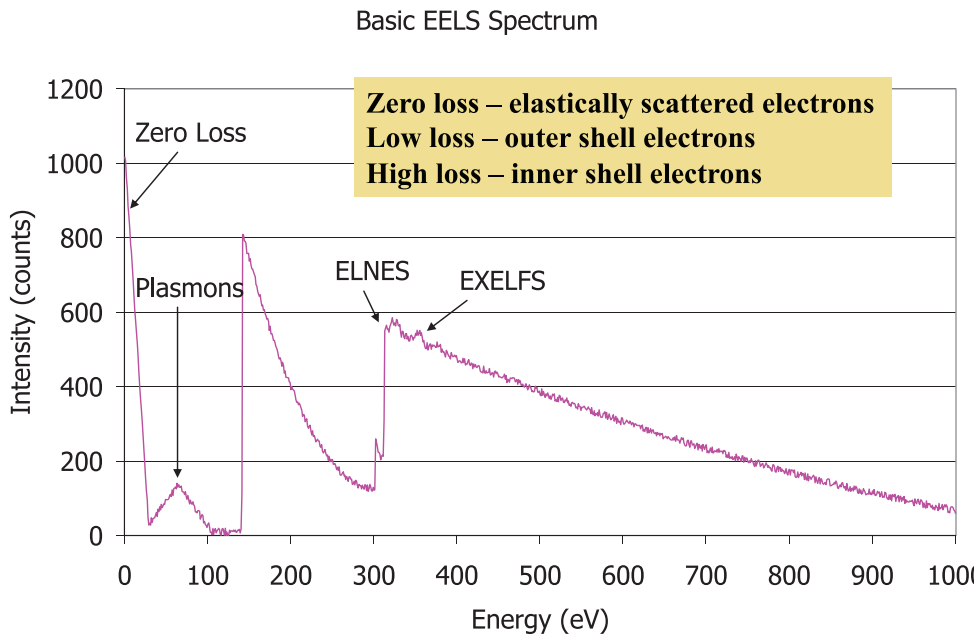

Figure 2. An example of an EELS Spectrum.

Figure 3 shows an example of an EELS spectrum on a sample with a defect in the gate region of an MOS transistor. Interestingly, this defect showed significant contrast in the FIB, but very little in the TEM image. The engineers used EELS to determine that the anomaly was actually an aluminum or aluminum oxide particle incorporated into the gate region.

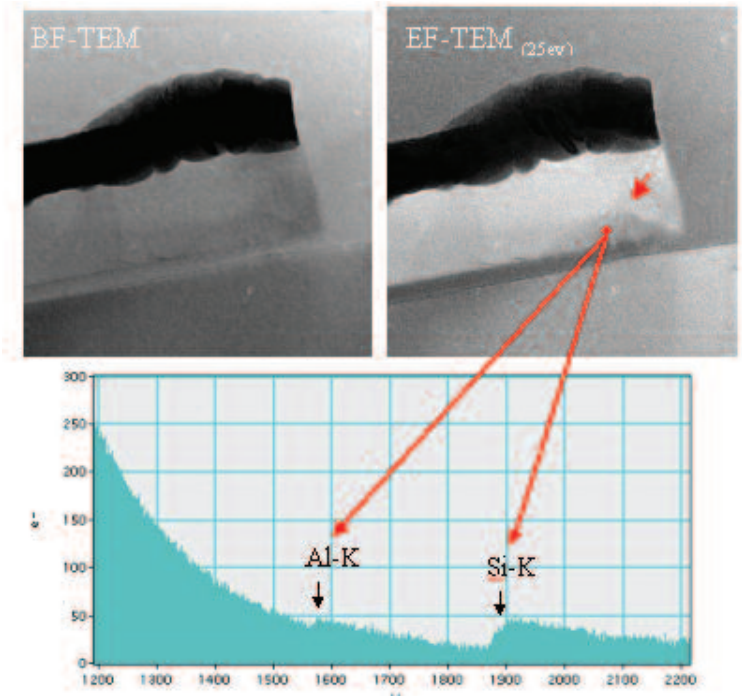

Figure 3. TEM images and EELS spectrum of a defect in the gate region of a transistor.

Like energy dispersive x-ray spectroscopy, EELS can also yield elemental dot maps. These examples show dot maps that highlight certain elements. The dot maps come from the same field of view. The dot map on the left is a nitrogen map and shows a nitride layer on an integrated circuit, while the dot map on the right is an oxygen map and shows an oxide layer on a circuit. EELS dot maps can have a sensitivity down to the parts per million range, and can provide a spatial sensitivity of 10 nanometers or better.

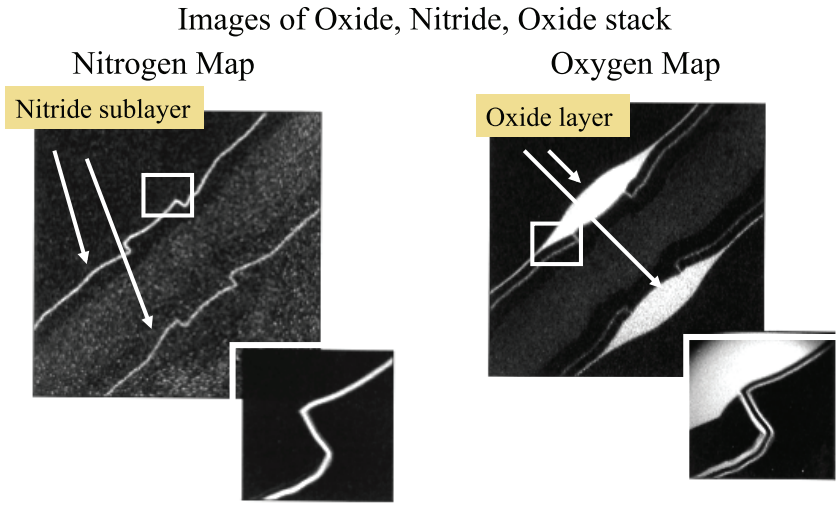

Figure 4. EELS elemental dot maps of a Shallow Trench Isolation (STI) process on the left, and a Local Oxidation of Silicon (LOCOS) process on the right.

In summary, EELS is a powerful technique for determining the elemental constituents of defects at the nanometer-scale level. EELS requires significant sample preparation since one performs EELS in the TEM or STEM. As feature sizes shrink further, EELS is one of the few techniques that allow engineers to see potential defects and analyze their composition. This is crucial for problem-solving and corrective action.

Technical Tidbit

Parallel Test Efficiency

One method for reducing the cost of test is to test components in parallel on the same test system. Test engineers commonly use this approach on devices with low pin counts. Many analog and mixed-signal devices fall into this category. Ideally, one should be able to achieve a factor N speedup, where N is the number of devices tested in parallel. Sometimes N is referred to as the number of test sites, or simply number of sites. In reality, one cannot achieve this ideal increase in test efficiency. Factors like program loads and setups for parallel testing cannot be shrunk, so one cannot achieve 100% efficiency in parallel test. Therefore, engineers use a concept called Parallel Test Efficiency, or PTE, to describe the increase from multi-site testing.

The equation for Parallel Testing efficiency is:

$$x = \frac{N - \frac{T_m}{T_s}}{N - 1}$$, where

x is the parallel test efficiency
N is the number of sites
T_m is the multi-site test time
T_s is the single site test time

We can write this in a different form if we're interested to determine the multi-site test time.

$T_m = x \cdot T_s + N(1-x)T_s$, where $T_m = x \cdot T_s$ is the parallel component and $N(1-x)T_s$ is the serial component.

Let's work an example then. Let's assume that we have a test configuration for a single site test and a four-site test. Let's assume the test times are 0.65 seconds for the single site and 0.95 seconds for the four-site test. The parallel test efficiency would then be:

$$x = \frac{4 - \frac{0.95}{0.65}}{4 - 1} = 0.846 = 84.6\%$$

Ask the Experts

Q: Why are IC test floors so loud?

A: The air conditioning and tester fans create the noise. Automatic Test Equipment to test high performance ICs use a lot of power. These systems need to be able to produce and capture accurate waveforms at high frequencies. This requires specialized circuits that dissipate a lot of power. When you couple this with the fact that a test system might require several hundred of these circuits, and the fact that there might be dozens of testers on a test floor, a lot of heat must be dissipated. A round number for a tester might be 10 watts per channel times 400 channels. Therefore, 20 testers would dissipate 80,000 watts. If the A/C were interrupted on one of these test floors, the temperature would climb 40 °F (22 °C) in a matter of 15 minutes.

Spotlight: Wafer Fab Processing

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. ***Wafer Fab Processing*** is a one-day course that offers an overview look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we summarize the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the basics of each processing step and the issues surrounding them, participants will learn why certain techniques are preferred over others. Our instructors work hard to explain how semiconductor processing works without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Processing Steps.** Each processing step addresses a specific need in IC creation. Participants learn the fundamentals of each processing step and why they are used in the industry today.
2. **The Evolution of Each Processing Step.** It is important to understand how wafer fab processing came to the point where it is today. Participants learn how each technique has evolved for use in previous and current generation ICs.
3. **Current Issues in Wafer Fab Processing.** Participants learn how many processing steps are increasingly constrained by physics and materials science. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.

COURSE OBJECTIVES

1. The seminar will provide participants with an overview of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind the fundamental wafer fab processing steps.
3. The seminar will identify the key issues related to each of the processing techniques and their impact on the continued scaling of the semiconductor industry.
4. Participants will be able to identify the basic features and principles associated with each major processing step. These include processes like chemical vapor deposition, ion implantation, lithography, and etching.

5. Participants will understand how processing, reliability, power consumption and device performance are interrelated.
6. Participants will be able to make decisions about how to construct and evaluate processing steps for CMOS, BiCMOS, and bipolar technologies.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

COURSE OUTLINE

1. Raw Silicon Wafers
2. Ion Implantation
3. Thermal Processing
4. Contamination Monitoring and Control
5. Wafer Cleaning and Surface Preparation
6. Chemical Vapor Deposition
7. Physical Vapor Deposition
8. Lithography
9. Etch
10. Chemical Mechanical Polishing
11. Cu Interconnect and low-k Dielectrics
12. Leading Edge Technologies and Techniques
    a. ALD
    b. high-k gate and capacitor dielectrics
    c. metal gates
    d. SOI
    e. strained silicon
    f. plasma doping

For each of these modules, the following topics will be addressed:

1 fundamentals necessary for a basic understanding of the technique
2 its role(s) and importance in contemporary wafer fab processes
3 type of equipment used
4 challenges
5 trends

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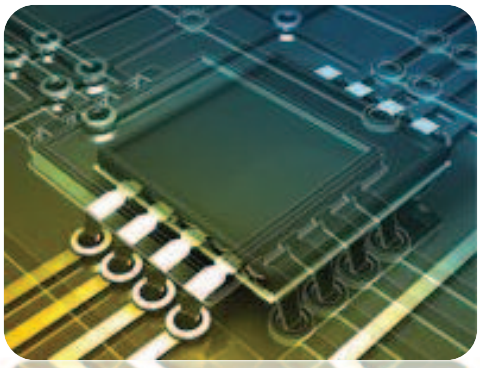

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October 23 – 25, 2013 (Wed – Fri)
Malaysia

Wafer Fab Processing
November 7, 2013 (Thur)
San Jose, California, USA

Advanced Thermal Management and Packaging Materials
November 19 – 20, 2013 (Tue – Wed)
Philadelphia, Pennsylvania, USA

Copper Pillar Technology and Challenges
December 19 – 20 2013 (Thur – Fri)
Malaysia

Semiconductor Reliability
February 11 – 13, 2014 (Tues – Thur)
San Jose, California, USA

Failure and Yield Analysis
February 17 – 20, 2014 (Mon – Thur)
San Jose, California, USA

Microelectronic Defect, Fault Isolation and Failure Analysis
February 19 – 21, 2014 (Wed – Fri)
Malaysia

Microelectronic Defect, Fault Isolation and Failure Analysis
February 24 – 26, 2014 (Mon – Wed)
Singapore