

# INFOTRACKS

## YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY



### Semiconductor Cleanroom Technology

By Christopher Henderson

In this month's Feature Article, we will continue our discussion of the Cleanroom Technology topic of storage and delivery of Chemicals and Gases in a Cleanroom by briefly covering each individual Gas. When constructing a new cleanroom facility, one must pay close attention to the types of Process Gases that one plans to use in the fabrication process. This will play a key role in locating the Gas storage areas, planning and implementing the delivery system, and determining safety requirements.

The first Gas to mention is Argon. Argon is naturally occurring, and comprises approximately 1% of the atmosphere. It is inert, so it doesn't pose an outdoor storage hazard other than potential mechanical hazards associated with compressed Gases. Argon is used primarily to support plasmas for deposition and etch reactions. It is also used in deep UV (ultra-violet) lithography lasers, and as a specialized cryogenic cleaning agent.

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- Advanced CMOS/FinFET Fabrication

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The first Gas to mention is Argon. Argon is naturally occurring, and comprises approximately 1% of the atmosphere. It is inert, so it doesn't pose an outdoor storage hazard other than potential mechanical hazards associated with compressed Gases. Argon is used primarily to support plasmas for deposition and etch reactions. It is also used in deep UV (ultra-violet) lithography lasers, and as a specialized cryogenic cleaning agent.

The next Gas to mention is Nitrogen. Nitrogen is naturally occurring, and is the most common Gas in the atmosphere, comprising approximately 78% of the atmosphere. It is inert, so it doesn't pose an outdoor storage hazard other than potential mechanical hazards associated with compressed Gases. However, in confined areas, it is a potential suffocation hazard. Nitrogen is heavily used in fab processing. Ultra-high purity Nitrogen is required during fab construction as the first infrastructure pipes and tubes are being welded together to exclude oxygen, moisture, and particles from the future supply to production tools. Eventually, Nitrogen is fed to every tool as part of the overall process flow, which keeps the semiconductor wafer free of all contaminants, from incoming inspection to final qualification. Nitrogen is used to purge any ingressed air and residual process chemicals, and to keep the wafer and all production-wetted surfaces and spaces free from oxygen, moisture, and particles. Nitrogen is also used to purge vacuum pumps, which need a constant Gas flow even when the tools are idle; and abatement equipment, which could be subject to pyrophoric conditions if air were present.

The next Gas is Oxygen. Oxygen comprises approximately 21% of the atmosphere. Unlike Argon, Oxygen is somewhat hazardous, even though we need Oxygen to survive. The primary hazard is its flammability. Oxygen itself is not flammable, but it directly fuels flammability in other materials. It is also an oxidizing agent, so it will damage materials and surfaces. Ultra-high purity Oxygen is used as a direct oxidizing agent to grow silicon oxide layers, and in more complex deposition and etch steps, as a co-reactant. In addition, industrial grade Oxygen is supplied to the abatement equipment as an oxidizer to turn reactive waste Gases into less hazardous and more easily removed compounds.

The next gas is Hydrogen. Because Hydrogen is such a small constituent of the atmosphere, only 5 parts per million, it is generated through other processes, like hydrocarbon steam reforming or electrolysis. Hydrogen is quite hazardous; it is an explosive hazard and must be protected from contact with Oxygen, except under controlled circumstances within the fab process tools. Hydrogen is used for epitaxial deposition of silicon and silicon germanium and for annealing of oxidized surfaces. More recently, it is also used in high volume as a cleaning agent to remove tin from the light sources of extreme UV lithography tools. Traditionally supplied by truck to the fab as a bulk gas or liquid, leading-edge fabs with high hydrogen demands can benefit from on-site production.

The next gas is Helium. Helium is the second lightest element and the coldest liquid. While Helium is the second most abundant element in the universe, it is relatively sparse on earth. It is produced as a by-product of nuclear decay of heavy elements in the Earth's crust, and it accumulates in the same geological deposits as natural gas. However, only a few such natural gas deposits have sufficient amounts of Helium to make it economically viable for separation, purification, and supply. It is liquefied to  $-269^{\circ}\text{C}$  and shipped around the globe in vacuum-jacketed containers, often taking several months to deliver from the point of production to the point of use. It is inert, so like Argon, it doesn't pose a storage hazard other than compressed Gas hazards. Helium is used in semiconductor manufacturing at hundreds of points in the fab for back-side wafer and load-lock cooling, plasma processing, and leak detection.

Next is Carbon Dioxide, or  $\text{CO}_2$ . Carbon Dioxide is present in the atmosphere in small quantities, approximately 0.035%. As such, Carbon Dioxide is obtained as the by-product from industrial production of ammonia, fertilizers, and hydrocarbons, and can also be captured from the production of Hydrogen by steam reforming. Special care is required to ensure the purity and consistency of  $\text{CO}_2$  supplies to the semiconductor industry. Carbon Dioxide isn't hazardous, other than the usual suffocation hazards that exist in confined spaces.  $\text{CO}_2$  is used in three major process steps in leading-edge fabs. First, Immersion lithography tools employ a thin layer of water between the final optical lens and the wafer surface to create a sharper focus of the light and enable smaller features.  $\text{CO}_2$  is added to water to displace dissolved nitrogen, which can create microscopic bubbles that distort the intended patterning. Second, small amounts of  $\text{CO}_2$  are also added to the ultrapure DI (deionized) water in some fab applications to increase the conductivity of the water, and thereby, safely dissipate any electrical charges that can attract small particles. Lastly,  $\text{CO}_2$  is also used in some etch and deposition processes.

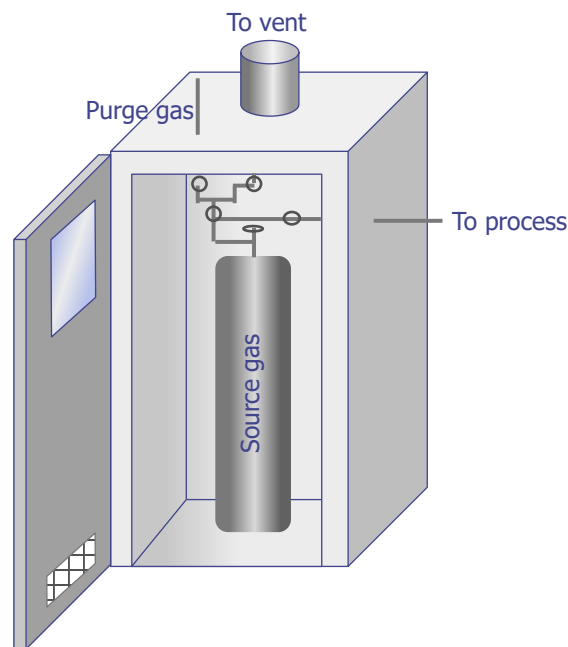
Next, let's briefly discuss bulk Electronic Specialty Gases, or ESGs. The most common ones include ammonia, hydrogen chloride, nitrogen trifluoride, nitrous oxide, and silane. Other than  $\text{SiH}_4$ , or silane, which is shipped as a compressed gas, these materials are delivered to the fab site as pressurized liquids, and then vaporized before distribution to the points of use. They are primarily obtained from chemical synthesis of industrial chemical feedstocks and further purified.  $\text{NF}_3$  or nitrogen trifluoride is the exception because it is made and used almost exclusively as a material for electronics manufacturing. ESGs were originally supplied to fabs in individual gas cylinders. Now, the size and intensity of leading-edge fabs, in terms of wafers under production and number of process steps, has increased the demand for these five important gas-phase chemicals to such large volumes that they need to be supplied to fabs in ISO containers to sustain supply chain logistics and economies of scale. We show an example of an ISO container in Figure 1 below.



**Figure 1- Example of an ISO container for shipping and storing bulk ESGs.**

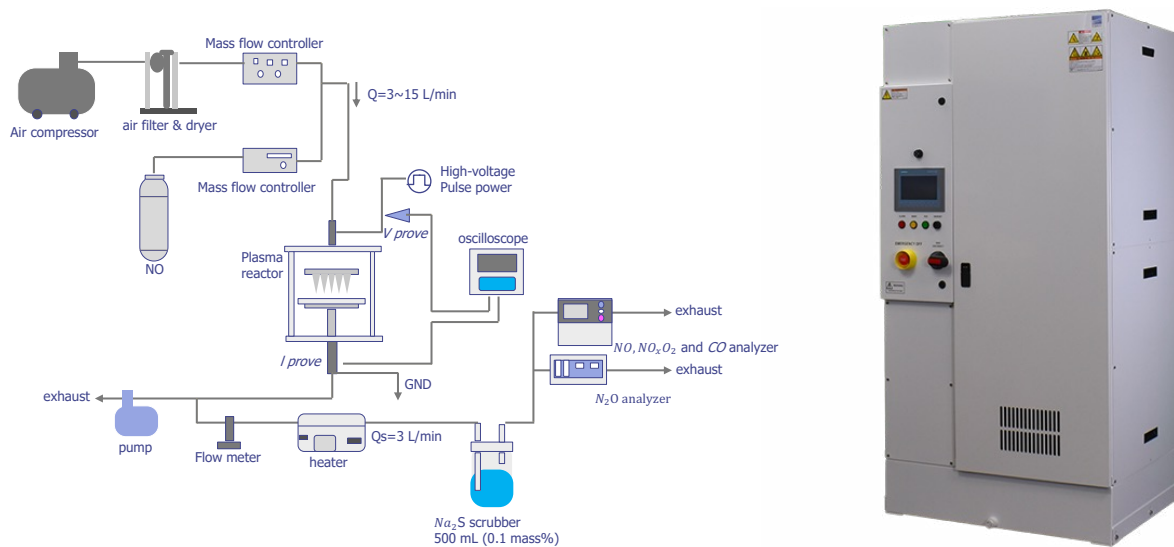
Let's now discuss hazardous Gases that are used in the cleanroom. These Gases range from the pyrophoric and/or toxic specialty Gases required for thin film deposition and doping processes, such as ammonia, methane, silane, germane, dichlorosilane, silicon tetrachloride, phosphine, diborane, arsine and others, to the reactive and corrosive gases needed in different etch processes, like chlorine, fluorine, halocarbons, nitrogen trifluoride, and others.

Hazardous high-pressure Gases include those with pyrophoric, flammable, corrosive, and toxic characteristics, such as silane, most hydrocarbons, fluorides and chlorides, phosphine, arsine, and others. Such Gases are typically stored in high pressure cylinders that must be maintained in well-vented gas cabinets that are specially designed to mitigate the hazard associated with a specific Gas. Most semiconductor fabrication plants have large numbers of such cabinets on site, and there are strict regulations governing the placement and number of hazardous gases in a given facility. See, for instance, the standards published by the National Fire Prevention Association, specifically NFPA 45, the "Standard on Fire Protection for Laboratories using Chemicals". Figure 2 shows a schematic of a typical hazardous gas cabinet designed to contain pyrophoric Gases such as silane. These cabinets are equipped with appropriate fittings for connection to the high-pressure cylinders and valve configurations that are designed for cross-purging piping connections to remove residual pockets of Gas prior to disconnecting an empty cylinder. Modern gas cabinets are normally equipped with analytical sensors that can detect any leakage from the cylinders or piping.



**Figure 2- Diagram of a hazardous gas storage cabinet.**

Let's discuss a brief example (see Figure 3). The process exhaust downstream from the cleaning, deposition and metal etch processes employed in a semiconductor fab often experiences problems due to fouling. This is most often caused by the condensation and build-up of solid or liquid process by-products on the internal surfaces of vacuum components and exhaust lines. Such build-up can be controlled by maintaining the exposed surfaces at elevated temperatures; therefore, fabs require technologies that accurately and precisely control the surface temperatures of the different components in the vacuum train and exhaust gas handling systems. Exhaust streams in a fab frequently contain very corrosive and/or toxic gases that must be removed by chemical scrubbing prior to release to the atmosphere. This entails the use of equipment in most fabs that is dedicated to managing and treating the process exhaust gas stream. We show an example scrubbing process from nitrogen oxides on the left, and an image of the scrubber itself on the right. Maintenance of this equipment constitutes an important cost factor in all fabs, and there is a keen interest in equipment that can reduce or prevent build-up and/or corrosion and prolong maintenance cycles.



**Figure 3- (Left) schematic of exhaust gas system, and (right) an exhaust gas system (courtesy Ebara).**

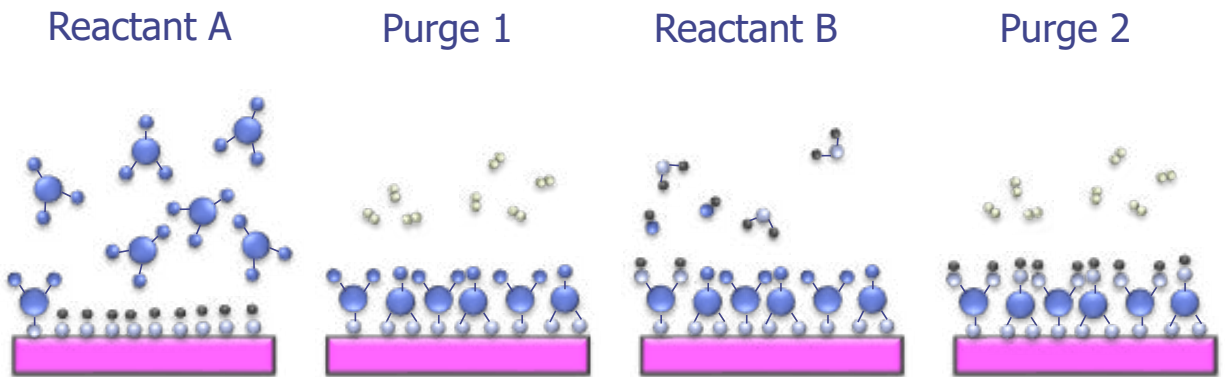
In next month's Feature Article, we will continue our discussion of the storage and delivery of Chemicals and Gases in a Cleanroom by discussing water usage in a semiconductor cleanroom environment.

# Technical Tidbit: Atomic Layer Deposition (ALD) for Nanoscale Devices

In this month's Technical Tidbit, we will provide a brief overview of Atomic Layer Deposition. Atomic Layer Deposition, or ALD, is an increasingly used process technique to deposit ultrathin, conformal layers in state-of-the-art wafer fab processes.

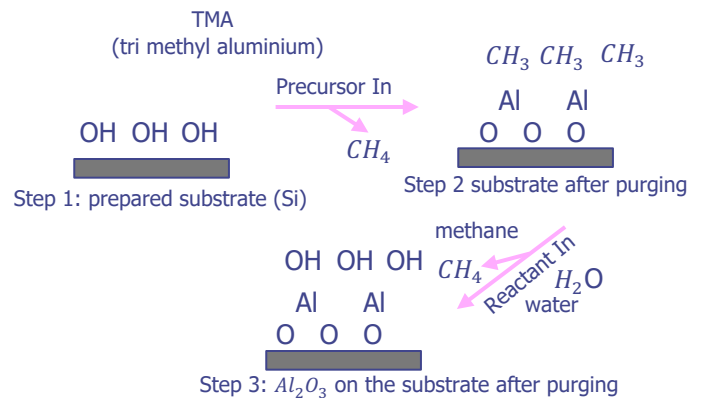
ALD has some important requirements for processing. In order for ALD to be useful, the layer deposited must be conformal, it must be smooth, and by necessity, it will need to be ultra-thin. It will need to be defect-free, exhibit excellent adhesion to the underlying materials, stoichiometric (a film with the proper element ratios), and exhibit no undesirable interface effects, like excess dangling bonds which can lead to trapped charge. Some additional features process engineers would like to see include precise control of the film thickness, a process that can be scaled to large areas and large wafers, and a process that generates a self-terminating reaction. The deposition conditions for ALD are quite similar to CVD. Process engineers typically use a moderately low pressure of around 1 torr to inject the inert or purge gases. They can use either heat or plasma, or a combination of the two, as an energy source to help drive the reaction. Using a plasma source can allow the process engineer to lower the deposition temperatures to between 50 and 100 C, which helps avoid damage to low-k dielectrics and other sensitive materials.

A critical part of the ALD process is the precursor. Precursors need to be volatile, or available in gas format; stable, or won't break down; and reactive, or will react with each other to form the layer, all at the required temperature. The byproducts must not interfere with the growing film; they should disperse and be removed from the chamber by the pumps. A basic process will have two precursors, while more complex processes may have 3 or 4 precursors. The precursor reaction steps are as follows. One, the first precursor bonds to the surface. This is self-terminating, self-limiting deposition that creates one monolayer. Two, the tool purges the first precursor and its byproducts. Three, the tool introduces the second precursor, which is typically an oxygen or nitrogen-containing species, and it will react with the first precursor now on the surface to create the deposited film. Again, this is a self-limiting, self-terminating bonding reaction involving one monolayer. Four, the tool purges precursor B and its byproducts. We show this process graphically in Figure 1.



Reactions occur at the surface

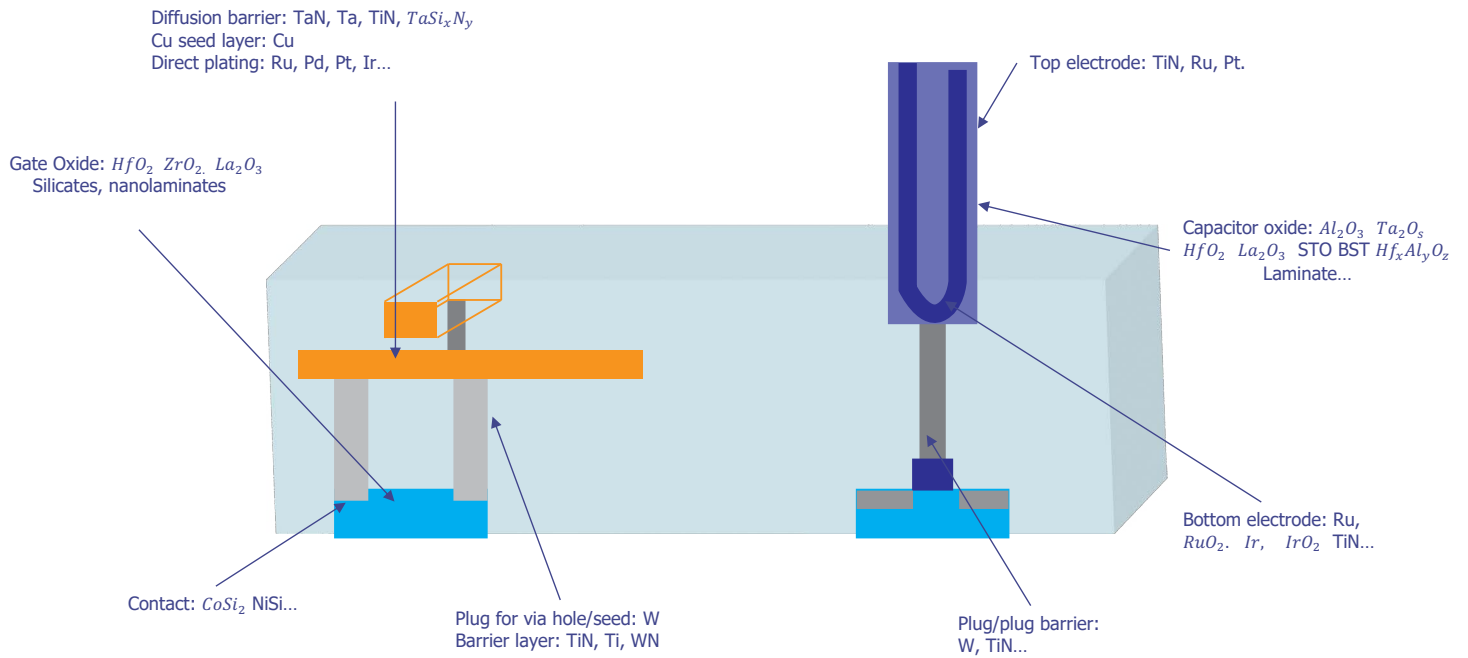
- Self-limiting growth process: gas-surface reactions occur until surface is saturated.
- Films are very uniform, smooth
- Precise thickness control
- Exact stoichiometry control
- Low contamination
- Conformal films in high aspect ratio structures



**Figure 1- Diagram showing an overview of the ALD process steps, and a specific example (lower right).**

In ALD processing, the chemical reactions occur on the surface of the wafer. It is a self-limiting growth process, so the gas-surface reactions occur until the surface is saturated, and then they stop. The films deposited by ALD are very uniform and smooth. With ALD, one can achieve precise thickness control and exact stoichiometry control. ALD films show low contamination levels. Finally, ALD films are conformal films, even in very high aspect ratio structures.

As we mentioned above, ALD is increasingly used in semiconductor manufacturing processes. We show some examples of where it is used in Figure 2. ALD is now used for gate dielectrics, contacts, vias, metal liners, and capacitor layers.



**Figure 2- Diagram showing some of the locations where ALD is used in semiconductor processing.**

In conclusion, ALD is a highly versatile technique that provides process engineers with the ability to deposit monolayers of material. This need is increasingly necessary as we approach atomic-scale dimensions for some of the finest layers on today's integrated circuits. Expect to see more use of ALD in future technologies.





# Ask The Experts

**Q:** I have a general question about the semiconductor industry. How do you see the longevity of semiconductor industry playing out compared to other industries such as oil and gas where we know that we are moving through an energy transition and more reliance on electronics? What is your opinion on that? How long will the semiconductor industry last?

**A:** Thanks for your question. I think that the semiconductor industry will be around for many years to come – at least 50 to 100 years. Right now, semiconductor components are the best way (by far) to process data and information, and I don't see any other technology that appears to be able to replace it, especially when it comes to cost, performance, and manufacturability.

I also think you will be surprised to see how long we continue to need oil and gas. I think we will probably still see a big use of oil and gas for the next 50 years, unless there is a complete movement to nuclear power in the very near future, which is highly unlikely. Solar and wind simply cannot supply the energy we need, and the manufacturers use too much oil and gas to create the solar panels, wind turbines and batteries.

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# Course Spotlight:FAILURE AND YIELD ANALYSIS

## OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Your industry needs competent analysts to help solve these problems. Failure and Yield Analysis is a 4-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a Do It Right the First Time approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

Participants will learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. **The Process of Failure and Yield Analysis.** Participants will learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.
2. **The Tools and Techniques.** Participants will learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools, light emission, electron beam tools, optical beam tools, decapping and sample preparation, and surface science tools.
3. **Case Histories.** Participants will identify how to use their knowledge through the case histories. They will learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

## **COURSE OBJECTIVES**

1. The seminar will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.
2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.
3. The seminar will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.
4. The seminar offers a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic technology features on semiconductor devices.
6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

## COURSE OUTLINE

1. Introduction
2. Failure Analysis Principles/Procedures
  - a. Philosophy of Failure Analysis
  - b. Flowcharts
3. Gathering Information
4. Package Level Testing
  - a. Optical Microscopy
  - b. Acoustic Microscopy
  - c. X-Ray Radiography
  - d. Hermetic Seal Testing
  - e. Residual Gas Analysis
5. Electrical Testing
  - a. Basics of Circuit Operation
  - b. Curve Tracer/Parameter Analyzer Operation
  - c. Quiescent Power Supply Current
  - d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
  - e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
  - f. Automatic Test Equipment
  - g. Basics of Digital Circuit Troubleshooting
  - h. Basics of Analog Circuit Troubleshooting
6. Decapsulation/Backside Sample Preparation
  - a. Mechanical Delidding Techniques
  - b. Chemical Delidding Techniques
  - c. Backside Sample Preparation Techniques
7. Die Inspection
  - a. Optical Microscopy
  - b. Scanning Electron Microscopy
8. Photon Emission Microscopy
  - a. Mechanisms for Photon Emission
  - b. Instrumentation
  - c. Frontside
  - d. Backside
  - e. Interpretation
9. Electron Beam Tools
  - a. Voltage Contrast
    - i. Passive Voltage Contrast
    - ii. Static Voltage Contrast
    - iii. Capacitive Coupled Voltage Contrast
    - iv. Introduction to Electron Beam Probing
  - b. Electron Beam Induced Current
  - c. Resistive Contrast Imaging
  - d. Charge-Induced Voltage Alteration
10. Optical Beam Tools
  - a. Optical Beam Induced Current
  - b. Light-Induced Voltage Alteration
  - c. Thermally-Induced Voltage Alteration
  - d. Seebeck Effect Imaging
  - e. Electro-optical Probing
11. Thermal Detection Techniques
  - a. Infrared Thermal Imaging
  - b. Liquid Crystal Hot Spot Detection
  - c. Fluorescent Microthermal Imaging
12. Chemical Unlayering
  - a. Wet Chemical Etching
  - b. Reactive Ion Etching
  - c. Parallel Polishing
13. Analytical Techniques
  - a. TEM
  - b. SIMS
  - c. Auger
  - d. ESCA/XPS
14. Focused Ion Beam Technology
  - a. Physics of Operation
  - b. Instrumentation
  - c. Examples
  - d. Gas-Assisted Etching
  - e. Insulator Deposition
  - f. Electrical Circuit Effects
15. Case Histories

# Upcoming Courses:

## Public Course Schedule:

[IC Packaging Technology](#) - January 23-24, 2024 (Tues.-Wed.) | Phoenix, Arizona - \$1,295

[Advanced CMOS/FinFET Fabrication](#) - January 29-30, 2024 (Mon.-Tues.) | Phoenix, Arizona - \$995

[Fundamentals of High-Volume Production Test](#) - January 29-30, 2024 (Mon.-Tues.) | Phoenix, Arizona - \$1,295

[Wafer Fab Processing](#) - February 26-29, 2024 (Mon.-Thurs.) | Munich, Germany - \$2,095

[Failure and Yield Analysis](#) - March 4-7, 2024 (Mon.-Thurs.) | Munich, Germany - \$2,095

[Semiconductor Reliability and Product Qualification](#) - March 11-14, 2024 (Mon.-Thurs.) | Munich, Germany - \$2,095

[Defect-Based Testing](#) - March 20-21, 2024 (Wed.-Thurs.) | Munich, Germany - \$1,195

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at [jeremy.henderson@semitracks.com](mailto:jeremy.henderson@semitracks.com)

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