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InfoTracks

Semitracks Monthly Newsletter

Thermal Detection Techniques

By Christopher Henderson

This month, we will begin a new series of Feature Articles that will cover techniques that localize heat-generating defects, or thermal detection techniques. Certain types of defects generate heat over and above the background heat generated by a semiconductor device. Although these techniques are becoming less useful on today's high power dissipation circuits, they are still important for the failure analyst. There are three competing technologies used frequently by the failure analysis community to identify and characterize heat-generating defects: Infrared Thermal Imaging, Liquid Crystal Thermography, and Fluorescent Microthermal Imaging. In this, the first of three articles, we will cover blackbody radiation and infrared thermography, which are classified under Infrared Thermal Imaging.

Failure analysts have always needed a way to identify thermal signatures on semiconductor devices and integrated circuits. Many types of defects can emit heat. Shorts, such as collector-emitter shorts, gate oxide shorts, and metal-to-metal shorts can emit heat. Incorrectly biased transistors can emit heat, as well as leakage paths due to parasitic structures and patterning defects.

In this Issue:

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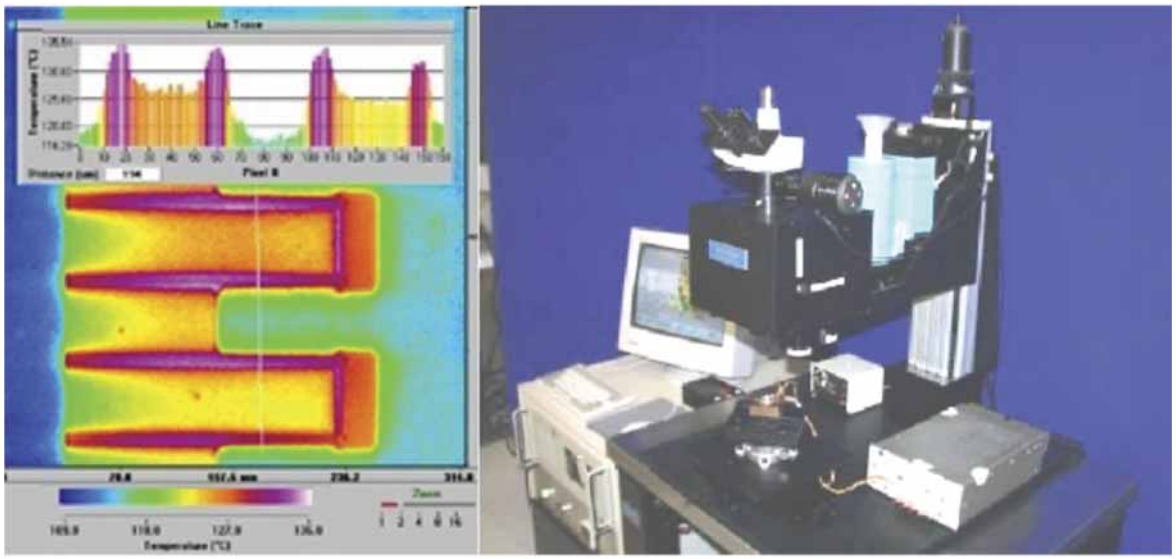

Figure 1. Thermal image (left) and thermal imaging system (right).

Infrared thermography is based on blackbody radiation physics. Blackbody radiation has been studied since the 19th century, and the concepts developed by scientists investigating the phenomenon apply directly to infrared (IR) thermography. IR thermography is a non-contact thermal analysis technique that directly senses heat from a circuit. In Figure 1, we show an example of a thermal image on the left and a thermal imaging system on the right. The camera in the system detects heat, much the way our eyes can see thermal data from a very hot object like a burning log. The advantage to this is that Infrared thermography is non-contact, and doesn't require a coating or film for use. The biggest disadvantage to infrared thermography is the spatial resolution. We'll see why this is the case in this article.

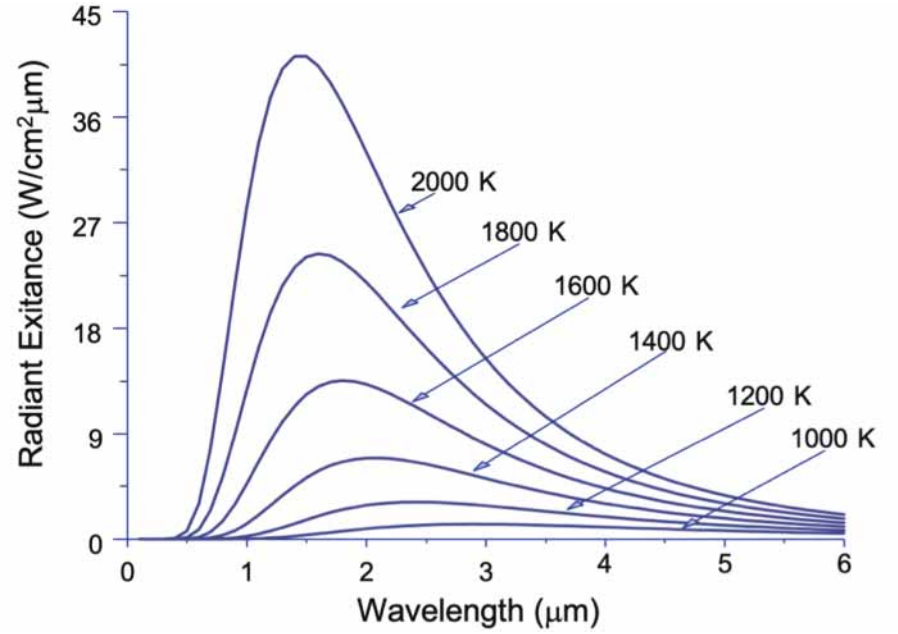

Figure 2. Radiation intensity for a blackbody as a function of wavelength for temperatures between 1000 and 2000 K.

Infrared thermography detects blackbody radiation. At very high temperatures, blackbody radiation can be quite significant. The sun is a good example of this. If one plots the radiancy versus wavelength, the relationship can be seen. In Figure 2, notice that as the temperature increases, the peak in the radiancy moves toward shorter wavelengths. For the sun, whose surface is approximately 5500 K, the peak in the wavelength is in the visible range that we can see as a brilliant white light.

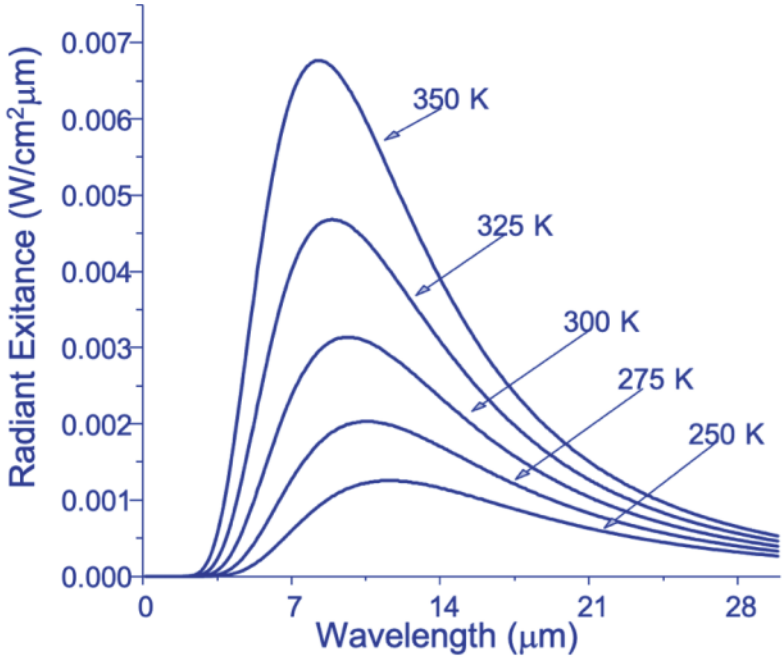

Figure 3. Radiation intensity for a blackbody as a function of wavelength for temperatures between 250 and 350 K.

One normally performs thermal imaging of semiconductor components at temperatures near room temperature. Figure 3 shows the radiancy as a function of wavelength for temperatures closer to room temperature. Notice that the radiancy is about four orders of magnitude less. That means IR thermography will require a very sensitive detector. More importantly, notice that the peak wavelengths are between 7 and 14 □m. This means that infrared thermography is effectively limited to around 7 □m spatial resolution unless the detector is extremely sensitive.

Material	Emissivity
Ideal black body	1.00
Lampblack	.95
Asbestos paper	.95
White Lacquer	.95
Bronze paint	.80
Carbon, rough plate	.76
Oxidized steel	.70
Polished brass, oxidized copper	.60
Aluminum paint	.55
Oxidized monel metal	.43
Cast iron- polished	.25
Copper- polished	.15
Nickel- polished	.12
Aluminum- highly polished	.05
Silver- highly polished	.02

Table 1. Emissivity values for selected materials.

IR Thermography not only depends on blackbody radiation, but it also depends on the type of object emitting the radiation. The optical property of interest here is emissivity. Emissivity can vary quite widely for various materials. Table 1 shows some common materials and their emissivity. A material, like lampblack, that absorbs light has a high emissivity, while a material that reflects light has a low emissivity, like highly polished silver. Notice that materials used in semiconductor devices, like aluminum and copper, have low emissivity. One needs to take this into account when examining these devices.

Parameter	HgCdTe	QWIP (n-type)	InSb
IR absorption	Normal incidence	$E_{optical} \perp$ plane of well Normal incidence: no absorption	Normal incidence
Quantum efficiency	≥70%	≤10%	≈30-40%
Spectral sensitivity	Wide band	Narrow-band	Wide band
Optical gain	1	0.2-0.4 (30-50 wells)	1
Thermal generation lifetime	≈1μs	≈10ps	≈0.1μs
RoA product (λ_c=10μm)	300Ω-cm^3	10,000Ω-cm^3	100Ω-cm^3
Detectivity (λ_c=10μm)	2×10^{12} cm-Hz$^{1/2}$-W^{-1}	2×10^{10} cm-Hz$^{1/2}$-W^{-1}	5×10^{11} cm-Hz$^{1/2}$-W^{-1}

Table 2. Properties of common infrared detectors.

Table 2 shows a list of the more common infrared detector types on the market. Almost all IR detectors are made from either mercury-cadmium-telluride quantum well infrared photoconductors, or indium antimonide. Although these detectors are sensitive down to about 1 μm wavelengths, there is virtually no spectral information at those wavelengths. Remember that the peak in radiancy is around 7 to 14 μm. The most popular systems on the market for semiconductor failure analysis, as of this writing, use indium antimonide detectors. This is due to the fact that indium antimonide has good quantum efficiency from about 1 to 5.5 μm, whereas mercury-cadmium-telluride has some gaps in quantum efficiency between 2.5 and 8 μm.

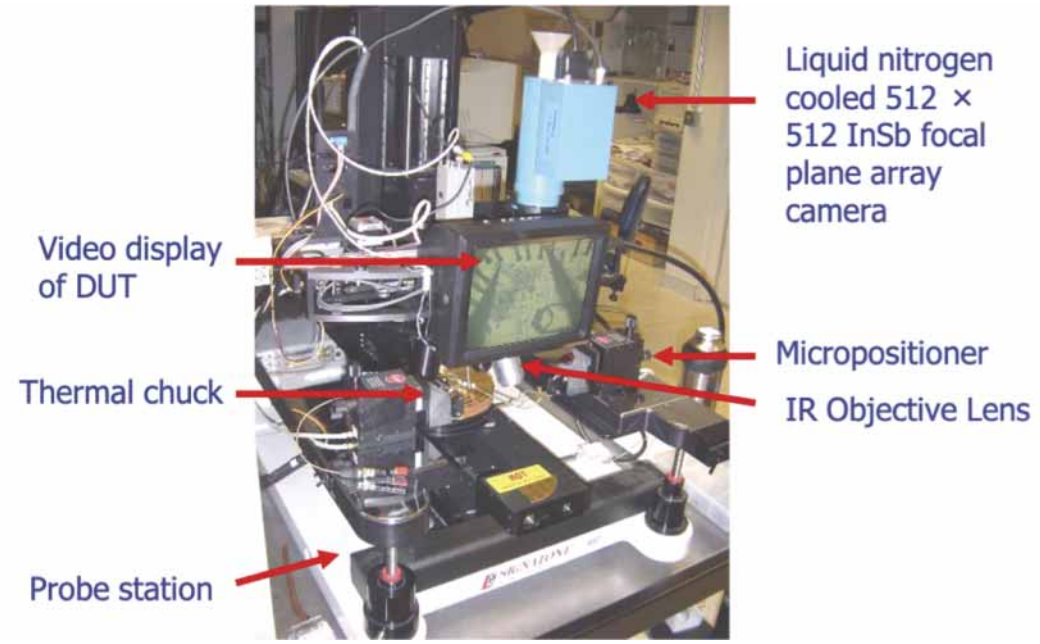

Figure 4. Basic infrared imaging microscope setup.

Figure 4 shows an example of an infrared thermal imaging microscope. The system consists of a probe station with an IR camera mounted on it. In this case, the camera is a liquid nitrogen-cooled 512 by 512 indium antimonide array camera. The IR image can be seen on the video display. The circuit can be powered through a probe card, or through individual probes. In this system, the stage can be heated if necessary.

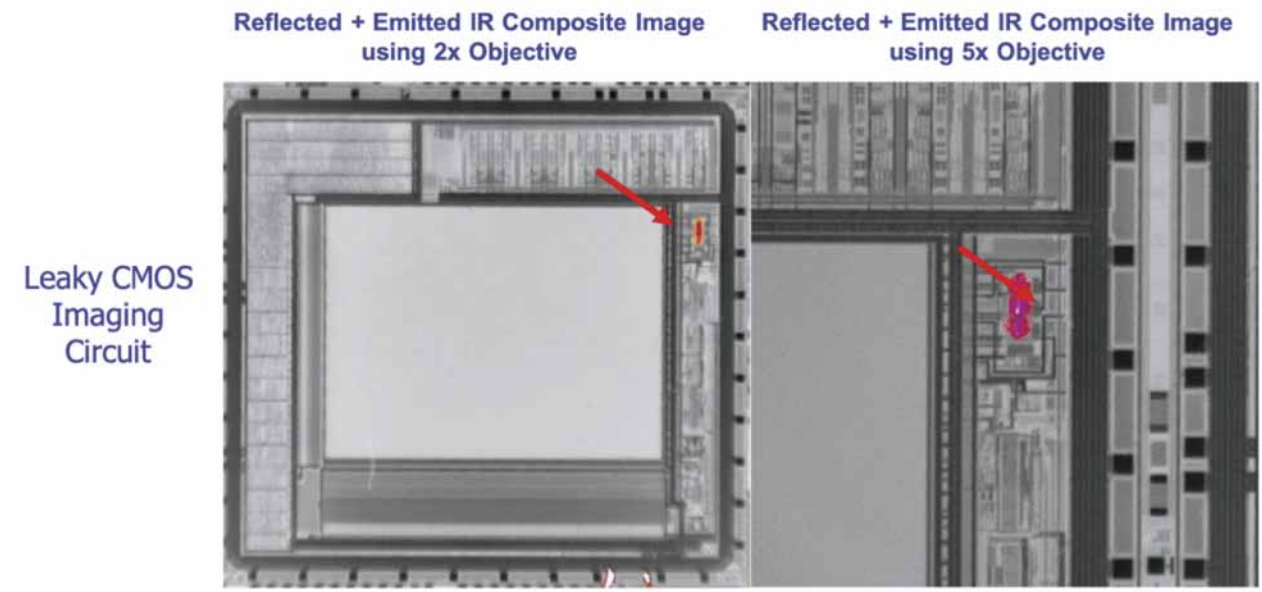

Figure 5. Thermal imaging of a CMOS imaging circuit with a defect.

Figure 5 shows an example analysis using infrared thermal imaging. This particular integrated circuit is a CMOS imaging circuit with leakage in a driver circuit. The arrow in the image on the left indicates the location of the leakage. The images are a composite of reflected infrared light and emitted infrared light. The image on the right shows a higher magnification image of the leaky circuit.

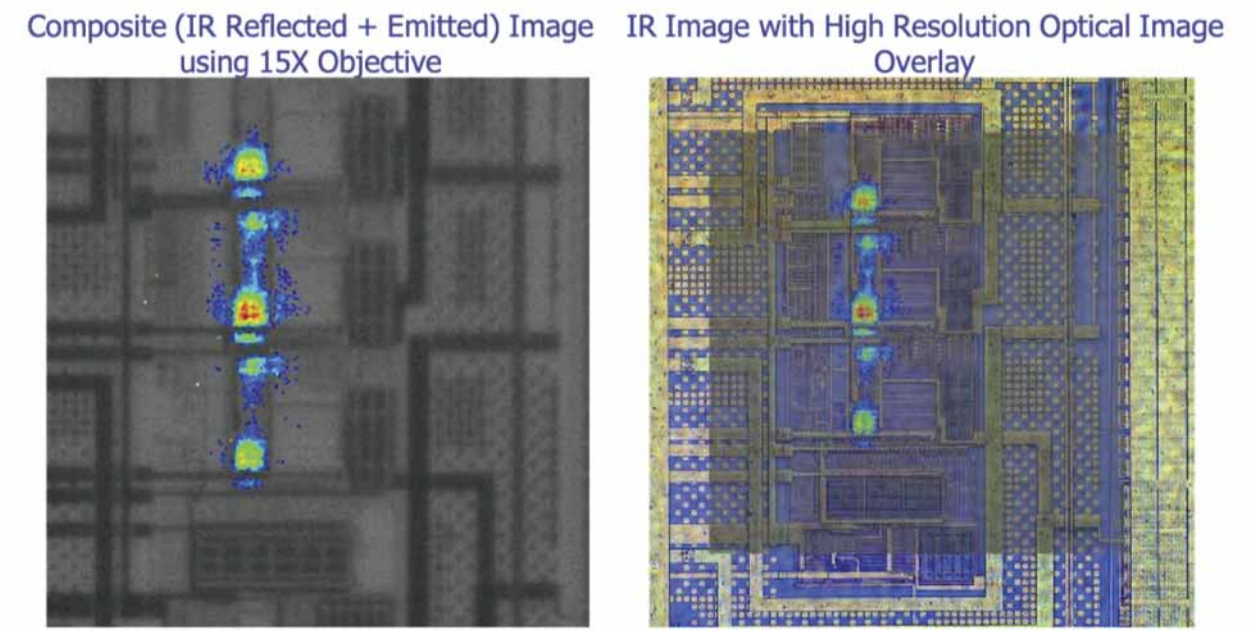

Figure 6. Higher magnification images of the defects seen in Figure 5.

Figure 6 shows the infrared thermal emission at a higher magnification. The image on the left shows a composite reflected IR-emitted IR image, and the image on the right shows the emitter IR image overlaid

on an optical image of the area in question. Again, the spatial resolution of the technique is limited to around 5μm, but it does allow one to rapidly and non-destructively locate the area where the leakage is occurring. Further analysis work will be necessary to localize the exact defect spot.

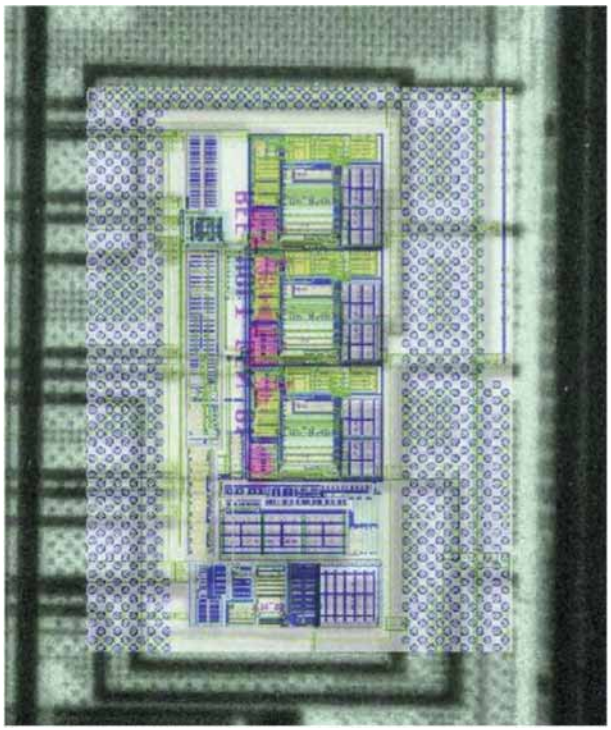

Figure 7. Defective region on a CMOS Imaging Circuit, overlaid with design database information.

Figure 7 shows the emitted IR overlaid on a computer-aided design database image of the area in question. This particular circuit, containing a group of PMOS transistors, was found to exhibit a low drain-to-source breakdown voltage.

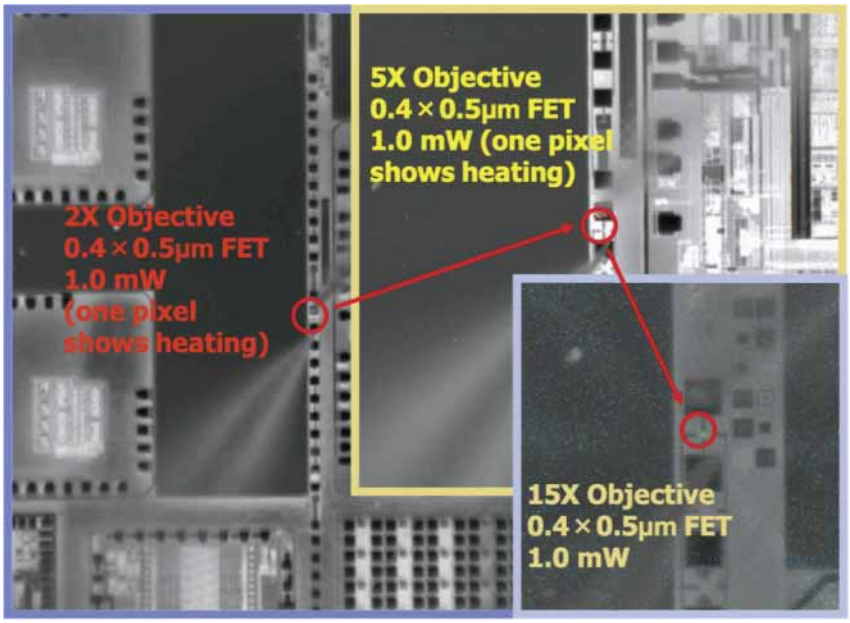

Figure 8. IR thermal images of transistor test structure.

Figure 8 shows the practical limits to the sensitivity of the system. At 20X and 50X magnification, the heat-generating location is limited to one pixel. At 150X, the heat generating site is beginning to spread out somewhat. The power of the tool is not in its resolution, but rather its ability to image non-destructively. No coatings are required, as is the case with Liquid Crystal Thermography and Fluorescent Microthermal Imaging.

In next month's Feature Article, we will discuss Liquid Crystal Thermography.

Technical Tidbit

Process Instabilities

In this month's Technical Tidbit, we will give a quick overview on the subject of process instabilities.

What is a process instability? Well, it is a factor or condition that causes the results of a parameter we examine to change in an irregular or even unpredictable manner. There are various causes, but it is often related to process steps that involve charging, like ion implantation, etch, CVD or PVD, or photoresist profiles.

First, let's discuss normal process variation and its effect of process on yield. An electrical parameter that is sensitive to a process parameter is in general, undesirable. To improve the yield, the best approach is to operate in a region of lower sensitivity. We illustrate that concept in Figure 1. The red curve represents the sensitivity of an electrical parameter to a process parameter. If one operates higher on the curve, the electrical parameter is less sensitive to the process parameter, as we show in the green region on the left, whereas lower on the curve, it is more sensitive, as we show in the red region on the left. The compatibility between the design assumptions and the manufacturing statistical process control is crucial for this to work.

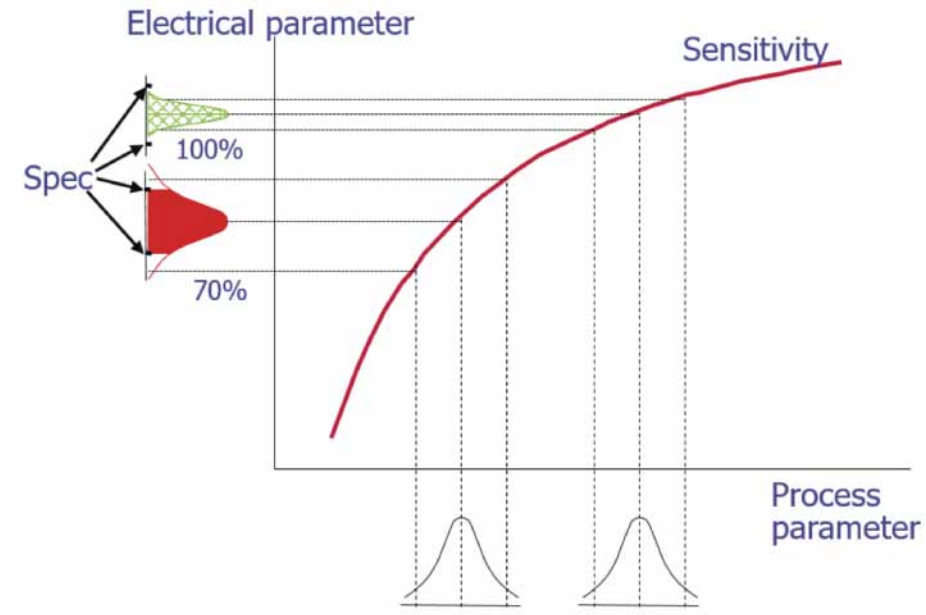

Figure 1. Test Structure Electrical Behavior vs a Relevant Process Parameter.

As shown in Figure 2, the control chart is one of the more important methods to visualize process instabilities. A control chart, also known as a Shewhart Chart (named after its inventor, Walter Shewhart), or an SPC chart, provides a way to graph a parameter, or group of parameters over time. Often the 'over time' variable is done by using lot numbers or wafer numbers, like we show in Figure 2.

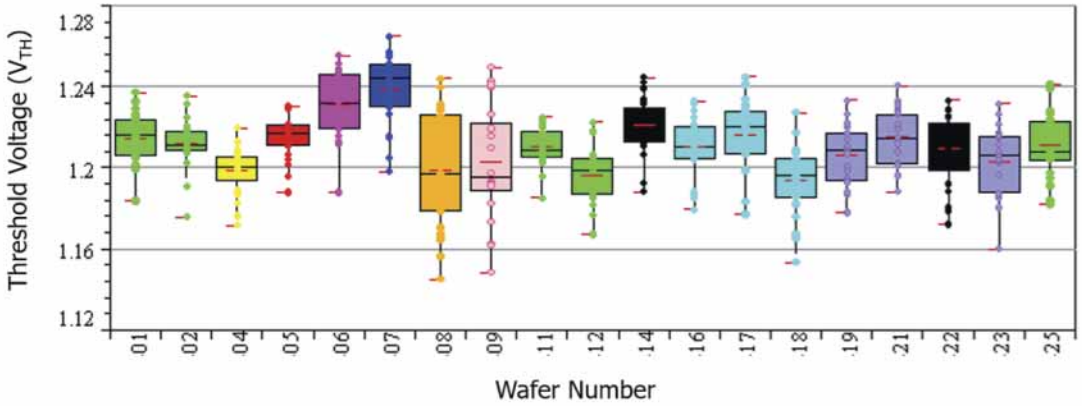

Figure 2. Control Chart showing Threshold Voltage as a function of the Wafer Number.

Now let's look at the control chart in Figure 3. Is this process stable? The answer is no. Notice that there are two significant spikes, one around run number 12, and another one around run number 67, that exceed the 3 sigma limits. There is also a run of about 10 points above the trend line around runs 82 through 92. These conditions are patterns that indicate the overall process is not stable, and is not in control.

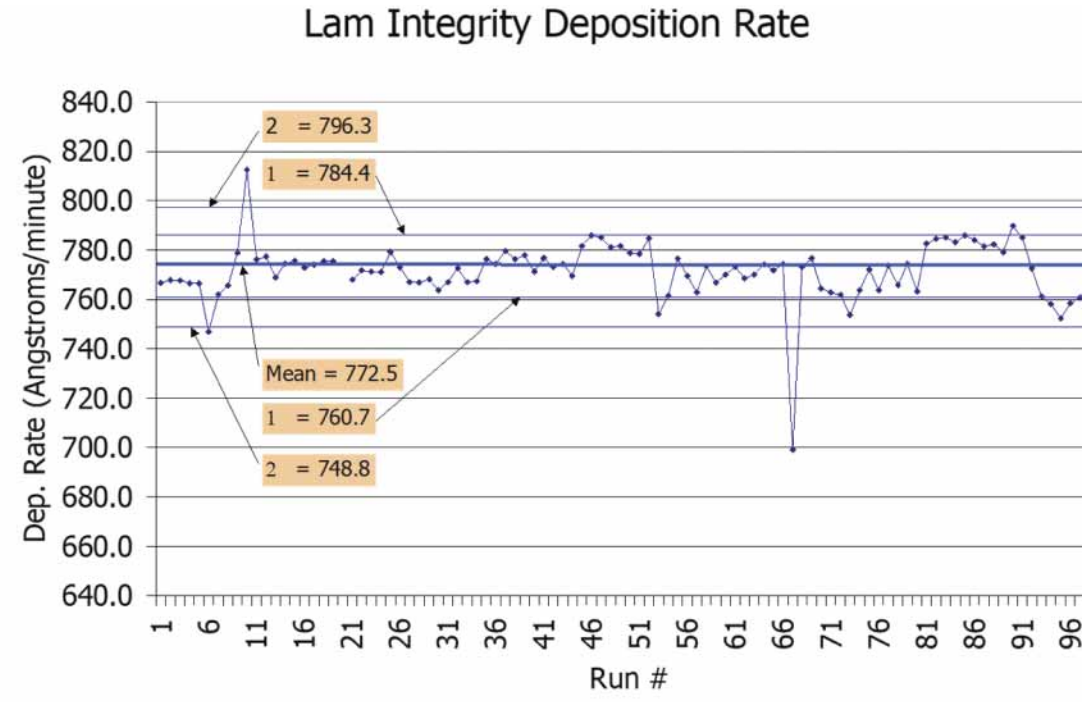

Figure 3. Control Chart showing Deposition Rate as a function of Wafer Operations (Denoted as "Run #" in the Figure).

Once we have identified we have a process instability, how do we go about troubleshooting the problem to find a solution? First, we need to identify the root cause of the failure. A common approach is to use the Ishikawa, or Fishbone, diagram to explore the possible causes. As shown in Figure 4, the Fishbone diagram typically uses 5 or 6 bones that emanate from the spine to describe the source of the problem: Man, Machine, Method, Measurement, Materials, and in some cases, Environment. The idea is to brainstorm more specific problems that might fall in these groupings that can lead to the process instability. For example, under machine we might suspect a temperature sensor that has malfunctioned. We would put that in as a secondary bone and then brainstorm for others. Bones can be hierarchically constructed in a fishbone diagram, so a category like temperature sensor may have multiple reasons for malfunctioning.

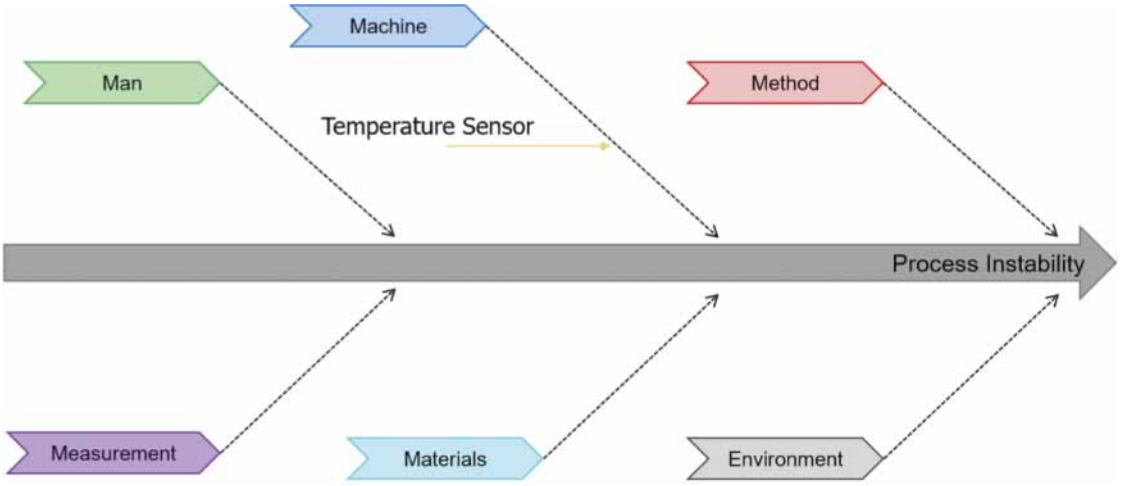

Figure 4. Ishikawa, or Fishbone, Diagram.

Ask the Experts

Q: Is Electromigration as common now as it was in the past on larger geometry parts? What about <28nm parts? Any comments are appreciated?

A: Electromigration is well handled today by design tools, but occasionally there can be issues. Usually, issues result when design engineers do not feed results of thermal analysis and simulation back to the layout engineers. Electromigration rates are strongly dependent on temperature, with higher temperatures leading to more rapid degradation. This lack of feedback and communication can result in metal interconnect that are not robust for the application, since higher temperatures allow for electromigration to proceed more rapidly. In this situation, the interconnect would need to be sized larger to lower the current density and offset the effects of the higher temperatures.

Spotlight: Wafer Fab Processing

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. ***Wafer Fab Processing*** is a 4-day course that offers an in-depth look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we delve into the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the basics of each processing step and the issues surrounding them, participants will learn why certain techniques are preferred over others. Our instructors work hard to explain how semiconductor processing works without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Processing Steps.** Each processing step addresses a specific need in IC creation. Participants learn the fundamentals of each processing step and why they are used in the industry today.
2. **The Evolution of Each Processing Step.** It is important to understand how wafer fab processing came to the point where it is today. Participants learn how each technique has evolved for use in previous and current generation ICs.
3. **Current Issues in Wafer Fab Processing.** Participants learn how many processing steps are increasingly constrained by physics and materials science. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind the fundamental wafer fab processing steps.
3. The seminar will identify the key issues related to each of the processing techniques and their impact on the continued scaling of the semiconductor industry.
4. The seminar offers a wide variety of sample problems that participants work to help them gain knowledge of the fundamentals of wafer fab processing.
5. Participants will be able to identify the basic features and principles associated with each major processing step. These include processes like chemical vapor deposition, ion implantation, lithography, and etching.

6. Participants will understand how processing, reliability, power consumption and device performance are interrelated.
7. Participants will be able to make decisions about how to construct and evaluate processing steps for CMOS, BiCMOS, and bipolar technologies.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

COURSE OUTLINE

Day 1

1. Module 1: Basics & Fundamentals; Semiconductor Devices and ICs
    a. Acronyms
    b. Common Terminology
    c. Brief History
    d. Semiconductor Materials
    e. Electrical Conductivity
    f. Semiconductor Devices
    g. Classification of ICs & IC Processes
    h. Integrated Circuit Types
2. Module 2: Crystallinity, Crystal Defects, Crystal Growth
    a. Crystallinity
    b. Crystal Defects
    c. Crystal Growth
    d. Controlling Crystal Defects
3. Module 3: Basic CMOS Process Flow
    a. Transistors and Isolation
    b. Contacts/Vias Formation
    c. Interconnects
    d. Parametric Testing
4. Module 4: Ion Implantation 1 (The Science)
    a. Doping Basics
    b. Ion Implantation Basics
    c. Dopant Profiles
    d. Crystal Damage & Annealing

5. Module 5: Ion Implantation 2 (Equipment, Process Issues)
    a. Equipment
    b. Process Challenges
    c. Process Monitoring & Characterization
    d. New Techniques

Day 2

6. Module 6: Thermal Processing
    a. Overview of Thermal Processing
    b. Process Applications of SiO2
    c. Thermal Oxidation
    d. Thermal Oxidation Reaction Kinetics
    e. Oxide Quality
    f. Atomistic Models of Thermal Diffusion
    g. Thermal Diffusion Kinetics
    h. Thermal Annealing
    i. Thermal Processing Hardware
    j. Process Control
7. Module 7: Contamination Monitoring and Control
    a. Contamination Forms & Effects
    b. Contamination Sources & Control
    c. Contamination Characterization & Measurement
8. Module 8: Wafer Cleaning
    a. Wafer Cleaning Strategies
    b. Chemical Cleaning
    c. Mechanical Cleaning
9. Module 9: Vacuum, Thin Film, & Plasma Basics
    a. Vacuum Basics
    b. Thin Film Basics
    c. Plasma Basics
10. Module 10: CVD 1 (Basics, LPCVD, Epitaxy)
    a. CVD Basics
    b. LPCVD Films
    c. LPCVD Equipment
    d. Epi Basics
    e. Epi Process Applications
    f. Epi Deposition Process
    g. Epi Deposition Equipment

Day 3

11. Module 11: PVD
    a. PVD (Physical Vapor Deposition) Basics
    b. Sputter Deposition Process
    c. Sputter Deposition Equipment
    d. Al-Based Films
    e. Step Coverage and Contact/Via Hole Filling
    f. Metal Film Evaluation
12. Module 12: Lithography 1 (Photoresist Processing)
    a. Basic Lithography Process
    b. Photoresist Materials
    c. Photoresist Process Flow
    d. Photoresist Processing Systems
13. Module 13: Lithography 2 (Image Formation)
    a. Basic Optics
    b. Imaging
    c. Equipment Overview
    d. Actinic Illumination
    e. Exposure Tools
14. Module 14: Lithgroaphy 3 (Registration, Photomasks, RETs)
    a. Registration
    b. Photomasks
    c. Resolution Enhancement Techniques
    d. The Evolution of Optical Lithography
15. Module 15: Etch 1 (Basics, Wet Etch, Dry Etch)
    a. Etch Basics
    b. Etch Terminology
    c. Wet Etch Overview
    d. Wet Etch Chemistries
    e. Types of Dry Etch Processes
    f. Physics & Chemistry of Plasma Etching

Day 4

16. Module 16: Etch 2 (Dry Etch Applications and Equipment)
    a. Dry Etch Applications
    b. SiO2
    c. Polysilicon
    d. Al & Al Alloys
    e. Photoresist Strip
    f. Silicon Nitride
    g. Dry Etch Equipment
    h. Batch Etchers
    i. Single Wafer Etchers
    j. Endpoint Detection
    k. Wafer Chucks
17. Module 17: CVD 2 (PECVD)
    a. CVD Basics
    b. PECVD Equipment
    c. CVD Films
    d. Step Coverage
18. Module 18: Chemical Mechanical Polishing
    a. Planarization Basics
    b. CMP Basics
    c. CMP Processes
    d. Process Challenges
    e. Equipment
    f. Process Control
19. Module 19: Copper Interconnect, Low-k Dielectrics
    a. Limitations of "Conventional" Interconnect
    b. Copper Interconnect
    c. Cu Electroplating
    d. Damascene Structures
    e. Low-k IMDs
    f. Cleaning Cu and low-k IMDs

20. Module 20: Leading Edge Technologies & Techniques
    a. Process Evolution
    b. Atomic Layer Deposition (ALD)
    c. High-k Gate and Capacitor Dielectrics
    d. Ni Silicide Contacts
    e. Metal Gates
    f. Silicon on Insulator (SOI) Technology
    g. Strained Silicon
    h. Hard Mask Trim Etch
    i. New Doping Techniques
    j. New Annealing Techniques
    k. Other New Techniques
    l. Summary of Industry Trends

References:

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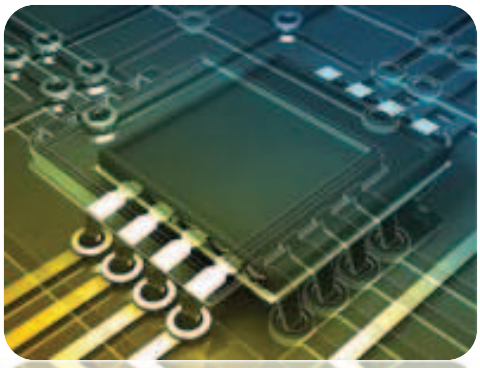

Upcoming Webinars

(Click on each item for details)

Failure and Yield Analysis

4 sessions of 4 hours each
US: November 29 – December 2, 2021
(Mon – Thur), 11:00 A.M. – 3:00 P.M. EST;
8:00 A.M. – 12:00 NOON PST

Advanced CMOS/FinFET Fabrication

4 sessions of 2 hours each
US: December 6 – 9, 2021
(Mon – Thur), 11:00 A.M. – 1:00 P.M. EST;
8:00 A.M. – 10:00 A.M. PST

Wafer Fab Processing

4 sessions of 4 hours each
US: February 28 – March 3, 2022
(Mon – Thur), 11:00 A.M. – 3:00 P.M. EST;
8:00 A.M. – 12:00 noon PST

Semiconductor Reliability / Product Qualification

4 sessions of 4 hours each
US: March 7 – 10, 2022 (Mon – Thur),
11:00 A.M. – 3:00 P.M. EST;
8:00 A.M. – 12:00 noon PST

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.

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We look forward to hearing from you!