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Qualification Process Part 1

By Christopher Henderson

In this article, we will begin to discuss the qualification process. Qualification takes into account the design, package and customer use conditions, so this is a very significant and important topic, especially from the customer's perspective. In part 1 we will cover general concepts associated with product qualification. We will discuss the wafer level reliability tests, standards-based testing, and package stress tests performed during qualification. In part 2, we will provide an overview of product qualification procedures, paying particular attention to the Joint Electron Device Engineering Council (JEDEC) standard, since we qualify most of our components on the basis of this standard. We also cover the Automotive Electronics Council (AEC) standard, briefly cover the Military Standard (MIL-STD), and mention others. We will also walk through the major standards-based tests that we perform when qualifying products.

Assume that I come to you to purchase integrated circuits for an electronics application I am building. I want to make sure that your circuits will work in my application. The challenge is how to demonstrate that. You may provide me with data that indicates in your mind that the product will work in my application, but I may not be convinced. We need a framework upon which we can both agree will demonstrate the "fitness" of your component. There are a number of issues associated with this task. They include new configurations and technologies which introduce changes from

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what was previously done. The complexity of the product can make it challenging, because we may not be able to test or characterize the components fully. The reliability margins of components are shrinking, so we may not simply be able to increase the margin arbitrarily to avoid problems. The component may be used by many different customers in different applications, each with their own needs and objectives. The now-prevalent fabless/foundry model can make it difficult to obtain the necessary data. And finally, there are new failure modes for which we do not have an understanding, nor the models to make accurate predictions.

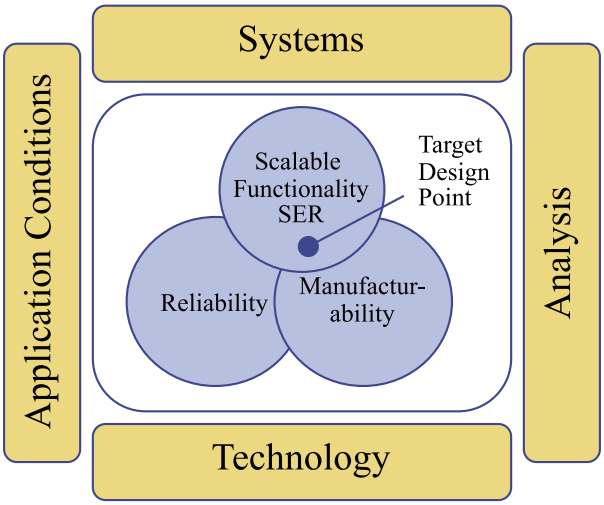


Figure 1.

Product qualification involves a number of requirements. These are typically a set of both electrical and mechanical stresses that are designed to ensure the product will meet all of its specifications under the application use conditions for the desired life of the product. The qualification effort should determine the field failure rates and lifetime expectancies for the component of interest. The results will be unique to the component. Product qualification also includes certification. The manufacturer is required to certify that the product will perform all of its functions as expected and meet its functionality and usability requirements. As the graphic in Figure 1 depicts, there are four areas that feed into this assessment: the top-level system behavior, analysis of the component behavior, its technology, and the application conditions. Furthermore, product qualification involves the intersection of functionality, reliability and manufacturability. A successful component should be able to meet all three at the target design point, like we show in Figure 1.

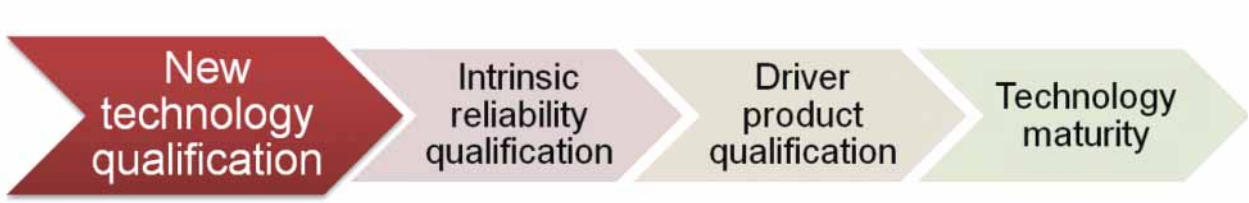


Figure 2.

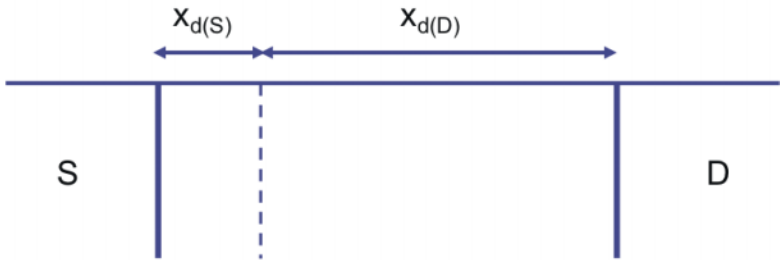
Product qualification involves three major activities: intrinsic reliability qualification, driver product qualification, and technology maturity, where most products undergo qualification. Intrinsic reliability qualification is typically performed in conjunction with technology development, or the development of a new wafer fabrication process. Engineers look for new reliability failure mechanisms, and develop reliability models for designers. They also perform component reliability qualification with test structures and simulation, both at the silicon and package level. Driver product qualification involves qualifying the lead product on the technology. This is typically a product that is a flagship product for a company, and is quite often shipped in high volumes. This would be qualified per JEDEC or the customer's requirements. Once this is complete, the technology enters maturity. We then qualify additional designs using JEDEC, automotive, or other standards-based qualification procedures, or a customer-specific procedure.

[To be continued in the December 2018 Newsletter]

Technical Tidbit

Punch-Through

This month's technical tidbit covers an important device physics concept called punch through. Punch-through is basically a condition where the depletion region from the source merges with the depletion region from the drain. The merging of the depletion regions disrupts the transistor behavior, causing it to conduct higher currents without the ability to control that current using the gate.

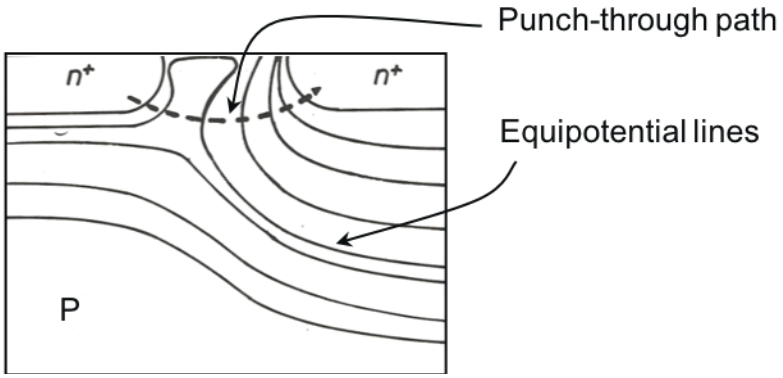


This diagram shows a simplified one-dimensional representation of the onset of punch-through where the source and drain depletions merge. Punch-through is a serious short-channel effect. For V_D less than the punch-through voltage, the drain field lines end on the ionized impurities in the channel. However, at punch-through the drain field lines begin to end directly on the source electrons. At that point all available channel ions are "imaged" on drain, and the drain current becomes almost independent of gate voltage. For the drain voltage greater than the punch-through voltage, the source is forward-biased by the drain bias. The current increases exponentially according to this equation:

$$I_{PT} \cong I_{PT0} e^{\frac{aq(V_D - V_{PT})}{kT}}$$

where "a" is a fitting parameter greater than one, and IPT zero is the drain current at onset of punch-through.

It should be noted that punch-through is a two-dimensional effect, and occurs deeper in the channel where the gate provides less control. Evaluating punch-through can be challenging, because non-uniform doping profiles, junction curvature and the gate all affect its behavior.



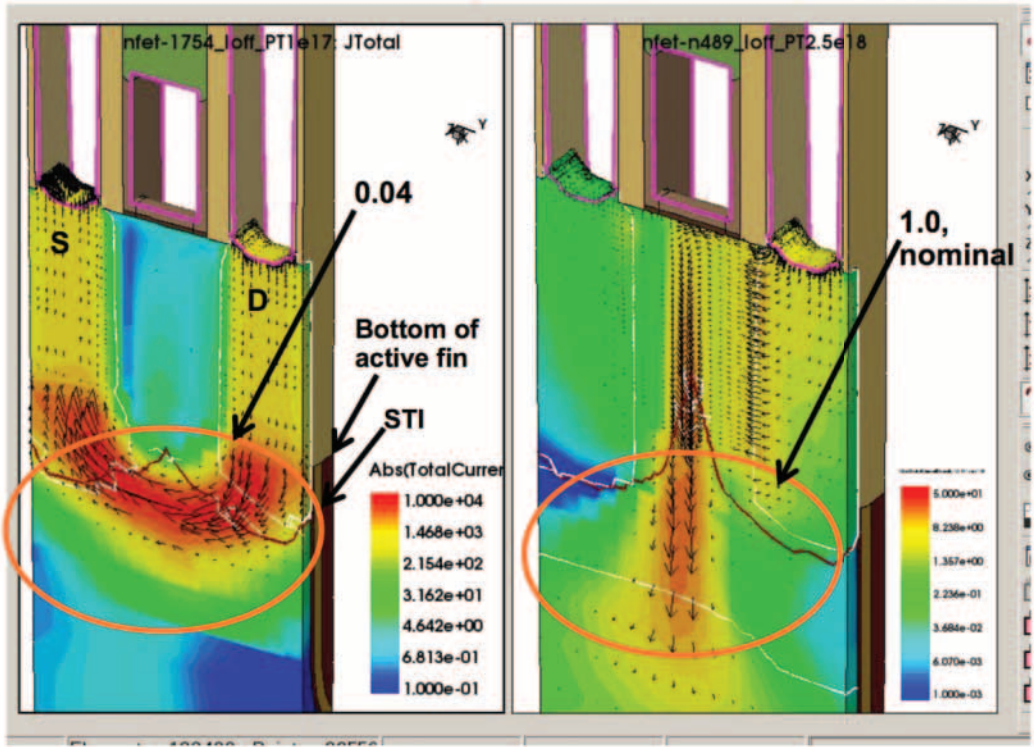
It can be approximated through this equation:

$$V_{PT} \cong L_{eff}^2 \frac{qN_A}{2\varepsilon_{Si}} = 7.72x10^{-8} L_{eff}^2 N_A$$

where the punch-through voltage is a function of the square of the effective channel length, the number of acceptors in the silicon, and the dielectric constant of the silicon.

One can draw several conclusions from the previous equation. We summarize them here. For a given dopant concentration, punch-through voltage increases with increasing channel length. For a given channel length, the punch-through voltage increases with dopant concentration. So, to reduce the effective channel length while avoiding punch-through the body doping level should increase, but this affects mobility. Increasing the junction depth and body-bias also reduces punch-through susceptibility. However, all of the above steps impact performance to varying degrees, so trade-offs must be made. Angled implantation—such as halo implants, pocket implants and the like—partially solves this problem.

Punch-through is not only a problem with planar transistors, but it can also affect FinFETs. This image shows a TCAD plot of substrate (punch-through) leakage, with V_g=0 and V_d=V_{dd}, and relative arbitrary substrate doping values of 1.0 for the nominal condition, and 0.04 for the lightly doped condition.



With low doping, the depletion region reaches from Drain to Source and punch-through leakage current flows below the active fin. With high or nominal doping, the depletion region is much reduced and punch-through leakage is cut off.

Ask the Experts

Q: What is LVS, or Layout Versus Schematic?

A: Layout versus Schematic, or LVS, is a process used to verify that the layout implements the design that the designers intended. Basically, a software algorithm examines the layout database of the chip and re-constructs the transistors and interconnect, and then compares them to the original design. This step is very important in the design verification process to help reduce the possibility of mistakes.

Spotlight: Advanced CMOS/FinFET Fabrication

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" Advanced CMOS/ FinFET Fabrication is a 1-day course that offers detailed instruction on the processing used in a modern integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

WHAT WILL I LEARN BY TAKING THIS CLASS

By concentrating on the latest developments in CMOS and FinFET technology, participants will learn why FinFETs and FD-SOI are fast becoming the technologies of choice at feature sizes below 20nm. Our instructors work hard to explain semiconductor processing without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants learn basic but powerful aspects about FinFET technology. This skill-building series is divided into four segments:

1. Front End Of Line (FEOL) Overview. Participants study the major developments associated with FEOL processing, including ion implantation, Rapid Thermal Annealing (RTA) for implants and silicides, and Pulsed Plasma Doping. They also study alternate substrate technologies like SOI as well as High-k/Metal Gates for improved leakage control.
2. Back End Of Line (BEOL) Overview. Participants study the major developments associated with BEOL processing, including copper metallization and Low-k Dielectrics. They learn about why they're necessary for improved performance.
3. FinFET Manufacturing Overview. Participants learn how semiconductor manufacturers are currently processing FinFET devices and the difficulties associated with three-dimensional structures from a processing and metrology standpoint.
4. FinFET Reliability. They also study the failure mechanisms and techniques used for studying the reliability of these devices.

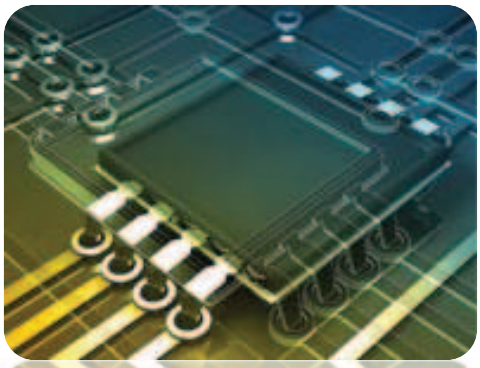
COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of SOI technology and the technical issues.
2. Participants will understand how Hi-K/Metal Gate devices are manufactured.
3. Participants will also understand how FinFET devices are manufactured.
4. The seminar provides a look into the latest challenges with copper metallization and Low-k dielectrics.
5. Participants will understand the difficulties associated with non-planar structures and methods to alleviate the problems.
6. Participants will be able to make decisions about how to evaluate FinFET devices and what changes are likely to emerge in the coming years.
7. Participants will briefly learn about IC reliability and the failure modes associated with these devices.
8. Finally, the participants see a comparison between FD-SOI (the leading alternative) and FinFETs.

COURSE OUTLINE

1. Advanced CMOS Fabrication – Introduction
2. Front End Of Line (FEOL) Processing
    a. SOI and FD-SOI
    b. Ion Implantation and Rapid Thermal Annealing
    c. Pulsed Plasma Doping
    d. Hi-K/Metal Gates
    e. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology
3. Back End Of Line (BEOL) Processing
    a. Introduction and Performance Issues
    b. Copper
        i. Deposition Methods
        ii. Liners
        iii. Capping Materials
        iv. Damascene Processing Steps
    c. Lo-k Dielectrics
        i. Materials
        ii. Processing Methods
    d. Reliability Issues

4. FinFET Manufacturing Overview
    a. Substrates
        i. Bulk
        ii. SOI
    b. FinFET Types
    c. Process Sequence
    d. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology
5. FinFET Reliability
    a. Defect density issues
    b. Gate Stack
    c. Transistor Reliability (BTI and Hot Carriers)
    d. Heat dissipation issues
    e. Failure analysis challenges
6. Future Directions for FinFETs
    a. Comparison of FD-SOI and FinFETs – Are FinFETs a better choice?
    b. Scaling



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Failure and Yield Analysis
April 23 – 26, 2019 (Tue – Fri)
Munich, Germany

Wafer Fab Processing
April 23 – 26, 2019 (Tue – Fri)
Munich, Germany

EOS, ESD and How to Differentiate
April 29 – 30, 2019 (Mon – Tue)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 6 – 9, 2019 (Mon – Thur)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 13 – 16, 2019 (Mon – Thur)
Tel Aviv, Israel

Introduction to Processing
June 3 – 4, 2019 (Mon – Tue)
San Jose, California, USA

Failure and Yield Analysis
June 3 – 6, 2019 (Mon – Thur)
San Jose, California, USA

Advanced CMOS/FinFET Fabrication
June 5, 2019 (Wed)
San Jose, California, USA

Interconnect Process Integration
June 6, 2019 (Thur)
San Jose, California, USA