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Semitracks Monthly Newsletter

Optical Pyrometry Part 2

By Christopher Henderson

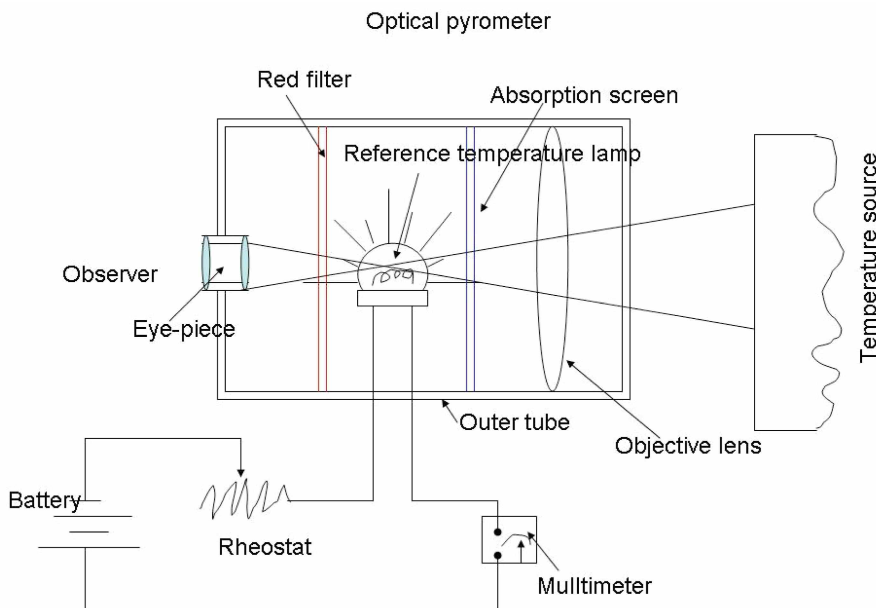

Figure 4. Equipment: classical system.

Optical pyrometry has been in use for over 100 years. This graph shows the basic concept behind a simple optical pyrometer. The system records the color variation with the change in temperature as an index of the temperature. This optical pyrometer compares the brightness of image produced by the temperature source with that of

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a reference temperature lamp. The current in the lamp is adjusted until the brightness of the lamp is equal to the brightness of the image produced by the temperature source. Since the intensity of light of any wavelength depends on the temperature of the radiating object, the current passing through the lamp becomes a measure of the temperature of the temperature source when calibrated. The main components within an optical pyrometer are:

- An eye piece at one end and an objective lens at the other end.
- A power source (battery), rheostat and millivolt meter (to measure current) connected to a reference temperature bulb.
- An absorption screen is placed in between the objective lens and reference temperature lamp. The absorption screen is used to increase the range of the temperature which can be measured by the instrument.
- The red filter between the eye piece and the lamp allows only a narrow band of wavelength of around 0.65 microns.

There are several advanced features associated with optical pyrometry that we should mention. First, modern pyrometers are electronically-driven, which makes them faster and more accurate. Second, modern pyrometers can use optical fiber to better gather light in tight or inaccessible locations. Third, modern pyrometers can sense infrared light at multiple frequencies to provide a more accurate reading. And fourth, some state-of-the-art pyrometry systems might use Raman techniques, since Raman techniques can allow for more accurate temperature determination.

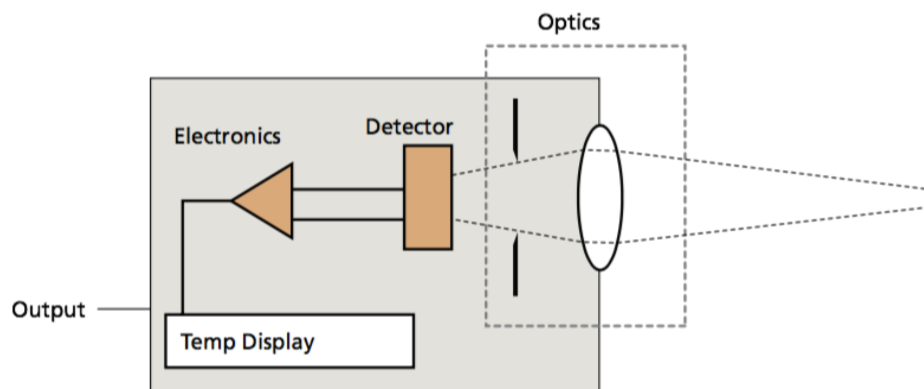


Figure 5. Modern electronic pyrometer.

A modern pyrometer is electronic. These systems quite often use different detector formats that fit the application of interest. One important concept is to use a portion of the spectrum where there is significant change in emissivity over the temperature range of interest. This can make the determination of the temperature more accurate. This is a significant issue at longer wavelengths, where the emissivity

is relatively constant at higher temperatures. Figure 5 shows a typical setup for the electronics in optical pyrometry. The signals generated typically range from zero to ten volts, and four to twenty milliamps.

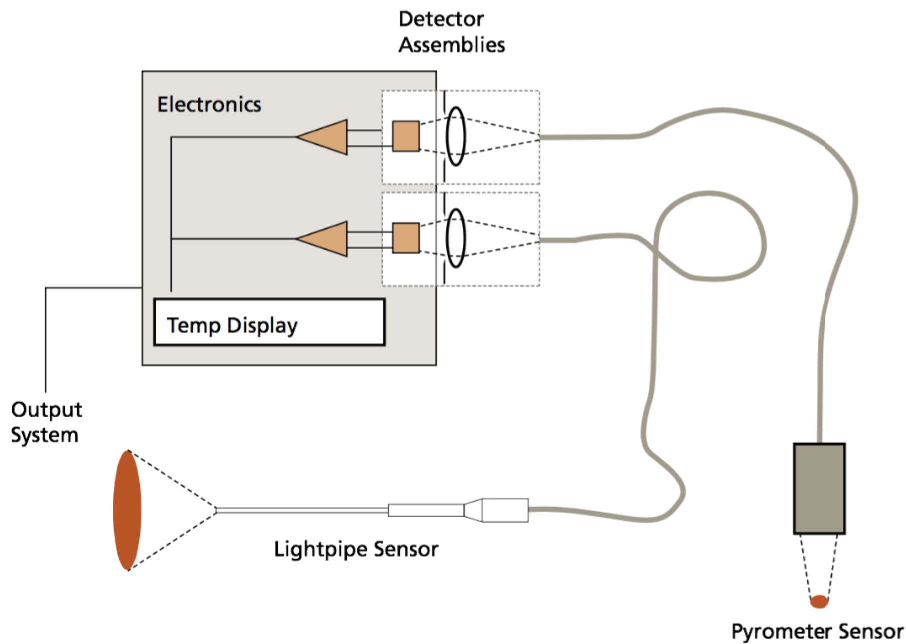


Figure 6. Optical fiber.

The optical fiber pyrometer is another important development. This concept was implemented in the 1980s. An optical fiber to the pyrometer sensor helps avoid reflection problems from the heaters in the chamber. The heating elements are very hot, and emit their own signals that can reflect off the sample and into the sensor. The fiber helps avoid signals from other hot objects in the chamber, like the chamber walls, wafer clamps, and so on. It also helps avoid configuration issues where the light from the sample can't easily reach the detector in a straight line.

Another development in the 1990s for optical pyrometry was the introduction of multiple frequencies, or examination at specific frequencies. For example, one can use a filter with a narrow frequency range that operates at 9.4 microns with a plus or minus 0.3 micron to evaluate thin films of oxide on a silicon

substrate. By matching the wavelength to a particular silicon-oxygen bond frequency, one can provide more sensitive results.

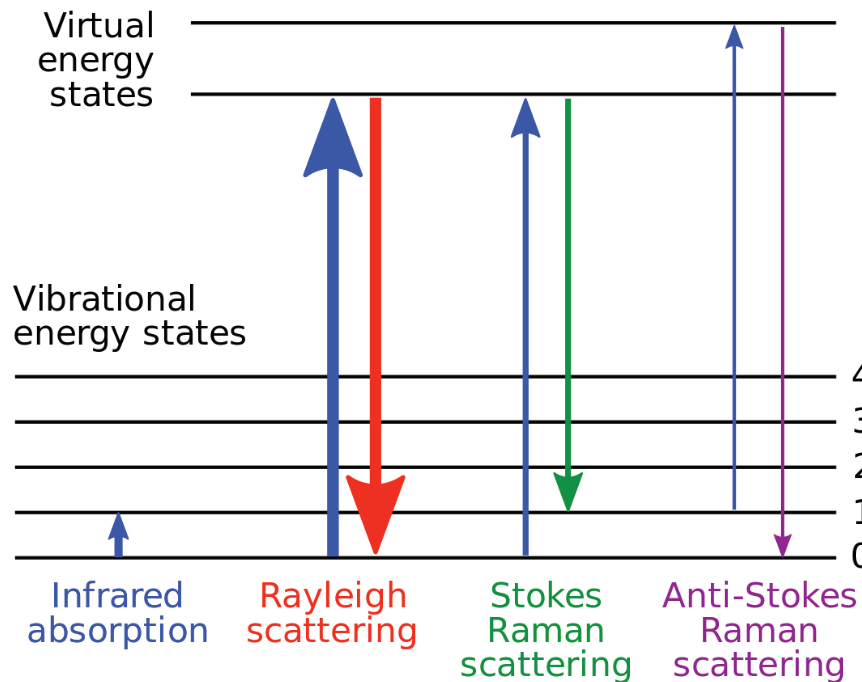


Figure 7. Raman spectroscopy.

Another concept is to use Raman Spectroscopy to measure temperature. This is a possible extension of the optical pyrometer concept to provide more flexibility and accuracy for measuring temperature. The challenge with this approach is the cost associated with the measurement and detection electronics.

There are several important issues with optical pyrometry as a technique. First, there is the issue of noise from reflections. Reflections from other hot objects such as heating elements can lead to noise in the measurement system. This type of noise can be minimized through the use of optical fiber paths. However, a fiber only collects light from a limited area, so multiple measurements might be required then. Second, the thin films on the wafer surface can lead to difficulties in obtaining an accurate temperature. One way to avoid this is to measure from the wafer backside, but that may not be practical in some tools. Furthermore, the backside temperature may not correspond well to the front side wafer temperature. The film thickness and the film stresses can distort the temperature measurements, creating errors. And third, gases in the chamber can absorb different wavelengths, creating errors in the temperature measurement process.

Optical pyrometry has several advantages as a measurement technique.

- Physical contact of the instrument is not required to measure temperature of the temperature source.
- Accuracy can be fairly high, to within + or – 5°C.
- Provided a proper sized image of the temperature source is obtained in the instrument, the

distance between the instrument and the temperature source doesn't matter.

- The instrument is easy to operate.

However, there are several limitations with the technique.

- Temperatures of more than 700°C can only be measured since illumination of the temperature source is a must for measurement. However, there are newer techniques that allow for readings at lower temperatures.
- Since it is manually operated, it cannot be used for the continuous monitoring and controlling purpose.

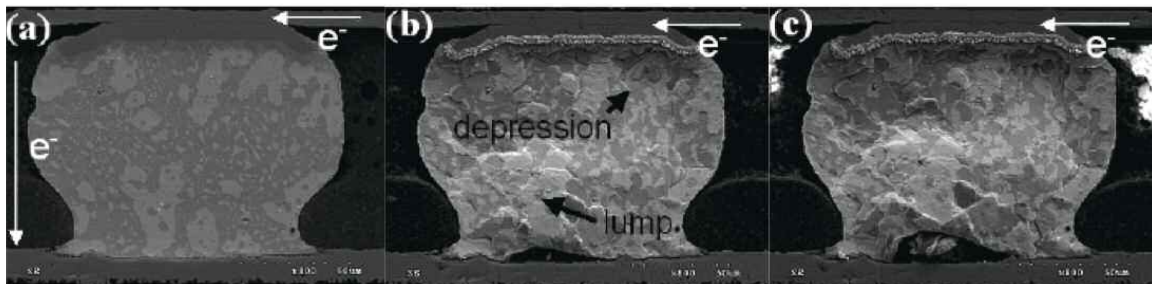
In conclusion, optical pyrometry is a common technique for measuring high temperatures that are common in Chemical Vapor Deposition, Rapid Thermal Processing, Czochralski Growth, and other wafer fabrication processes. It is a non-contact technique, so there is no risk of damage to the wafer during processing. Engineers have made a number of improvements over the past 20 years, allowing for more accurate temperature measurements. There are several issues associated with optical pyrometry and accurate temperature measurement. They include noise from reflections, films on the wafer surface, and gases in the chamber. The use of better filters as well as Raman techniques may provide an avenue to improve this technique further in the future.

Technical Tidbit

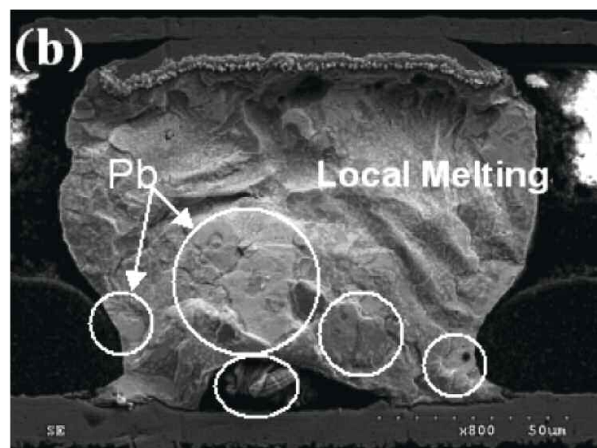
Electromigration in Solder Bumps

In this month's technical tidbit, we will discuss electromigration, but in a different location – the solder bump.

Electromigration is an important failure mechanism in solder bumps. In fact, solder bumps can be very susceptible to electromigration. If the current density is above about $1x10^4$ amps/cm^2, electromigration can occur. This is a much lower density than what it takes to create electromigration in metal systems on the chip. This problem is getting worse as the solder bump sizes get smaller. Electromigration voiding leads to resistance increases. A problem that is related to electromigration is thermomigration, or the movement of tin or lead under a thermal gradient. This can also lead to a resistance increase. We show some examples of electromigration below.



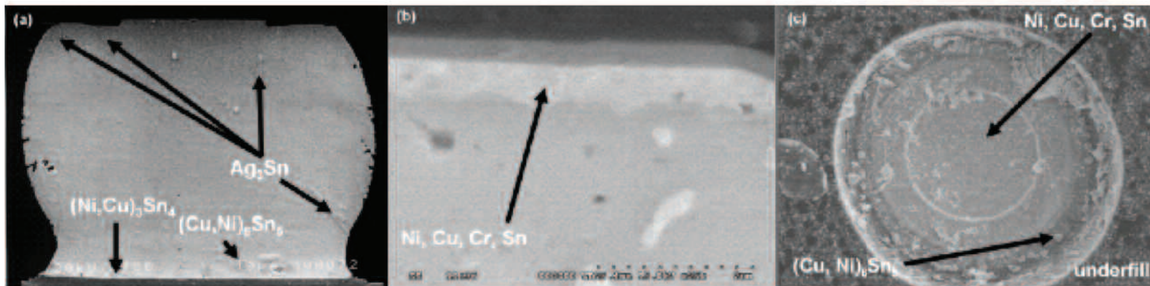
As the resistance increases, this can also lead to heating. If the temperature climbs enough then the solder can actually melt, causing the solder joint to fail. The image below shows an example of localized melting within the solder joint, highlighted by the white circles.



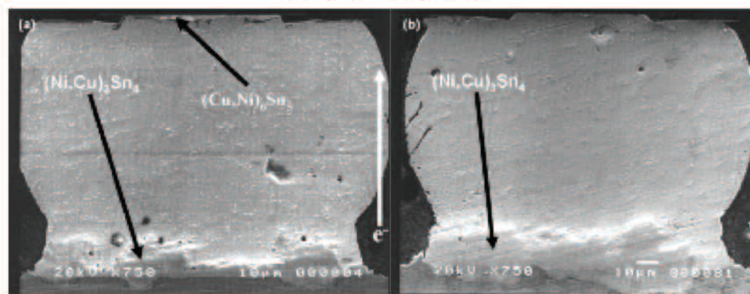
In order to minimize the possibility of electromigration, one needs to achieve good wetting between the pad and the solder ball to help increase the cross-sectional area. To accomplish this, one should use as large a pad as possible, and use a barrier metal. Also, using solder materials with higher melting

temperatures help. SAC solder balls will have better electromigration performance than lead-tin solder balls.

Before Stress



After Stress



Simply using SAC solders does not solve the problem though. One must pay attention to the current through the balls. The images above show examples of electromigration failures. On the left we show a cross-sectional SEM image of a flip-chip SAC305 bump before current stressing. In the center we show an enlarged SEM image on the interface of the solder and the chip-side UBM. On the right we show a plan-view SEM image of the chip side without current stressing, in which SAC305 solder has been selectively etched away. The images above at the bottom are cross-sectional SEM images of the flip chip package after stressing with the current density of 1×10^4 A/cm^2 at 150°C for 22 hours.

Electromigration and the associated heating can lead to increased intermetallic formation. The images above are plan-view SEM images of the flip chip package. The image on the left shows the anode/chip side after stressing with the current density of 1×10^4 A/cm^2 at 150°C for 12 hours. The image in the center shows the cathode/chip side after stressing with the current density of 1×10^4 A/cm^2 at 150°C for 12 hours, and the image on the right shows the chip side after aging at 150°C for 12 hours without current stressing.

Ask the Experts

Q: I came across the term “deglaze.” What does this term mean?

A: Engineers use the term “deglaze” sometimes to refer to removal of a thin oxide layer. In particular, we would use the term to refer to the removal of an oxide layer that would be created through a thermal process, either intentionally, like a sacrificial oxide layer, or as a by-product of another thermal process, that oxidizes the surface of either the silicon or polysilicon.

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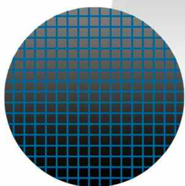


SEMITRACKS, INC.

Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

Spotlight: Semiconductor Reliability and Product Qualification

OVERVIEW

Package reliability and qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. in particular, the proliferation of new package types. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. While customers expect high reliability levels, incorrect testing, calculations, and qualification procedures can severely impact reliability. Your company needs competent engineers and scientists to help solve these problems. ***Semiconductor Reliability and Product Qualification*** is a four-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability and qualification. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

What Will I Learn By Taking This Class?

Participants learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions and their parameters.
2. **Failure Mechanisms.** Participants learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die and at the package level. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, etc.
3. **Qualification Principles.** Participants learn how test structures can be designed to help test for a particular failure mechanism.
4. **Test Strategies.** Participants learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.
2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.
3. The seminar will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.
4. The seminar offers a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.

6. Participants will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

COURSE OUTLINE

Day 1 (Lecture Time 8 Hours)

1. Introduction to Reliability
    1. Basic Concepts
    2. Definitions
    3. Historical Information
2. Statistics and Distributions
    1. Basic Statistics
    2. Distributions (Normal, Lognormal, Exponent, Weibull)
    3. Which Distribution Should I Use?
    4. Acceleration
    5. Number of Failures

Day 2 (Lecture Time 8 Hours)

1. Overview of Die-Level Failure Mechanisms
    1. Time Dependent Dielectric Breakdown
    2. Hot Carrier Damage
    3. Negative Bias Temperature Instability
    4. Electromigration
    5. Stress Induced Voiding
2. Package Level Mechanisms
    1. Ionic Contamination
    2. Moisture/Corrosion
        1. Failure Mechanisms
        2. Models for Humidity
        3. Tja Considerations
        4. Static and Periodic stresses
        5. Exercises
    3. Thermo-Mechanical Stress
        1. Models
        2. Failure Mechanisms
    4. Interfacial Fatigue
        1. Low-K fracture
    5. Thermal Degradation/Oxidation

Day 3 (Lecture Time 8 Hours)

1. Package Attach (Solder) Reliability
    1. Creep/Sheer/Strain
    2. Lead-Free Issues
    3. Electromigration/Thermomigration
    4. MSL Testing
    5. Exercises
2. TSV Reliability Overview
3. Board Level Reliability Mechanisms
    1. Interposer
    2. Substrate
4. Electrical Overstress/ESD
5. Test Structures and Test Equipment
6. Developing Screens, Stress Tests, and Life Tests
    1. Burn-In
    2. Life Testing
    3. HAST
    4. JEDEC-based Tests
    5. Exercises

Day 4 (Lecture Time 8 Hours)

1. Calculating Chip and System Level Reliability
2. Developing a Qualification Program
    1. Process
    2. Standards-Based Qualification
    3. Knowledge-Based Qualification
    4. MIL-STD Qualification
    5. JEDEC Documents (JESD47H, JESD94, JEP148)
    6. AEC-Q100 Qualification
    7. When do I deviate? How do I handle additional requirements?
    8. Exercises and Discussion

INSTRUCTIONAL STRATEGY

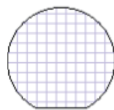
By using a combination of instruction by lecture, video, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

The Semitracks Analysis Instructional Videos™

One unique feature of this workshop is the video segments used to help train the students. Reliability Analysis is a visual discipline. The ability to identify nuances and subtleties in graphical data is critical to locating and understanding the defect. Some tools output video images that must be interpreted by engineers and scientists. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).



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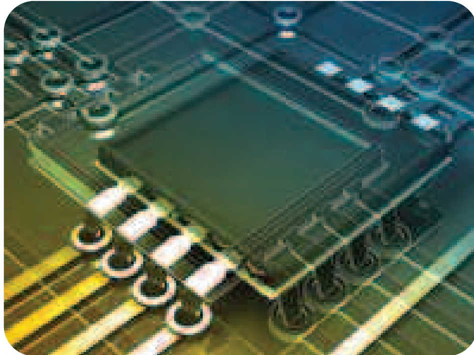
Registration is available at www.irps.org

Chris Henderson, Semitracks President

Chris would be happy to meet with you and discuss any training needs you have. Contact him at henderson@semitracks.com anytime before the symposium!



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Failure and Yield Analysis
March 19 – 22, 2018 (Mon – Thur)
San Jose, California, USA

Semiconductor Reliability / Product Qualification
March 26 – 29, 2018 (Mon – Thur)
Portland, Oregon, USA

Failure and Yield Analysis
April 9 – 12, 2018 (Mon – Thur)
Munich, Germany

Wafer Fab Processing
April 9 – 12, 2018 (Mon – Thur)
Munich, Germany

Semiconductor Reliability / Product Qualification
April 16 – 19, 2018 (Mon – Thur)
Munich, Germany

CMOS, BiCMOS and Bipolar Process Integration
September 10 - 12, 2018 (Mon – Tue)
San Jose, California, USA