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Leadframes—Part I

By Christopher Henderson

In this two-part article we will discuss leadframes for use in IC packaging. The leadframe creates an electrical connection between the perimeter of the die and the outside of the package. Typically, manufacturers use bondwires to connect the leadframe to the die bond pads. Keep watching to learn more about this technology.

The outline for this section is shown here. First we will discuss stamped leadframes. This is a cost-effective high volume approach but has high non-recurring engineering costs. Next we will discuss etched leadframes. This has a lower non-recurring engineering cost, but typically costs more in high volume production. We'll then discuss leadframe materials, followed by leadframe plating materials and techniques.

Let's begin with a brief overview. We use the leadframe to make electrical connections to the printed circuit board. The leadframe is one of two major techniques for making the connection to the circuit board; the other is the use of solder balls, a process known as bumping. The leadframe approach is the oldest and more mature of the processes. We can create leadframes through two processes: stamping or etching to create geometries we need. We can plate leadframes to improve bonding, corrosion resistance and solderability. We create leadframes from various metals, but the primary metal is copper. Manufacturers process most leadframes in long coils, approximately 900 feet or longer.

Engineers prefer stamped leadframes for high volume manufac-

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turing. This is a low cost manufacturing option, but the tooling is more expensive. The tooling can run into the hundreds of thousands of dollars to buy the machinery and create the punch die. There is typically a long lead time as well. In high volume manufacturing though, the advantages of the low unit cost will still outweigh the up-front tooling costs and times. Older leadframe strips are typically around 30 millimeters in width, while newer leadframes are typically 250 by 70 millimeters. This facilitates higher volumes.

In order to create the shape of the leads in the leadframe, we require a set of stamping dice. These die are made from hard materials like silicon carbide, so that they can punch through many copper lead-frames without degrading the dice. This image shows a set of stamping dice for a leadframe.

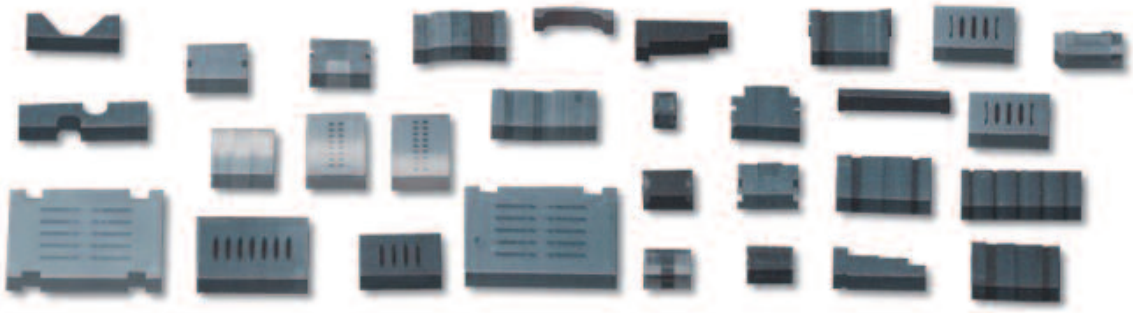


Figure 1. Stamping die set for a leadframe.

The stamping process occurs in a pipeline fashion. The machine feeds the leadframe in stages and a heavy plate, containing the stamp die set, stamps the portions sequentially. This machine is relatively ex-pensive, so there is a higher non-recurring engineering cost, but once we purchase the machinery and the die stamp set, it produces a low cost leadframe, on the order of one cent per part or even less. The top image shows the machinery, while the bottom image shows the stamp sequence. The stamp sequence proceeds from left to right. In order to reduce stress on the copper and the machinery, one stamps a small section at a time, so the stamp may need to run more than 20 times to stamp the pattern to create the leadframe.

Figure 2. Stamping machinery.

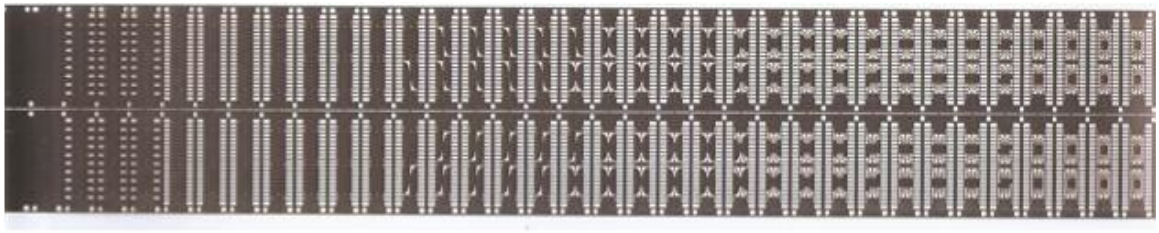


Figure 3. Leadframe showing progressive stamping. The machine would feed the strip from left to right.

The second major technique for creating a leadframe is the etch technique. Etching is a sort of chemical stamping or milling. The advantages include faster turn-around times, a low initial cost for tooling, more options for form factors, and lower stress leadframes. The non-recurring engineering costs are much lower, on the order of $5000, and the turn-around time is around 6 weeks. The images on the right show the impact of the stress on the copper from the stamping and etching. Notice the deformation in the copper with the stamped process that introduces stress into the copper. The disadvantages include higher costs for volume production on some leadframe formats, and the inability to create some patterns. Many companies might start their new products with an etched leadframe, and then when volumes ramp, go to a stamped leadframe. The Quad Flat No-Lead, or QFN, is typically done as an etched leadframe. One can

etch the leadframe in such a way as to achieve a scalloped surface to facilitate mold locking. The scallops prevent the leads from falling out or being pulled out during later assembly steps.

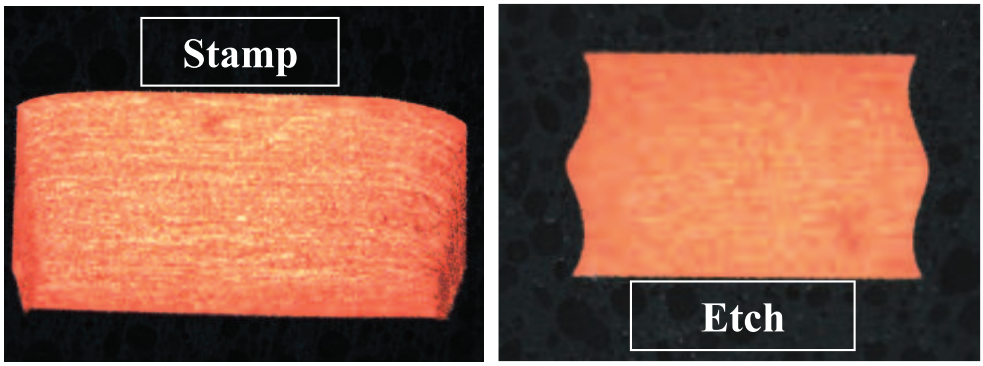


Figure 4. Cross-section of a stamped leadframe (left) and an etched leadframe (right).

There are several common materials used for leadframes. One material used early on in the semiconductor industry was Invar or Alloy 42. Alloy 42 is a mixture of iron and nickel. Although Alloy 42 is not as conductive as copper, it does have the advantage in that it doesn't form a troublesome intermetallic with the tin plating. It also has a low coefficient of thermal expansion, which can help prevent stress problems at the die level. The more common leadframe materials today are copper and its alloys. While pure copper can be used, a copper alloy lead frame like copper-iron, copper-chromium, copper-nickel-silicon, or copper-tin, can have better hardness properties, which reduce bending and deformation during the assembly process and in more aggressive thermal cycling situations. The challenge is to increase hardness without increasing the resistance too much, since an element alloyed with copper will increase the resistance.

Next month we will discuss leadframe platings and their effect on the leadframe and packaging process.

Technical Tidbit

I2C Interface

This month's technical tidbit describes the Inter-Integrated Circuit Interface, or I2C interface. It is a two-wire interface that is gaining increased acceptance as an analog design for test technique to test complex analog circuits.

The I2C interface was developed by Philips Electronics in the early 1980s as a method to attach low speed peripherals to a personal computer. Although this interface has long since disappeared for personal computer devices in favor of the Universal Serial Bus, it still is used for testing purposes on integrated circuits. Although the original specification for I2C called for a 100kHz operating frequency, newer versions of the I2C standard run at frequencies as high as 5MHz.

This drawing shows a block diagram of the I2C interface. There are two pins that interface to the outside world, SDA, the data line, and SCL, the clock line. This extremely low pin count interface is popular for circuits with limited pins, as this interface can be implemented with just two pins. Basically, one microcontroller acts as a master device, and the rest of the devices then operate as slaves to the master. The I2C bus uses pull-up resistors to the power supply, so the combination of those resistors and the capacitance of the SDA and SCL lines limit the frequency of operation.

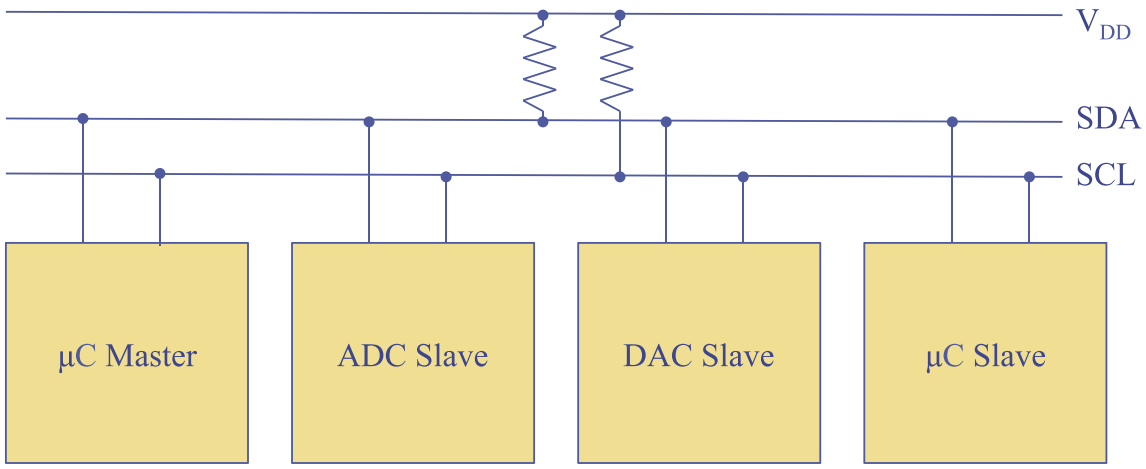


Figure 1. I2C Bus block diagram.

There are four operating modes for the I2C interface: master transmit, master receive, slave transmit, and slave receive. The most common data and address format is 7-bits, but some versions run with 10-bits. Data transfer is initiated with the Start bit when SDA is pulled low while SCL stays high. Then, SDA sets the transferred bit while SCL is low (blue) and the data is sampled (received) when SCL rises (green). When the transfer is complete, a Stop bit is sent by releasing the data line to allow it to be pulled up while SCL is constantly high. In order to avoid false marker detection, the level on SDA is changed on the falling edge and is captured on the rising edge of SCL. The address and data arrive with the most significant bit first.

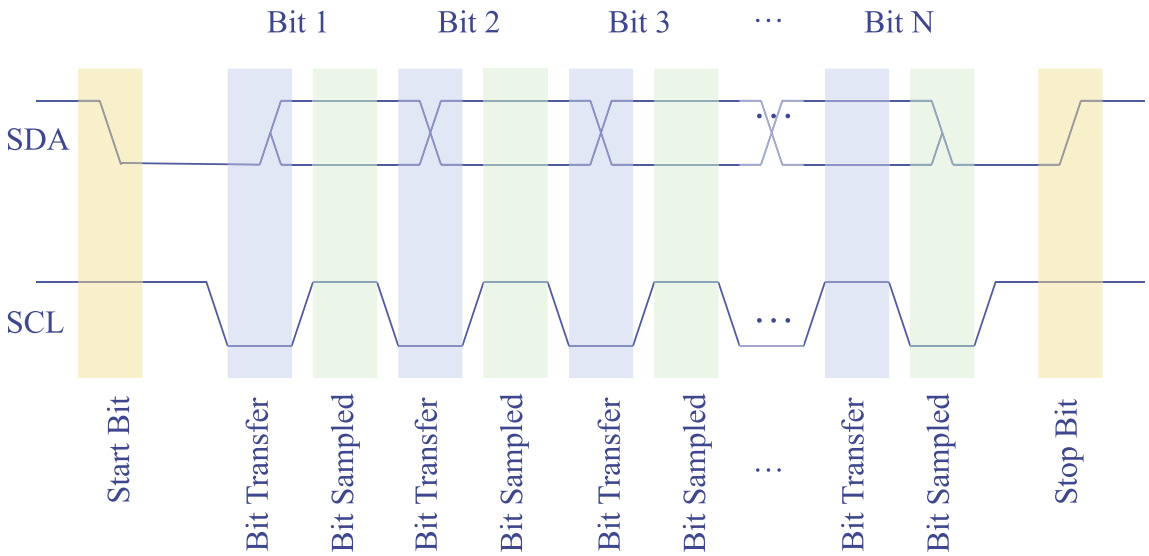


Figure 2. Bus Protocol for I2C Interface.

An example of a chip that uses this interface is Linear Technology's LTC2309, an 8-channel, 12-bit Successive Approximation Register (SAR) Digital-to-Analog Converter (DAC). The data input to the DAC uses the I2C interface.

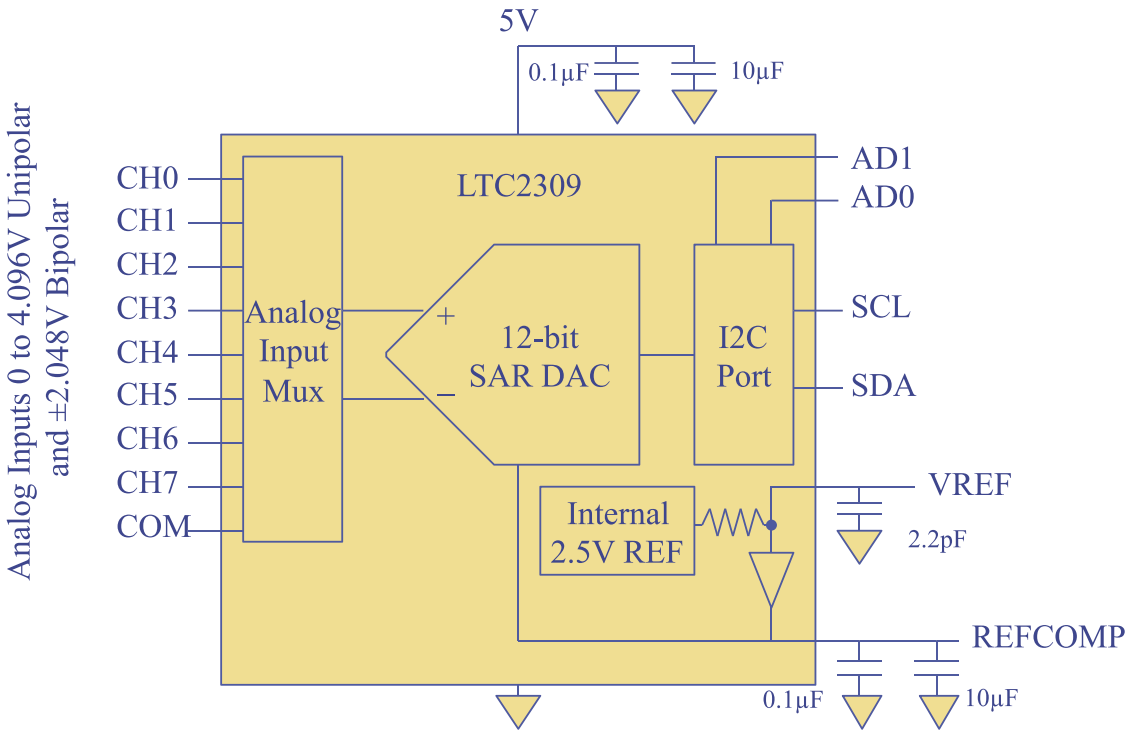


Figure 3. Linear Technology's LTC2309 uses the I2C bus as an interface to the DAC.

Ask the Experts

Q: Why do some suppliers sell Copper Alloy lead frames rather than just pure copper lead frames?

A: A copper alloy lead frame (like Cu-Fe, Cu-Cr, Cu-Ni-Si, or Cu-Sn) can have better hardness properties which reduce bending and deformation during the assembly process and in more aggressive thermal cycling situations. The challenge is to increase hardness without increasing the resistance too much, since an element alloyed with copper will increase the resistance.

Spotlight: Product Qualification

OVERVIEW

Package reliability and qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can also involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. In particular, the proliferation of new package types can create difficulties. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. Customers expect fast, smooth qualification, but incorrect assumptions, use conditions, testing, calculations, and qualification procedures can severely impact this process. Your company needs competent engineers and scientists to help solve these problems. ***Product Qualification*** is a two-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor technology and product qualification. This course is designed for every manager, engineer, and technician concerned with qualification in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

Participants learn to develop the skills to determine the best process for qualification, how to identify issues and how to resolve them.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions and relationship to qualification.
2. **Failure Mechanisms.** Participants learn how product qualification and failure mechanisms relate to one another. We provide an overview of these mechanisms. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, EOS, ESD, latchup, drop tests, etc.
3. **Qualification Principles.** Participants learn how test structures can be designed to help test for a particular failure mechanism.
4. **Test Strategies.** Participants learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to qualify today's components.
2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.
3. The seminar will identify major failure mechanisms; explain how they are observed, how they are modeled, and how they are handled in qualification.

4. The seminar will discuss the major qualification processes, including JEDEC JESD47, AEC Q-100, MIL-STD, and other related documents.
5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.
6. Participants will be able to knowledgeably implement additional tests that are appropriate to assure the reliability of a component.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

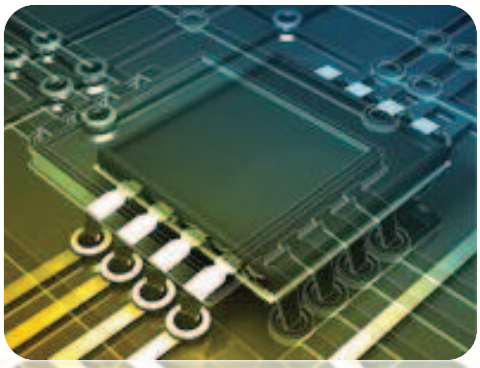
COURSE OUTLINE

1. Introduction to Reliability
   a. Basic Concepts
   b. Definitions
   c. Historical Information
2. Statistics and Distributions
   a. Basic Statistics
   b. Distributions (Normal, Lognormal, Exponent, Weibull)
   c. Which Distribution Should I Use?
   d. Acceleration
   e. Number of Failures
3. Overview of Die-Level Failure Mechanisms
   a. Time Dependent Dielectric Breakdown
   b. Hot Carrier Damage
   c. Negative Bias Temperature Instability
   d. Electromigration
   e. Stress Induced Voiding

4. Overview of Package Level Mechanisms
   a. Ionic Contamination
   b. Moisture/Corrosion
   c. Thermo-Mechanical Stress
   d. Interfacial Fatigue
   e. Thermal Degradation/Oxidation
   f. Solder Joint Reliability
5. Overview of Board Level Reliability
   a. Solder Joint Reliability
   b. EOS/ESD/LatchUp
   c. Single Event Effects

Day Two (Lecture Time 8 Hours)

6. Test Structures and Test Equipment
7. Developing Screens, Stress Tests, and Life Tests
   a. Burn-In
   b. Life Testing
   c. HAST
   d. JEDEC-based Tests
   e. Exercises
8. Developing a Qualification Program
   a. Process
   b. Standards-Based Qualification
   c. Knowledge-Based Qualification
   d. MIL-STD Qualification
   e. JEDEC Documents (JESD47H, JESD94, JEP148)
   f. AEC-Q100 Qualification
   g. When do I deviate? How do I handle additional requirements?
   h. Exercises



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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
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Upcoming Courses

(Click on each item for details)

Wafer Level Chip Scale Packaging
December 16 – 17, 2013 (Mon – Tue)
Malaysia

Copper Pillar Technology and Challenges
December 19 – 20 2013 (Thur – Fri)
Malaysia

CMOS, BICMOS and Bipolar Process Integraion
January 21 – 23, 2014 (Tue – Thur)
San Jose, California, USA

ESD Design and Technology
February 11 – 13, 2014 (Tue – Thur)
San Jose, California, USA

Semiconductor Reliability
February 11 – 13, 2014 (Tues – Thur)
San Jose, California, USA

Failure and Yield Analysis
February 17 – 20, 2014 (Mon – Thur)
San Jose, California, USA

Wafer Fab Processing
February 18, 2014 (Tue)
San Jose, California, USA

Microelectronic Defect, Fault Isolation and Failure Analysis
February 19 – 21, 2014 (Wed – Fri)
Malaysia

Microelectronic Defect, Fault Isolation and Failure Analysis
February 24 – 26, 2014 (Mon – Wed)
Singapore