

# InfoTracks

Semitracks Monthly Newsletter



## Reliability Test Equipment: Wafer Level, Part 1

By Christopher Henderson

In Part 1 of this document, we will cover reliability test equipment. The appropriate test equipment is essential for conducting reliability studies. In addition, one must know how to set up the equipment and understand issues related to cabling, noise, and long-term testing.

Reliability test equipment falls loosely into two main categories: wafer-level equipment, and packaged-parts equipment. Within the wafer-level equipment category, there are turn-key systems that come ready to use with minimal set up and programming; manual systems or probers for ad hoc work; and component systems. We should note that a prober is usually a key piece of equipment in most component systems. In addition to probers, probes and probe cards are key technologies for wafer-level reliability testing. Probes make contact between the wafer and the probe card. Within the packaged-parts equipment category, there are burn-in and life test systems; and highly accelerated stress test systems that incorporate high humidity and high pressure.

Why does the industry perform wafer-level reliability testing? It saves cost, and more importantly, time! Package-level testing introduces a delay because of the assembly process. In many instances, the assembly house is quite distant from the wafer fab or engineering center, resulting in a delay. Package-level testing is time-consuming and costly. The equipment and space required for these activities can be expensive. Furthermore, there are limited

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acceleration opportunities with packaged-parts testing. The upper temperature for package-level testing is between 125 and 175°C, whereas wafer-level testing can be as high as 400°C. Wafer-level reliability testing can even be accomplished prior to the completion of the wafer lot. For instance, one can examine transistor reliability issues such as Negative Bias Temperature Instability (NBTI) once the metal-1 layer is deposited, if the test structure supports this configuration. This provides faster feedback to the process engineers. One can also use higher frequencies if one uses self-stressing test structures.



Figure 1. Illustrations of automated systems for performing wafer-level reliability.

There are several turn-key systems on the market for wafer-level reliability (See Figure 1). Agilent Technologies has the most comprehensive line of equipment available. The 4070 and 4080 series systems are some of the most well-engineered systems for semiconductor characterization on the market. Keithley is another player in this field. Keithley markets a system known as Automated Characterization Suite, or ACS. Although it does not have the precision of the Agilent system, it is more affordable. It is flexible and able to handle wafers and packaged parts. Aetrium sells a wafer-level characterization system called the 1164. It is the least precise, but is the most affordable. It is also quite flexible, capable of handling wafer-level and packaged-parts characterization. In general, these systems are designed to dock to an automated wafer prober for production measurements. They can also be docked to a manual probe system for ad-hoc or engineering measurements.



Figure 2. Illustration of Agilent 4070/4080 series.

As shown in Figure 2, the Agilent 4070 and 4080 series systems are some of the most precise and sensitive systems made for semiconductor characterization. They are capable of both DC and RF measurements. Their 2MHz frequency measurement capabilities allow them to accurately perform ultrathin dielectric C-V characterization. Their 10 nsec pulse generator allows accurate characterization of fast phenomena like NBTI and hi-k dielectric charge trapping. The systems also have optional electronics to evaluate flash memory cell and ring oscillator circuits. The 4080 series is architected to permit parallel testing to increase throughput. The 20 GHz 8 by 10 RF switch matrix allows characterization of a variety of RF devices.



Figure 3. Illustration of 4083A test head direct docking scheme .

Agilent's source measurement units, switches, tri-axial cabling, and test head direct docking scheme (see Figure 3) are the key to the low noise and accurate readings. The 4070 contains 8 source measurement units, 2 high resolution units, and 2 high power units. Agilent has gone to great pains to shield the units, and design low noise circuitry. These units allow measurements of currents as low as 1 femtoamp, and voltages as low as 2 microvolts. This precision comes with a price, however. A fully configured 4070 or 4080 series system can cost in excess of \$1M.

Another approach to reliability testing is to put together a system from individual components. With Agilent equipment, one can purchase a 4156 Semiconductor Parameter Analyzer, a low leakage switching mainframe, and the appropriate cabling. Agilent also sells a software package that can be used to measure and store the voltage and current values. To allow the components to talk with one another, one must generate the appropriate scripts that control the switching mainframe and the parameter analyzer. Like the turn-key approach, this solution also assumes that a prober or probe station is available. It is a less costly solution than a comparable turn-key system. However, one must be willing to invest substantial time in labor to automate the process for testing multiple sites or wafers.



Figure 4. Agilent Semiconductor Parameter Analyzer.

Figure 4 is an illustration of the Agilent 4156 Semiconductor Parameter Analyzer. The 4156 is essentially the same electronic system that forms the core electronics in the 4070 and 4080 series instruments. It has very low noise levels—below 10 fA current sensitivity and 2  $\mu$ V voltage sensitivity. To achieve these levels, one must use appropriate tri-axial shielding and shield as close to the structure as possible. It can be controlled manually through the panel or keyboard interface, or automatically through the IEEE-488 port. The unit has 4 source measurement units. It is a common system and used extensively in the industry for ad-hoc and engineering measurements that don't require a lot of test site integration.



Figure 5. Illustration of Agilent switch matrix.

If one has a test structure with multiple sites, it may make sense to design a system that can measure each of the sites without moving the probes or changing cabling. This can be accomplished using the Agilent switch matrix, as shown in Figure 5. The critical feature of a switching matrix is to eliminate background noise. This particular switch matrix has noise levels comparable to the 4156, making it ideal for low noise measurements. It is rack-mountable and can be expanded to as many as 384 channels. Connections can be made using tri-axial cables or through SMA cables. Like the 4156, it can be controlled through the IEEE-488 port. Let's assume that we have test structures designed to be accessed with a  $2 \times 10$  probe card. We can design a system that can test all of the sites on the test structure with a 4156, a 24 channel 5250 switch matrix, a probe station, and the appropriate cabling and probe card.

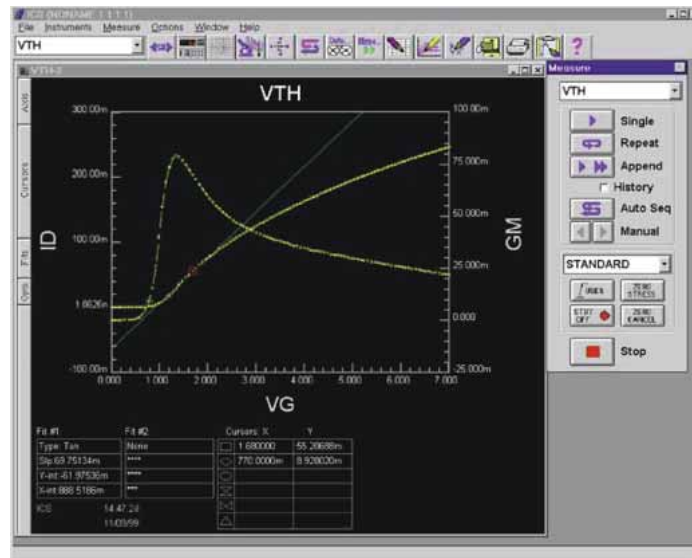


Figure 6. Agilent ICS software.

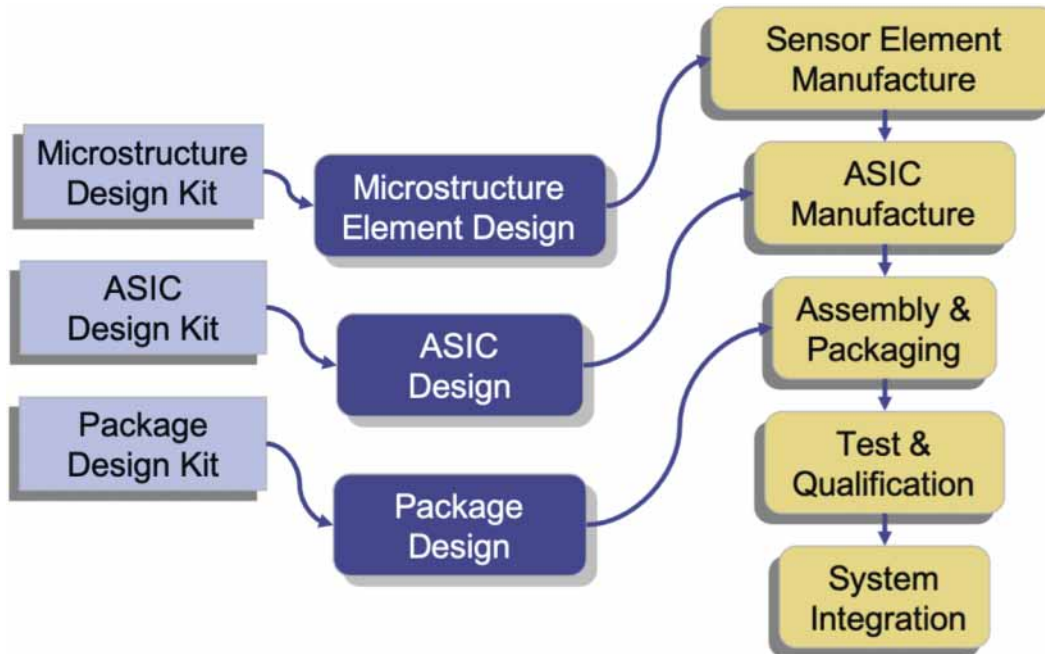
Agilent also sells a software package for basic transistor and current-voltage characterization called ICS. ICS stands for Interactive Characterization Software. We show this in Figure 6. This software can run on a PC with an IEEE-488 controller card. The software can control the 4156 and 5250 and make measurements of the test structure. The data can be stored and analyzed using its built-in software functions, or by exporting the data and analyzing it in a third-party software package.

Our discussion of Reliability Test Equipment will be continued in the June Newsletter.

## Technical Tidbit

### MEMS Development

In this month's technical tidbit, we will give a quick overview of the MEMS development process.



MEMS development is somewhat different than a traditional integrated circuit development process. The MEMS, or microstructure, development usually occurs with a different design kit and flow than the integrated circuit. Today, there are some tools that allow for MEMS structures to be included into a standard integrated circuit design flow. The package design is also typically done as a separate flow with a separate package design kit. When MEMS are included into the system, one must re-think the development flow. At the end, the sensor element must integrate in with integrated circuit elements. These must then be integrated in with the assembly and packaging. Finally, test, qualification, and system integration must be considered. MEMS devices may place special needs on the testing and qualification process. Even integration at the system level may require specialized assembly procedures.

Traditionally, MEMS development has been a research activity. The ideas, concepts, feasibility, design, modeling, prototyping, testing and evaluation were all done within laboratory environments by scientists and engineers. The manufacturing has been limited to small sample sizes to show proof-of-concept, and as such, it has been very costly, or even impossible to transform these proof-of-concepts into high-volume manufacturing.

What we are experiencing now is a wave of industrial MEMS development. Here we require established, documented, and qualified processes. The traditional flow of ideas, concepts, feasibility, design, modeling, prototyping, testing and evaluation now needs to include trial production runs,

qualification, and high-volume production ramps. In an industrial environment, we need the infrastructure for support from design and development through to manufacturing. With an established process, one has confidence, in not only the stability of the process, but also the ability to estimate production costs, which is critical for sales of MEMS devices.



## Ask the Experts

**Q: What type of substrate works best for RF applications?**

**A:** In terms of signal integrity, using a substrate with a low dielectric constant is best, so materials like Benzocyclobutene (BCB) or Bismaleimide Triazine (BT) work well. Another option is to use a chip-package co-design process to optimize the signal integrity, much like RF engineers do for Monolithic Microwave Integrated Circuits (MMICs). Of course, layout plays a critical role, so one may need to perform extensive simulation to confirm the materials and traces will perform properly.

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## Spotlight: IC Packaging Technology

### OVERVIEW

Overview: Integrated Circuit packaging has always been integral to IC performance and functionality. An IC package serves many purposes: (1) pitch conversion between the fine features of the IC die and the system level interconnection, (2) chemical, environmental and mechanical protection, (3) heat transfer, (4) power, ground and signal distribution between the die and system, (5) handling robustness, and (6) die identification among many others. Numerous critical technologies have been developed to serve these functions, technologies that continue to advance with each new requirement for cost reduction, space savings, higher speed electrical performance, finer pitch, die surface fragility, new reliability requirements, and new applications. Packaging engineers must fully understand these technologies to design and fabricate future high-performance packages with high yields at exceptional low-costs to give their company a critical competitive advantage.

This two-day class will detail the vital technologies required to construct IC packages in a reliable, cost effective, and quick time to market fashion. When completed, the participant will understand the wide array of technologies available, how technologies interact, what choices must be made for a high-performance product vs. a consumer device, and how such choices impact the manufacturability, functionality, and reliability of the finished product. An emphasis will be given to manufacturing, processes and materials selection tailoring and development. Each fundamental package family will be discussed, including flip chip area array technologies, Wafer Level Packaging (WLP), Fan-Out Wafer Level Packaging (FO-WLP), and the latest Through Silicon Via (TSV) developments. Additionally, future directions for each package technology will be highlighted, along with challenges that must be surmounted to succeed.

### WHAT WILL I LEARN BY TAKING THIS CLASS?

1. **Molded Package Technologies.** Participants learn the fundamentals of molding critical to leaded, leadless, and area array packaging, enabling them to eliminate problems such as flash, incomplete fill, and wire sweep.
2. **Flip Chip Technologies.** Participants learn the fundamentals of plating, bumping, reflow, underfill, and substrate technologies that are required for both high performance and portable products.
3. **Wafer Level Packages.** Participants learn the newest technologies that enable the increasingly popular Wafer Chip Scale Level Packages (WCSPs) and Fan-Out Wafer Level Packages (FO-WLPs).
4. **Through Silicon Via Packages and Future Directions.** Participants will know the latest advances in the recently productized TSV technology, as well as future directions that will lead to the products of tomorrow.

### COURSE OBJECTIVES

1. The course will supply participants with an in-depth understanding of package technologies current and future.
2. Potential defects associated with each package technology will be highlighted to enable the student to identify and eliminate such issues in product from both internal assembly and OSAT houses.

3. Cu and solder plating technologies will be described with special emphasis on package applications in TSVs and Cu pillars for FO-WLPs. Emphasis will be placed on eliminating issues such as reliability, non-uniformity, void free thermal aging performance, and contamination free interfaces.
4. New package processes employed in Through Silicon Via production will be described, along with current cost reduction thrusts, to enable the student to understand the advantages and limits of the technologies.
5. Temporary bonding and wafer thinning processes will be highlighted, as well as the cost reduction approaches currently being pursued to enable wider adoption of TSV packages.
6. The trade-offs between silicon, glass, and organic interposers will be highlighted, along with the processes used for each.
7. Participants will gain an understanding of the surface mount technologies that enable today's fine pitch products.
8. The class will provide detailed references for participants to study and further deepen their understanding.

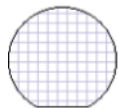
## COURSE OUTLINE

1. The Package Development Process as a Package Technology:
  - a. Materials and Process Co-Design
2. Molded Package Technologies:
  - a. Die Attach
    - i. Plasma Cleans
  - b. Wire Bonding
    - i. Au vs. Cu vs. Ag
    - ii. Die Design for Wire Bonding
  - c. Lead Frames
  - d. Transfer and Liquid Molding
    - i. Flash
    - ii. Incomplete Fill
    - iii. Wire Sweep
    - iv. Green Materials
  - e. Pre- vs. Post-Mold Plating
  - f. Trim Form
  - g. Saw Singulation
  - h. High Temperature and High Voltage Materials
3. Flip Chip and Ball Grid Array Technologies:
  - a. Wafer Bumping Processing
    - i. Cu and Solder Plating
    - ii. Cu Pillar Processing
  - b. Die Design for Wafer Bumping
  - c. Flip Chip Joining
  - d. Underfills
  - e. Substrate Technologies
    - i. Surface Finish Trade-Offs
    - ii. Core, Build-up, and Coreless

- f. Thermal Interface Materials (TIMs) and Lids
  - g. Fine Pitch Warpage Reduction
  - h. Stacked Die and Stacked Packages
  - i. Material Selection for Board Level Temperature Cycling and Drop Reliability
- 4. Wafer Chip Scale Packages:
    - a. Redistribution Layer Processing
    - b. Packing and Handling
    - c. Underfill vs. No-Underfill
  - 5. Fan-Out Wafer Level Packages:
    - a. Chip First vs. Chip Last Technologies
    - b. Redistribution Layer Processing
    - c. Through Mold Vias
  - 6. Through Silicon Via Technologies:
    - a. Current Examples
    - b. Fundamental TSV Process Steps
      - i. TSV Etching
      - ii. Cu Deep Via Plating
      - iii. Temporary Carrier Attach
      - iv. Wafer Thinning
    - c. Die Stacking and Reflow
    - d. Underfills
    - e. Interposer Technologies: Silicon, Glass, Organic
  - 7. Surface Mount Technologies:
    - a. PCB Types
    - b. Solder Pastes
    - c. Solder Stencils
    - d. Solder Reflow

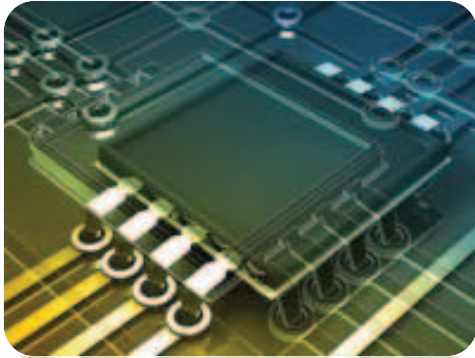
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6501 Wyoming NE, Suite C215  
Albuquerque, NM 87109-3971  
Tel. (505) 858-0454  
Fax (866) 205-0713  
e-mail: [info@semitracks.com](mailto:info@semitracks.com)



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(Click on each item for details)

### Introduction to Product Qualification

May 27 and 28, 2020 (Wed, Thu)  
8:00 A.M. – 12:00 noon PDT

## Upcoming Courses

(Click on each item for details)

Due to the CoronaVirus, the dates for these courses are in the process of being rescheduled. For questions about courses, please contact us at [info@semitracks.com](mailto:info@semitracks.com)

### Wafer Fab Processing

Date To Be Determined  
Munich, Germany

### Semiconductor Reliability / Product Qualification

Date To Be Determined  
Munich, Germany

### Failure and Yield Analysis

Date To Be Determined  
Munich, Germany

### IC Packaging Technology

Date To Be Determined  
Munich, Germany

### Advanced CMOS/FinFET Fabrication

Date To Be Determined  
Munich, Germany