

InfoTracks

Semitracks Monthly Newsletter



Chemical Vapor Deposition Basics Part 2

By Christopher Henderson

This month we will conclude our two-part series that provide an overview of chemical vapor deposition and the basic principles behind the technique. Process engineers usually refer to chemical vapor deposition by its short name CVD so we will refer to it that way as well.

One method for achieving higher reaction rates is to increase the gas phase mass transfer coefficient. This can be accomplished by inducing a laminar flow across the wafer. The figure here depicts the velocity of the gas across the wafer surface. A boundary layer exists near the surface of the wafer. This means that the velocity of the gas at the wafer surface will be zero. This effectively limits the film growth rate at higher gas flow rates (see Figure 1 on the next page).

Gas transport to the wafer is a key aspect of chemical vapor deposition. The mean free path of the gas molecules is a key component of the gas transport process. The lower the pressure is, the greater the mean free path. However, lower pressure also means fewer reactant molecules. Manufacturers of CVD systems design their systems such that gas flow is optimized over the wafer surfaces. The placement of gas inlets, wafers, and exhaust, the use of various reactants, the use of single wafer processing versus batch processing, and the use of thermal or plasma-enhanced chemical vapor deposition all affect the chamber design. There are two types of systems available for chemical vapor deposition: batch systems and single wafer systems. In a batch system, the wafers are loaded as a group into a furnace tube. The reactant gas is introduced at one end of the tube, and the exhaust gases are

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Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

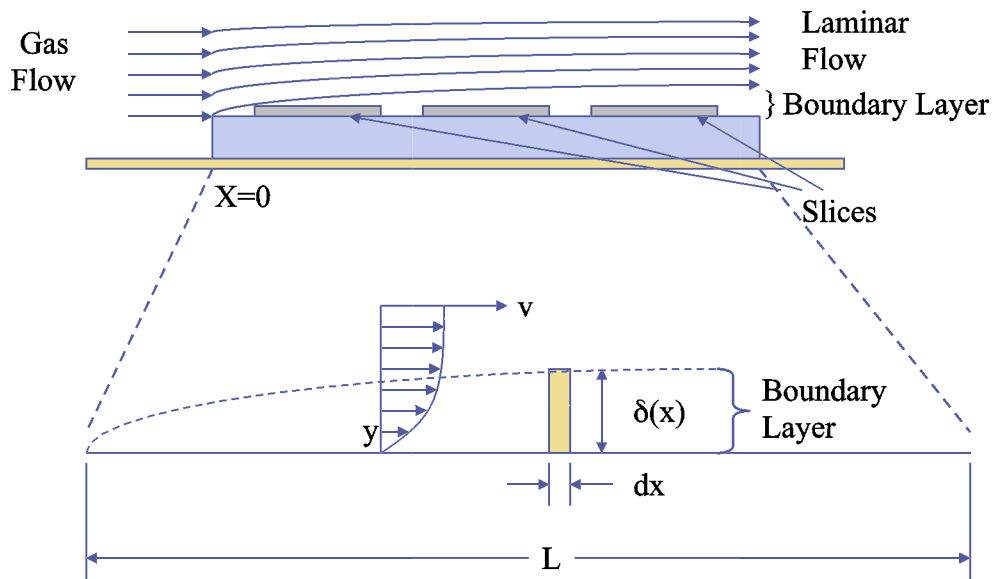


Figure 1. Boundary Layer in a Gas over a Flat Plate.

purged at the other end of the tube. In a single wafer system, the gas is introduced through a showerhead over the wafer, and the exhaust gases are purged at the side of the wafer.

CVD processes can be sub-divided into three types: atmospheric pressure CVD (or APCVD), low pressure CVD (or LPCVD), and plasma enhanced CVD (or PECVD). Both LPCVD and PECVD operate in a sub-atmospheric pressure regime, while APCVD operates at atmospheric pressure, as one would expect given the name. APCVD and LPCVD use thermal energy to drive the reaction, while PECVD uses plasma energy along with thermal energy to help lower the overall reaction temperature. These tables show the applications for the three types of CVD processes.

Acronym	Name	Pressure Regime	Energy	Reference
APCVD	Atmospheric Pressure CVD	Atmospheric	Thermal	APCVD module
LPCVD	Low Pressure CVD	Sub-atmospheric	Thermal	LP CVD module
PECVD	Plasma Enhanced CVD	Sub-atmospheric	Plasma + Thermal	PE CVD module
Films Commonly Deposited by CVD				
Film		APCVD	LPCVD	PECVD
Silicon Nitride		X	X	X
Polysilicon (doped or undoped)			X	
Silicon oxide (doped or undoped)		X	X	X
Epitaxial silicon		X	X	
Tungsten				X
Refractory metal siliicides and nitrides				X
Titanium nitride		X		X
Low-k IMDs				X
High-K gate/capacitor dielectrics			X	X

Table 1. Pressure regimes and applications of CVD.

There are four variants of chemical vapor deposition used in the semiconductor industry. Pure thermal chemical vapor deposition uses elevated temperatures to drive the reaction at the surface. Plasma Enhanced or PE-CVD is often used for faster reaction rates. Not only is energy for the reaction supplied by heat, but it is also supplied through RF energy. High Density Plasma or HDP-CVD is a recent development that is a variant of PE-CVD processing. In these processes, plasmas are struck at very low pressures in electron cyclotron resonance or inductively coupled plasma chambers. The gases, usually argon and oxygen, are then drawn by an electric field towards the wafer surface, where the oxygen reacts with silane. As a result, gap fill is improved, excellent high quality SiO₂ films are produced, and there is a net reduction in overall thermal budget. Rapid thermal processing is increasingly used as well to reduce the overall thermal budget during processing. Rapid thermal processing CVD works similarly to rapid thermal oxidation. The temperature ramps up quickly when the heat lamps are turned on, and ramps down quickly when the heat lamps are turned off.

In an atmospheric pressure CVD reaction, the reaction rate is mass transfer limited. In this situation the flow of the gas must be uniform. This means that wafers cannot be placed too close to each other; otherwise they will interrupt the flow of the reaction gas. Historically, process engineers used APCVD to grow thicker dielectrics like Borosilicate glasses and silicon nitride layers. With the advent of more advanced technologies with their thinner layers and lower processing temperatures, the use of APCVD has diminished. Engineers do still use the technique for some specialized operations, like epitaxial silicon growth and growth of silicon carbide films on silicon or silicon nitride substrates.

In a low pressure CVD reaction, the surface reaction is reaction rate limited. In order to grow the appropriate thickness, the temperature and time must be closely controlled. The reactions are heterogeneous in order to minimize particulate generation. LPCVD operates in a surface reaction rate limited regime, and since this eliminates limitations associated with mass transport, the equipment can process larger batches of wafers. This is an important consideration in a high-volume factory. The pressure in these systems ranges from around 0.25 to 1 Torr and operates at temperatures between 550 and 800°C. Given the high temperatures, this technique cannot be used after aluminum deposition on the chip. There are two types of process tools that employ LPCVD: hot-wall and cold-wall. Historically, engineers used hot wall reactors to process large groups of wafers simultaneously. Newer systems that cluster operations together are single wafer systems using cold-wall reactor technology.

Plasma Enhanced or PE-CVD is often used for faster reaction rates. Not only is energy for the reaction supplied by heat, but it is also supplied through RF energy. This technique operates in a temperature regime that makes the surface reaction rate the limiting factor. High Density Plasma or HDP-CVD is a recent development that is a variant of PE-CVD processing. In these processes, plasmas are struck at very low pressures in electron cyclotron resonance or inductively coupled plasma chambers. The gases, usually argon and oxygen, are then drawn by an electric field towards the wafer surface, where the oxygen reacts with silane. As a result, gap fill is improved, excellent high quality SiO₂ films are produced, and there is a net reduction in overall thermal budget.

This table summarizes the three types of CVD processes. All three CVD processes are heterogeneous reactions, but beyond that, each type has its own advantages and disadvantages. We cover these advan-

tages and disadvantages in more detail in our Online Training Systems, with sections on the specific CVD techniques.

Parameter	APCVD	LPCVD	PECVD
Reaction Type	Heterogeneous	Heterogeneous	Heterogeneous
Limiting Factor	Mass Transport Rate	Surface Reaction Rate	Surface Reaction Rate
Energy	Thermal	Thermal	RF Reaction Rate
Temp. Range	550 – 800°C	550 – 800°C	200 – 450°C
Post-Al Compatible?	No	No	Yes
Pressure Range	100 – 760 Torr	0.25 – 1.0 Torr	0.25 – 1.0 Torr
Chamber Walls	Hot or Cold	Hot or Cold	Cold
Step Coverage	Conformal	Conformal	Non-conformal to near-conformal
Range of Materials	Limited	Limited	Large
Film Purity	Lower (also stoichiometry issues)	Excellent	Lower (e.g. H ₂ Incorporation)
Deposition Rate	Higher	Lower	Higher

Table 2. Characteristics associated with the types of CVD reactions.

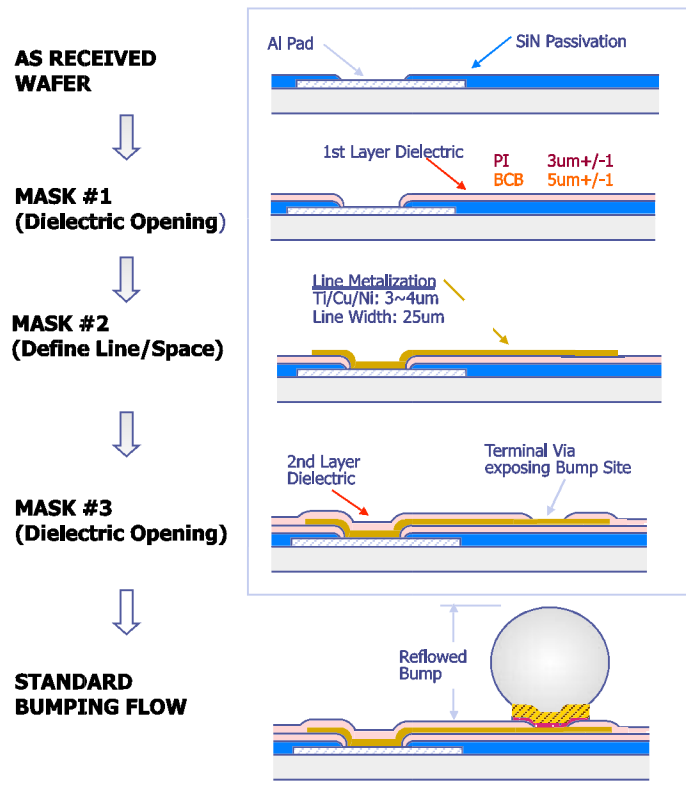
Let's summarize what we have learned. In a generic CVD process, the reactant gases are introduced into the reaction chamber. These gases diffuse through the boundary layer to the wafer surface. Once the gases reach the surface, we refer to them as reactants or adatoms, and they adsorb on the wafer surface. These adatoms migrate to the growth sites where they react with the surface to form the film. This reaction produces a solid film and gaseous by-products, and these reactions might be pyrolysis, reduction, or oxidation reactions. The gaseous by-products desorb from the surface, diffuse through the boundary layer back into the gas flow region where they are exhausted.

Technical Tidbit

Wafer Redistribution Process Flow

Redistribution and bump is a common process for chip-scale packages. The idea is to even out the distance between connections by adding an extra level of interconnect on top of the wafer to “redistribute” the connections such that they line up for various package formats like Ball Grid Array packages, Quad Flat No-Lead Packages, and so on.

STANDARD RDL PROCESS FLOW



The main advantage to this technology is that one silicon design can be used for multiple applications, or be placed in multiple packages. The disadvantages include the fact that: multiple mask layers for the redistribution interconnect require higher tool cost, multiple layer operations can increase process and materials cost by two to three times, and the increased process steps and operations lowers the final yield. Nonetheless, this is a popular option for certain types of parts, where a new layout might be more costly than the costs of the redistribution layer materials and processing.



Ask the Experts

Q: Why is there the option to perform Latchup Testing at both room and hot temperature? When should I test for latchup at hot temperatures?

A: JESD78 defines two classes of Latchup testing: Class I and Class II. Class I testing is at 25°C, whereas Class II testing is at the maximum operating temperature of the component. For most components, latchup susceptibility increases with temperature, so it makes sense to test at high temperatures, especially if the end application includes scenarios where one might operate at high temperatures, like in an automobile for example. Many companies will perform latchup testing at both 25°C and maximum operating temperatures just to be on the safe side.

Spotlight: Changes to Come

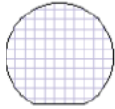
In the next month we will be upgrading our Online Training System Platform. Part of the reason to upgrade is to take advantage of some newer database technology features available in PostgreSQL and improve the implementation of some administrator functions, but another reason is to improve the user experience. The new system will allow us to incorporate more types of content. For example, we will now be able to directly post videos without the need to put them into a Flash player. This will allow users to see the videos on devices that do not have a built-in Flash player. It will also provide better support for embedding questions or short quizzes into presentations. The new system will also allow us to upload more interactive presentations in non-Flash format, so that they can be viewed on devices like the iPad for instance. For those of you who currently access the system, you will see some new features.

- You will no longer need to enter the characters from the image "Captcha" at the login screen. We have implemented a more robust security system that invalidates the need for this second level of identification.
- In the new system, Workspaces will now be called Classrooms, and Courses will be called Classes. This will provide consistency between our public-facing system and the custom-built systems we operate.

For those of you who currently have accounts, you will receive an email message with some more details about the rollout and change over.

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).



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AMFA2013
Advanced Materials Failure Analysis Workshop

Sunday, August 4

Indiana Convention Center
100 South Capitol
Indianapolis, IN 46225

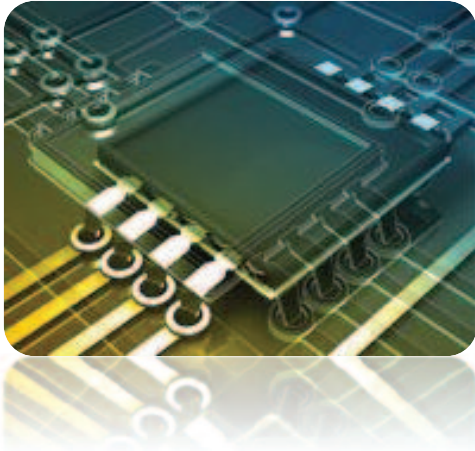
Chris Henderson of Semitracks will chair the

2013 Advanced Materials Failure Analysis Workshop

Sunday, August 4, 2013

Indiana Convention Center • Indianapolis, Indiana

<http://www.amfaworkshop.org>



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our web site!

<http://www.semitracks.com>

*To post, read, or answer a question, visit our [forums](#).
We look forward to hearing from you!*

Upcoming Courses

(Click on each item for details)

Copper Wire Bonding Technology and Challenges

May 13 – 14, 2013 (Mon – Tue)
Munich, Germany

Failure and Yield Analysis

May 13 – 16, 2013 (Mon – Thur)
Munich, Germany

MEMS Technology

May 15 – 16, 2013 (Wed – Thurs)
Munich, Germany

IC Packaging Design and Modeling

May 27 – 29, 2013 (Mon – Wed)
Penang, Malaysia

Failure and Yield Analysis

June 3 – 6, 2013 (Mon – Thur)
San Jose, California

Semiconductor Reliability

June 26 – 28, 2013 (Wed – Fri)
Penang, Malaysia

Failure and Yield Analysis

July 1 – 4, 2013 (Mon – Thur)
Penang, Malaysia

Advanced Thermal Management and Packaging Materials

September 2013 (Dates TBD)
Philadelphia, Pennsylvania