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INFOTRACKS

YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Semiconductor Cleanroom Technology

By Christopher Henderson

In last month's Feature Article, we continued our series on Cleanroom Technology by discussing Equipment Placement in a Cleanroom. In this month's Feature Article, we will continue our discussion on Cleanroom Technology with a focus on Power Usage in the Fab. Power is an integral part of the cleanroom design and construction, and plays a critical role in the successful processing of wafers. The main goal is to reduce power consumption in the fab.

There are a number of factors that affect and influence the power requirements and considerations in a wafer fabrication facility. These factors are listed here, and form the outline for this section. The first is the air change rates inside the fab. Next is the recirculation airflow, followed by the chilled water loops. Each of these systems requires powerful motors to enable the circulation of the air and water. We will cover the following factors in future Feature Articles: 1) The exhaust system for the fab. The exhaust system also uses power fans and must be optimized to reduce power consumption. 2) Low pressure air drop systems. The pressure inside the fab is slightly higher than the pressure outside of the fab, so fabs require pressure drop systems to control this difference. 3) The power associated with mini-environments. Some systems or areas within the fab may employ special environmental control. 4) The Heating Ventilation and Air Conditioning

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Semiconductor Reliability and Product Qualification

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systems, or HVAC systems. These systems control the temperature and humidity in the wafer fab. 5) Vacuum pump optimization. Vacuum pumps consume a large proportion of the power in a modern fabrication facility. 6) Water-side free cooling. Many systems inside the fab produce large amounts of heat, and as such, must be cooled. Water cooling is an efficient method for removing heat from many systems, but requires pumps and other equipment to circulate the water. 7) Deionized water generation and usage reduction. Deionized water is typically generated onsite, and the generation process uses a significant amount of power. Therefore, one must pay close attention to the power consumed in the generation process and look for ways to reduce the usage of deionized water generation.

When designing the wafer fabrication facility, power must be distributed appropriately to various locations in the fab. Some areas may require different voltages and current capacities, based on the type of equipment, the layout of the equipment in the fab, the distribution of air handlers, vacuum pumps, recirculation pumps, and so forth. Figure 1 shows a cross-section view of a wafer fab. The power requirements will vary in each section of the fab, with certain requirements for the air re-circulation fans, the work zones, the utility zones, the support tools in the sub-fab, the crawl space, the computer center and smock rooms, the maintenance shops, and the storage rooms.

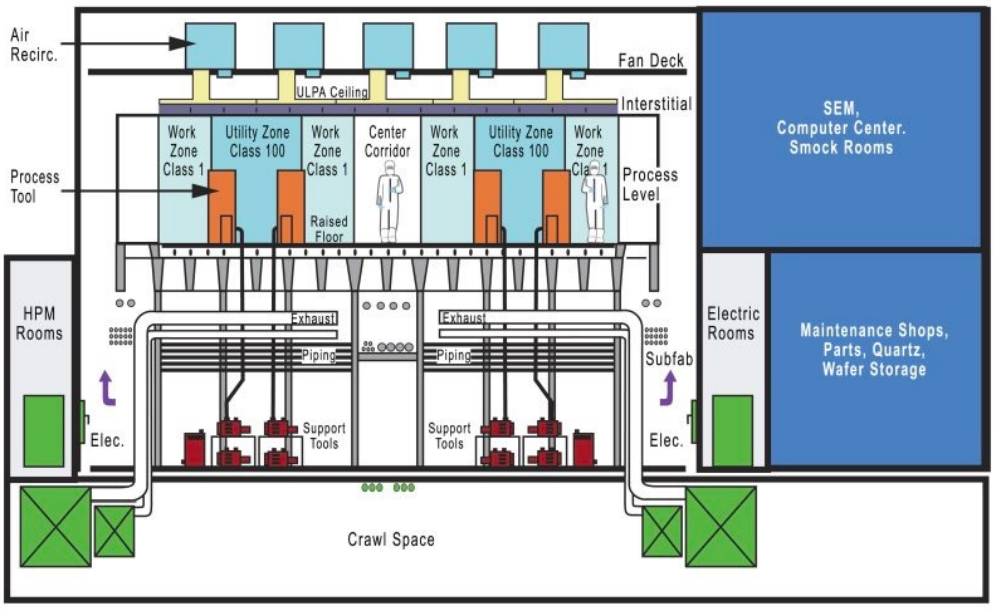

Figure 1- Cross-section view of a wafer fab (drawing courtesy MKS Instruments).

The first item we will discuss in more detail that affects and influences the power requirements and considerations is the air change rates in a fab. Recirculation Air Change Rates, or ACRs, to which they are referred by some in the industry, are an important factor in contamination control of a cleanroom, and are the single largest factor in determining fan and motor sizing for a recirculation air handling system. Air handler sizing and air path design both directly impact the capital costs and configuration of a building. Lower air change rates will allow the use of smaller fans. The fan power is proportional to the airflow cubed, so the recommended design

ranges for ISO 5 (Class 100) cleanroom ACRs are from 250 to 700 Air Changes per Hour, or ACH. Higher ACRs equate to higher airflows and more energy use and do not always achieve the desired cleanliness. Both new and existing systems can benefit from optimized air change rates. This often corresponds to lower air change rates. Furthermore, lower airflow can also minimize turbulence. This process has become quite complex, so engineers often use computational fluid dynamics to model and optimize the system.

Next, let's discuss recirculation airflow in more detail. Recirculation airflow can be controlled in various ways. The goal is to reduce recirculated airflow in the cleanroom when it is unlikely particles would be generated. Engineers typically optimize the airflow for the best contamination control by real-time particle monitoring with feedback to the recirculation system. This can be controlled in one of three ways. First, engineers use timers or scheduling software to lower airflow at certain times when the cleanroom is unoccupied and with minimal process activity. This generally would be a step change reduction in airflow when the room is expected to be unoccupied and increased back to higher airflow before the room is reoccupied. Second engineers can use occupancy sensors to determine when to lower airflow whenever people are not present in the cleanroom. Placement and time delay of sensors needs to be such as to sense when people have exited or are about to enter the space. Third, engineers can use particle counters to control airflow in the room based upon real-time cleanliness monitoring. In this scheme, particle counters would be deployed to monitor the various sizes of particles of concern for a given cleanroom's contamination control problem. The number and placement of counters would need to be determined through interaction with process engineers and may involve some experimentation. An output signal from the particle counters can directly control recirculation fan speed. Figure 2 shows a graph of the reduction in fan power for a cleanroom where a timer was used to set back airflow when the cleanroom was unoccupied at night and on weekends. The air change rate was reduced from 594 ACH to 371 ACH to achieve this reduction. This results in a reduction in fan power of approximately 75%, from approximately 8 kilowatts to just below 2 kilowatts, as shown in this graph from a pilot study done at Lawrence Berkeley National Lab (LBNL).

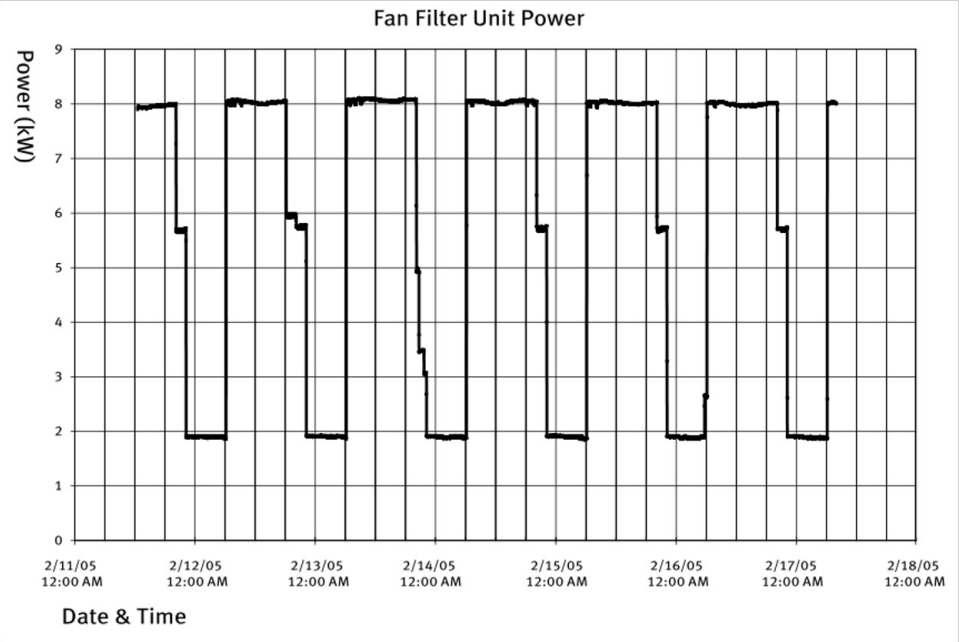

Figure 2- Graph showing reduction in fan power for a cleanroom with timer set-backs (courtesy LBNL).

Several methods of control have been shown to maintain cleanliness levels while minimizing airflow; one of which is demand-controlled filtration. The concept ranges from simple use of timers to sophisticated particle monitoring and control. During this pilot study at LBNL, reduction in airflow did not necessarily increase particle counts, as shown in Figure 3.

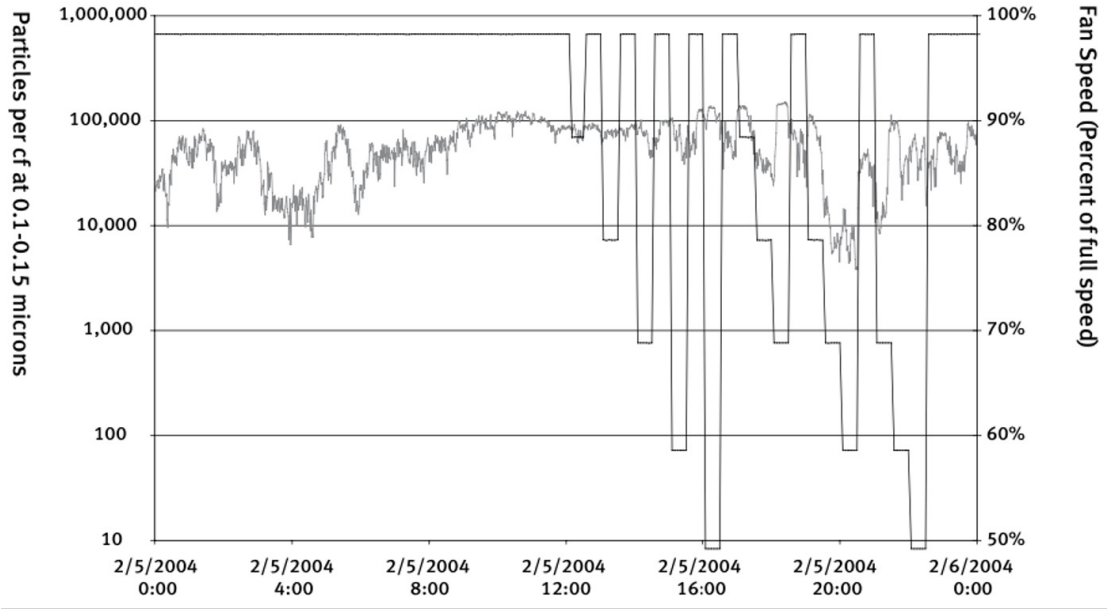

Figure 3- Graph showing reduction in fan power for a cleanroom with timer set-backs (courtesy LBNL).

Now, let's discuss chilled water loops. Chilled water loops can account for as much as 10 to 20 percent of the power usage in a cleanroom. Standard chilled water loops in a cleanroom operate at a temperature between 3 and 4°C. It is necessary for de-humidification in the fab, but it also creates an efficiency penalty on the chillers. We will explain efficiency in the next paragraph. One can improve the efficiency by providing chilled water at a higher temperature. There can be between a 20 and 40% savings if the temperature of the water is 11°C higher, but this may not necessarily be an option in many fabs. Chilled water is created using a chiller. A chiller is a machine that removes heat from a liquid via a vapor-compression or absorption refrigeration cycle. This liquid can then be circulated through a heat exchanger to cool air or equipment as required. As a necessary byproduct, this refrigeration cycle creates waste heat that must be exhausted to the outside environment (ambient) or, for greater efficiency, recovered for heating purposes. Chiller efficiency depends on the energy consumed and the cooling delivered. Absorption chillers are rated in fuel consumption per ton cooling. Electric motor driven chillers are rated in kilowatts of electricity per ton cooling.

In order to understand chiller efficiency, we must understand that the purpose of a chiller is to remove heat from any building's chiller water circuit and to reject it to the ambient by using either an air-cooled condenser (For Air Cooled Chillers) or a combination of water-cooled condenser/ cooling tower (For Water Cooled Chillers). In both cases, most of the power applied to the chillers is for the compressor which will pump the refrigerant between the evaporator and the condenser. The compressor takes up most of the power consumption for the chiller as it lifts the refrigerant from a low temperature/low pressure state in the evaporator to a high temperature/high pressure state in the condenser. In order to have a chiller which runs efficiently, the lift between refrigerant temperature in the evaporator and condenser must be minimized. This can be done by leaving chilled water at a relatively higher temperature (i.e. use of 7°C instead of 5°C. Leaving chilled water at a higher temperature will reduce the amount of lift required for the compressor and help improve the efficiency of the chiller). Therefore, operating a chilled water system at a higher temperature, like 15°C instead of 4°C is more efficient. We show the energy efficiency graph in Figure 4.

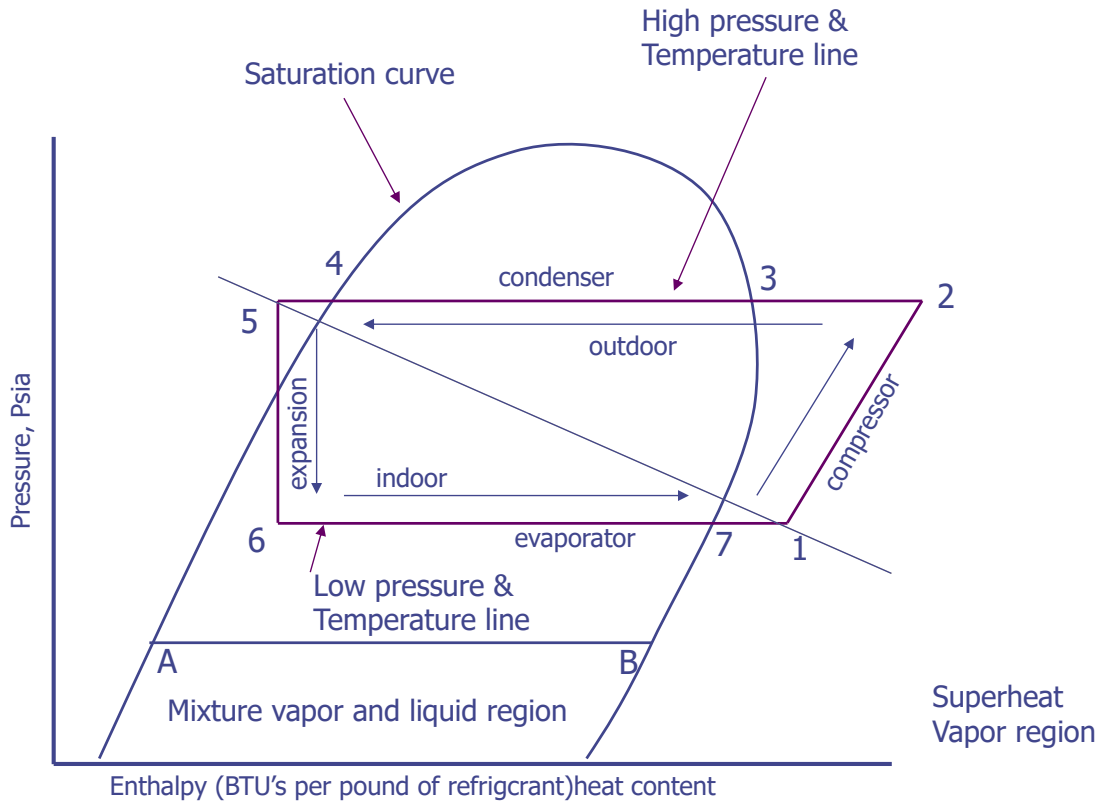

Figure 4- Energy efficiency graph showing pressure as a function of enthalpy, or BTUs per pound of refrigerant, for air conditioning units.

This concludes the first portion of our discussion on power for fabrication cleanrooms. We will continue this discussion in next month's Feature Article.

Technical Tidbit: ESD From Outside to Surface (ESDFOS)

This month's Technical Tidbit covers ESD From Outside to Surface (ESDFOS). Most engineers assume that ESD occurs in such a manner as to damage the circuitry directly connected to the input, output or power supply pins on a circuit. While this is true most of the time, it is not true all of the time. ESDFOS is a direct ESD-discharge into the surface of bare dies or wafers, or even packaged ICs, by breaking through the mold compound and the passivation layers.
Figure 1 (left) is an SEM image of the backside FIB cut showing a hole in an overlying polyimide layer with molding compound filling in the hole. Also note the detected metal filaments that are the cause of the Vdd to GND short, highlighted by the red circle. These failures occurred in the field. Figure 1 (right) is an SEM image of a frontside FIB cut showing a hole in a polyimide layer that penetrates to the upper metal layers in the IC. These failures were eventually traced down to ungrounded wafer mount stations in the assembly process. These events can be quite difficult to protect against through the chip design process. The charge bypasses ESD input protection circuits, so they are not effective against this particular type of ESD.

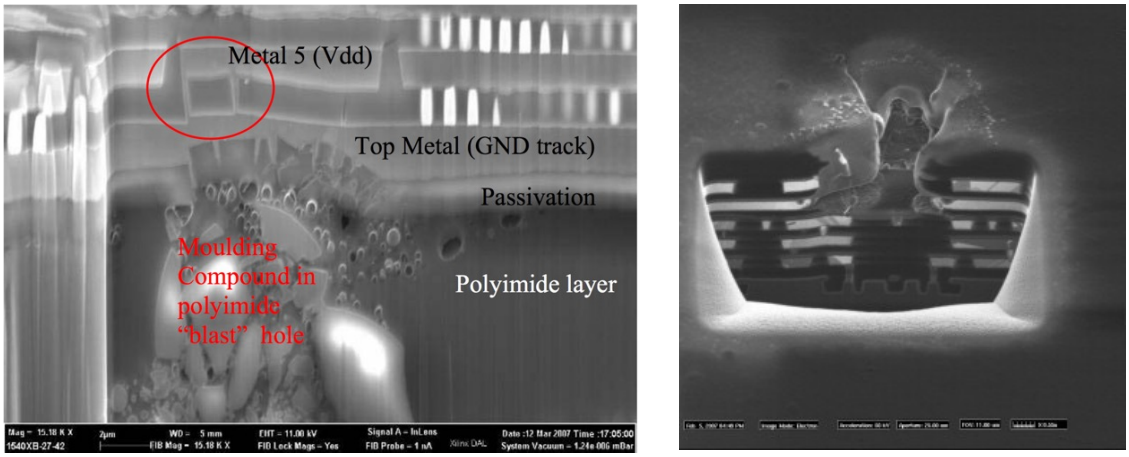

Figure 1 - (left) SEM image of a backside FIB cut showing damage from ESDFOS that occurred in the field; (right) SEM image of a frontside FIB cut showing damage from ESDFOS that occurred during assembly.

Ref. P. Jacob, Tool-Related ESD Surface Damage (ESDFOS) on Wafers in Cu-Technology, ISTFA, November 2007

Ask The Experts

Q: What happens with the copper surface during grinding and polishing steps in the course of TSV creation? Wouldn't the copper be severely damaged or smeared, leading to copper over the surface of the wafer?

A: Smearing of copper can occur, so the way to minimize this effect is to use a lighter pressure on the polishing pad, and to perform the polishing with a slower rotation speed on the polishing system.

Course Spotlight: IC PACKAGING TECHNOLOGY

OVERVIEW

Integrated Circuit packaging has always been integral to IC performance and functionality. An IC package serves many purposes: (1) pitch conversion between the fine features of the IC die and the system level interconnection, (2) chemical, environmental and mechanical protection, (3) heat transfer, (4) power, ground and signal distribution between the die and system, (5) handling robustness, and (6) die identification among many others. Numerous critical technologies have been developed to serve these functions, technologies that continue to advance with each new requirement for cost reduction, space savings, higher speed electrical performance, finer pitch, die surface fragility, new reliability requirements, and new applications. Packaging engineers must fully understand these technologies to design and fabricate future high-performance packages with high yields at exceptional low-costs to give their company a critical competitive advantage.

IC Packaging Technology is a two-day class that details the vital technologies required to construct IC packages in a reliable, cost effective, and quick time to market fashion. When completed, the participant will understand the wide array of technologies available, how technologies interact, what choices must be made for a high-performance product vs. a consumer device, and how such choices impact the manufacturability, functionality, and reliability of the finished product. An emphasis will be given to manufacturing, processes and materials selection tailoring and development. Each fundamental package family will be discussed, including flip chip area array technologies, Wafer Level Packaging (WLP), Fan-Out Wafer Level Packaging (FO-WLP), and the latest Through Silicon Via (TSV) developments. Additionally, future directions for each package technology will be highlighted, along with challenges that must be surmounted to succeed.

By focusing on current issues in packaging technology, participants will learn why advances in the industry are occurring along certain lines and not others. Our instructors work hard to explain semiconductor packaging without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor packaging. This skill-building series is divided into four segments:

1. Molded Package Technologies. Participants learn the fundamentals of molding critical to leaded, leadless, and area array packaging, enabling them to eliminate problems such as flash, incomplete fill, and wire sweep.

2. Flip Chip Technologies. Participants learn the fundamentals of plating, bumping, reflow, underfill, and substrate technologies that are required for both high performance and portable products.

3. Wafer Level Packages. Participants learn the newest technologies that enable the increasingly popular Wafer Chip Scale Level Packages (WCSPs) and Fan-Out Wafer Level Packages (FO-WLPs).

4. Through Silicon Via Packages and Future Directions. Participants will know the latest advances in the recently productized TSV technology, as well as future directions that will lead to the products of tomorrow.

Course Objectives

1. The course will supply participants with an in-depth understanding of package technologies current and future.
2. Potential defects associated with each package technology will be highlighted to enable the student to identify and eliminate such issues in product from both internal assembly and OSAT houses.
3. Cu and solder plating technologies will be described with special emphasis on package applications in TSVs and Cu pillars for FO-WLPs. Emphasis will be placed on eliminating issues such as reliability, non-uniformity, void free thermal aging performance, and contamination free interfaces.
4. New package processes employed in Through Silicon Via production will be described, along with current cost reduction thrusts, to enable the student to understand the advantages and limits of the technologies.
5. Temporary bonding and wafer thinning processes will be highlighted, as well as the cost reduction approaches currently being pursued to enable wider adoption of TSV packages.
6. The trade-offs between silicon, glass, and organic interposers will be highlighted, along with the processes used for each.
7. Participants will gain an understanding of the surface mount technologies that enable today's fine pitch products.
8. The class will provide detailed references for participants to study and further deepen their understanding.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor packaging and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is application. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field.

COURSE OUTLINE

Day 1

1. The Package Development Process as a Package Technology
    1. Materials and Process Co-Design
2. Molded Package Technologies
    1. Die Attach
        1. Plasma Cleans
    2. Wire Bonding
        1. Au vs. Cu vs. Ag
        2. Die Design for Wire Bonding
    3. Lead Frames
    4. Transfer and Liquid Molding
        1. Flash
        2. Incomplete Fill
        3. Wire Sweep
        4. Green Materials
    5 Pre- vs. Post-Mold Plating
    6. Trim Form
    7. Saw Singulation
    8. High Temperature and High Voltage Materials

Day 2

1. Flip Chip and Ball Grid Array Technologies
    1. Wafer Bumping Processing
        1. Cu and Solder Plating
        2. Cu Pillar Processing
    2. Die Design for Wafer Bumping
    3. Flip Chip Joining
    4. Underfills
    5. Substrate Technologies
        1. Surface Finish Trade-Offs
        2. Core, Build-up, and Coreless
    6. Thermal Interface Materials (TIMs) and Lids
    7. Fine Pitch Warpage Reduction
    8. Stacked Die and Stacked Packages
    9. Material Selection for Board Level Temperature Cycling and Drop Reliability
2. Wafer Chip Scale Packages
    1. Redistribution Layer Processing
    2. Packing and Handling
    3. Underfill vs. No-Underfill
3. Fan-Out Wafer Level Packages
    1. Chip First vs. Chip Last Technologies
    2. Redistribution Layer Processing
    3. Through Mold Vias
4. Through Silicon Via Technologies
    1. Current Examples
    2. Fundamental TSV Process Steps
        1. TSV Etching
        2. Cu Deep Via Plating
        3. Temporary Carrier Attach
        4. Wafer Thinning
    3. Die Stacking and Reflow
    4. Underfills
    5. Interposer Technologies: Silicon, Glass, Organic
5. Surface Mount Technologies
    1. PCB Types
    2. Solder Pastes
    3. Solder Stencils
    4. Solder Reflow

Upcoming Courses:

Failure and Yield Analysis - March 20-23, 2023 (Mon.-Thurs.) | Munich, Germany

Failure and Yield Analysis - May 1-4, 2023 (Mon.-Thurs.) | Oro Valley, Arizona

Semiconductor Reliability and Product Qualification - May 8-11, 2023 (Mon.-Thurs.) | Oro Valley, Arizona

Have an idea for a course? If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please email us at info@semitracks.com

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!