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Semitracks Monthly Newsletter

Reliability Test Equipment: Probes

By Christopher Henderson

In this document, we will cover probes used for reliability testing. The probe card and needles are an important component of the overall reliability test solution.

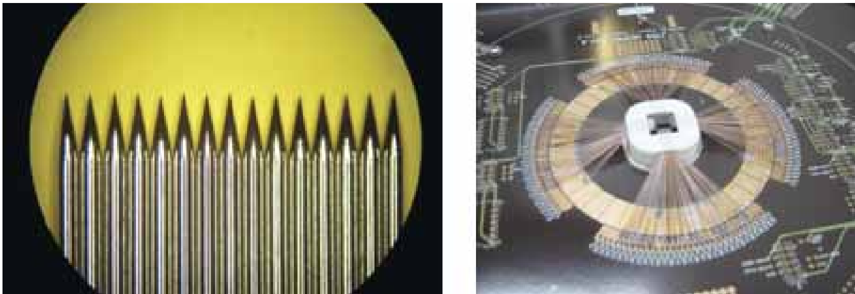

Figure 1. Images of probes (left) and probe cards (right).

A critical component in wafer-level reliability testing are the probe cards and probes themselves. Many inexperienced engineers will overlook the importance of choosing the right probe cards and probes for the application. There are a number of probe cards and probe manufacturers on the market. FormFactor is the leader in probe card technology. Another leader in the industry that specializes in reliability applications is Celadon Systems. As for individual probes, the probe station manufacturers provide a number of different probe tips and configurations.

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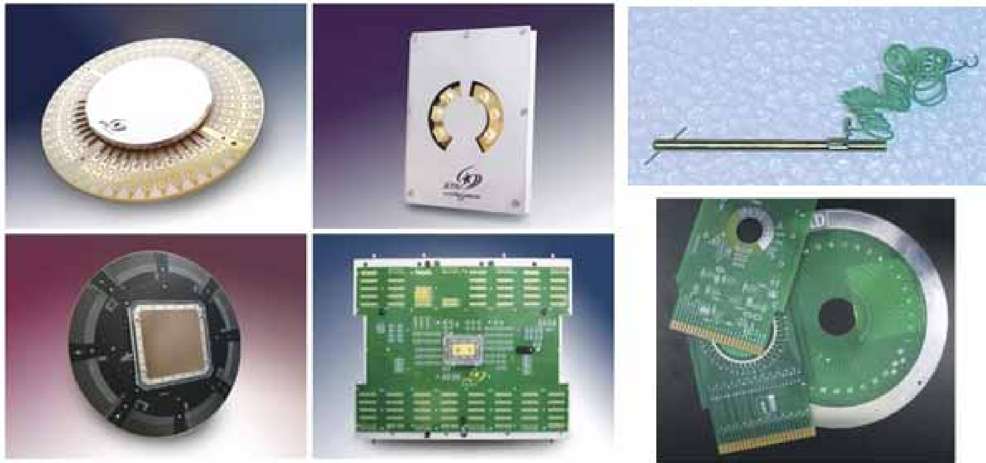


Figure 2. Probes and probe cards: issues.

The two biggest issues associated with probes and probe cards are damage to the probes and poor contact between the probes and the chip pads or interconnect. Poor contact can be the result of oxidation of the bond pad surface or the probe tips. Thermal expansion can cause the wafer to shift with respect to the probe tips. And insufficient overdrive can cause the probes to lose contact with the surface.

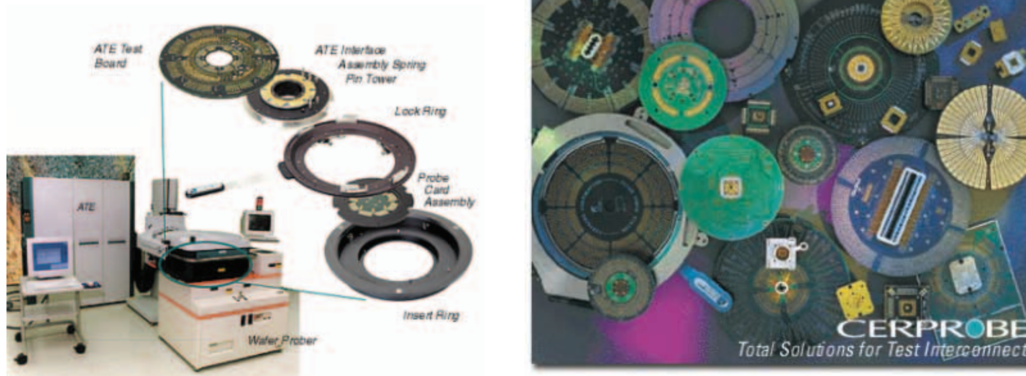


Figure 3. FormFactor technology.

The largest company supplying probe cards to the industry is FormFactor. Much of FormFactor's product line comes from the acquisition of the Cerprobe product line from Kulicke and Soffa. FormFactor supplies a variety of components that interface between the tester and the wafer or packaged part. This includes ATE test boards, interface assemblies, lock rings, and probe card assemblies. Since most probe cards are custom, FormFactor will take an engineering drawing and create the probe card from the drawing. Other suppliers like ESH and Celadon offer this service as well. FormFactor manufactures cards using epoxy ring, ceramic blade, buckling beam, and photolithographic technologies.

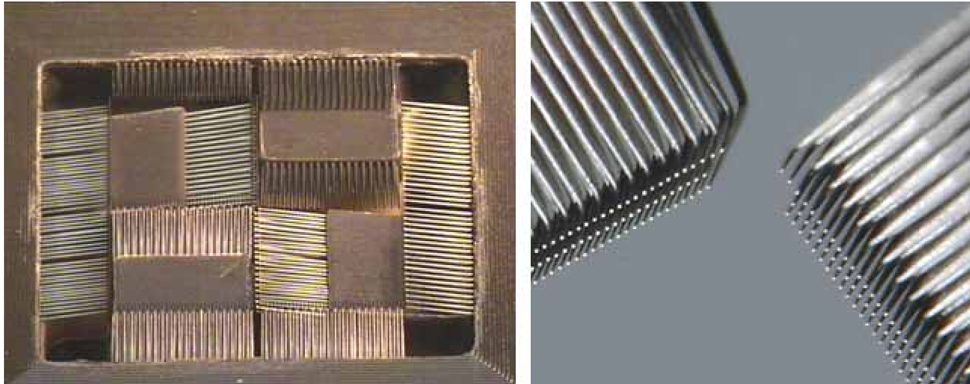


Figure 4. Example of cantilever probe card/probe needles .

The traditional method for probing is the cantilevered probe card. Figure 4 is an example of a cantilever probe card. The probe needles might come in at a shallow angle and touch the pad or they might have a bend, so that they touch down at a higher angle to the pad, like we show on the right. The high angle helps reduce the generation of particles on the wafer and reduce damage to the bond pads.

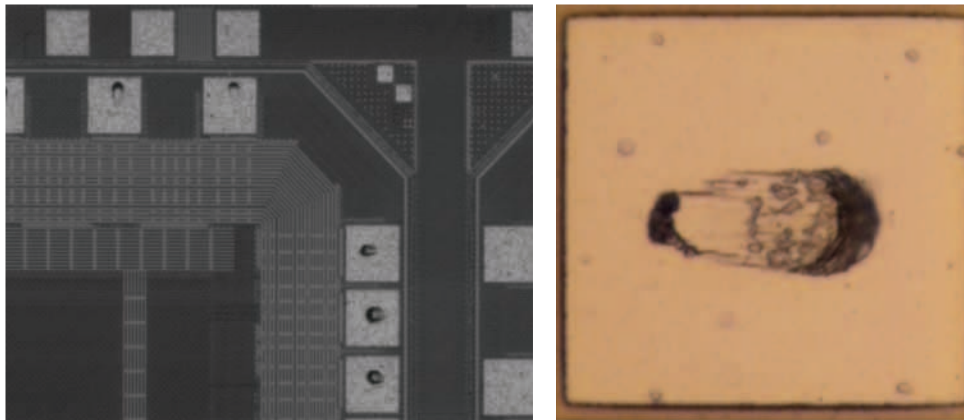


Figure 5. Typical cantilevered probe needle marks on aluminum bond pads: scrap mark (left) and probe mark (right).

Figure 5 is an example of the typical probe marks on bond pads left by cantilevered probes. The scrap mark, shown on the left, is typical of this type of cantilevered probe. The probe mark is also a great visual indicator that the device has been probed.

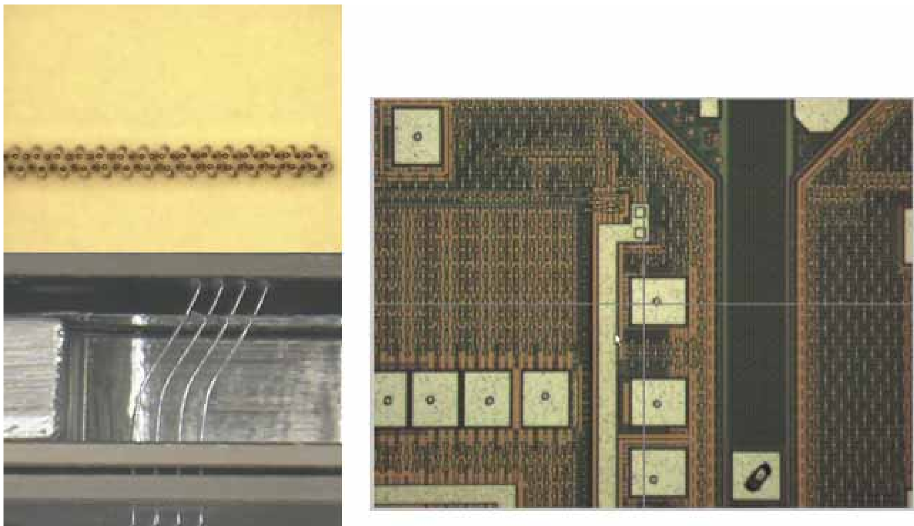


Figure 6. Vertical probe card: buckling beams (left); on aluminum bond pads (right).

The second type of probe card is the vertical probe. We generate the pressure on the pad to make positive contact by the bend in the probes, and this approach is sometimes known as buckling beams. We show examples of the probe marks on the pads in the image on the right in Figure 6. This type of probing will generate fewer particles, and can facilitate probing an array of pads.

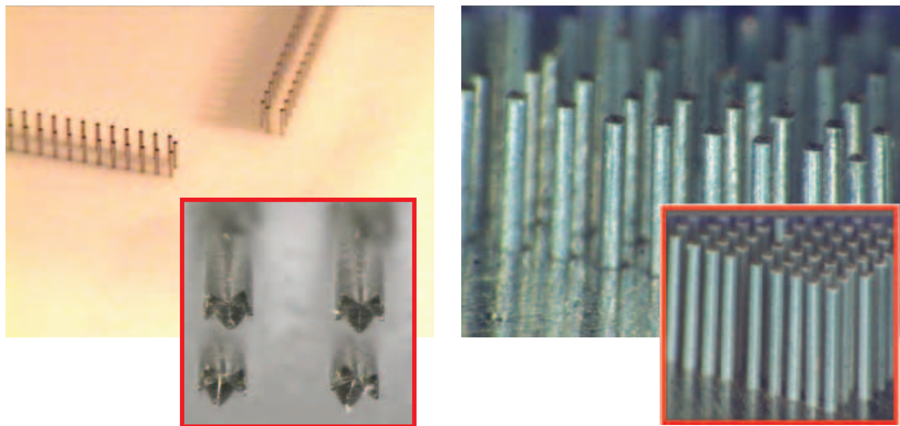


Figure 7. Images of cobra probe card.

A variation of the vertical probe card is the vertical probe card for probe on solder bumps. Vertical probe cards can be used on bond pads, or on solder bumps if the probe tips contain teeth. These images in Figure 7 show examples of a Cobra Probe Card for probe on bump. One can see the teeth at the end of the probe tip that press into the solder bump and maintain contact.

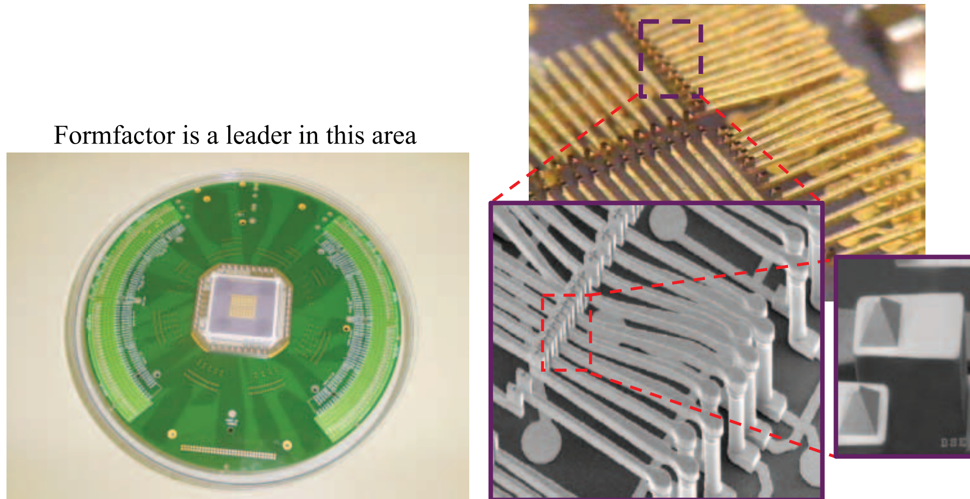


Figure 8. Illustration and images of MEMS probe cards.

Figure 8 is an example of a MEMS microcantilever probe card. We show the overall probe card on the left, and successively higher magnification images of the probe tips on the right. These probe tips are manufactured using a lithographic process. The metal structures form a supported rectangular structure that can flex in the middle. This is where we form the tip itself. The advantage of this type of probe card is that it can be manufactured through more automated processes. It also touches down in a manner similar to a vertical probe card. Furthermore, the structure of the probe and the probe tip result in a small mark with minimal chance of particle generation upon touchdown. These probe cards are now made by a number of manufacturers.

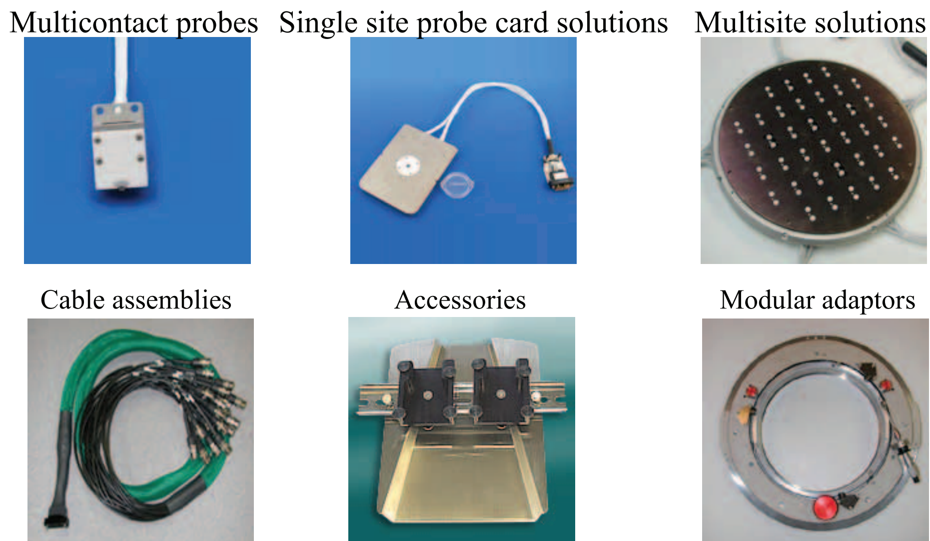
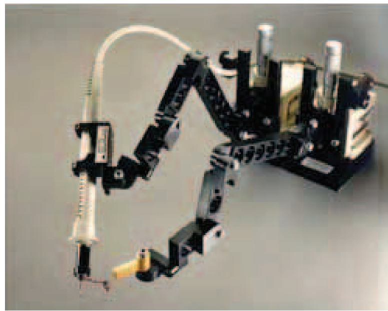


Figure 9. Celadon Systems.

While most companies address the general ATE market, Celadon specializes in reliability applications. They manufacture ceramic body cards that can be used to characterize single test structures or multiple sites on a wafer in parallel. Ceramic works well for wafer-level applications, since the ceramic can be manufactured with a thermal coefficient of expansion that is close to that of silicon. This works well for applications involving high temperature testing or thermal cycling. They also manufacture cable assemblies and other accessories for low noise, low leakage measurements. Their accessories include pin scramblers, light-tight enclosures, touch down sensors, cable clamps and supports, as well as modular adaptors that allow a probe card to sit firmly fixed to the probe station platen.

Active probe



Coplanar probes

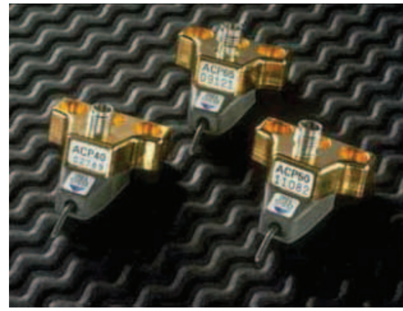


Figure 10. Images of high frequency probes.

One type of probe that is used occasionally in reliability measurements is the high frequency probe. A high frequency probe must be impedance-matched for the application. Two types of probes that fall into this category are active probes and co-planar probes. The two types shown here in Figure 10 are manufactured by Cascade Microtech. (now owned by FormFactor)

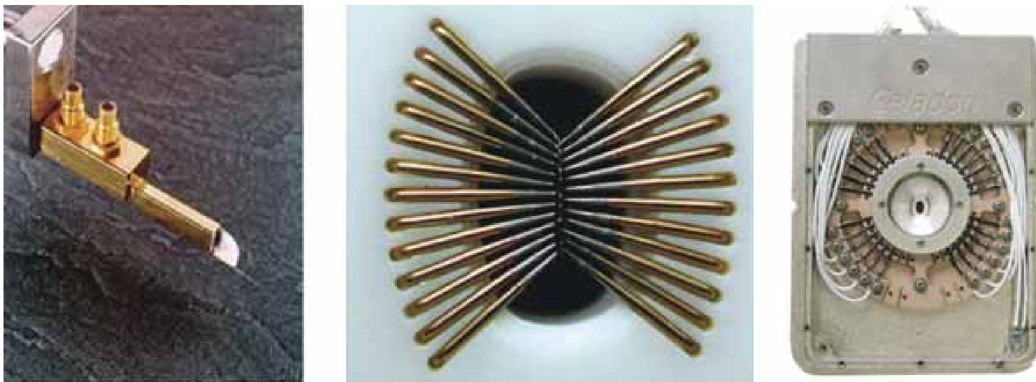


Figure 11. Images of low leakage/low noise probes.

Another major class of probes is the low leakage or low noise probe. Low noise requires additional shielding. The lowest noise probes use tri-axial cabling. The two levels of shielding allow measurements down into the femtoamp range. The key challenge is to shield the probe as close to the sample as possible. The probes shown in the center of Figure 11 shield to within 2 millimeters of the die surface.

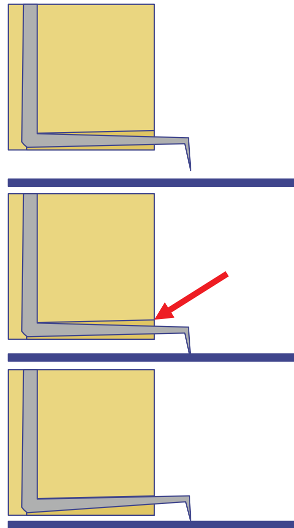


Figure 12. Technique for probe card damage prevention (probe channel).

We mentioned earlier that probe damage is a key concern. Probes can be dragged across the wafer surface by human error or equipment malfunction. This is a common problem with ceramic blade cards. This can cause the tips to go out of alignment, preventing contact with the probe pads. One method to help minimize probe damage is to use a probe channel (red arrow). The probe channel allows the probes to recede into the channel and protect the shafts from twists and torque. The reduced length of shaft exposed to the torque of the tips on the surface helps prevent misalignment problems.

There are several types of probe materials used for reliability applications. The most common probes are tungsten-based. Tungsten is a hard material that withstands numerous contacts with bond pads. Today, manufacturers are moving toward tungsten alloys. The most popular is tungsten-rhenium. It is less brittle than pure tungsten, giving it better properties for overdrive. It still has the hardness necessary for breaking oxide barriers on a probe pad to make good contact. It also has better wear resistance than pure tungsten and works well for high frequency measurements. Another common probe material is beryllium-copper. Beryllium-copper has a lower contact resistance, making it better for high power measurements where resistance can cause heating. They are also useful for measurements that require resolving small changes in resistance, like electromigration testing. Since the tips are softer, they require higher overdrive to make good contact for a long period of time. Therefore, they do not work well for burn-in or life test applications. Another common probe material is a fiber probe tip. Sometimes called cat whisker probes, these are useful in applications where one must avoid damage to the circuit. The downside of fiber probes is their high resistance.

Style	Tip diameter	Point radius (microns)	Point taper length	Material	Attributes
Fine tip	.005”	.35	.020”	Shank: nickel Tip: tungsten	Bendable, cat whisker, flexible tip and shaft
Heavy Duty Needle	.02”	0.5-200	0.06”-0.08”	Tungsten	Larger targets
Small Target with “C” bend	.005”	0.35	0.025”	Dumet (CuFe)	Bendable, cat whisker
High Temperature	.020”	5	.075”	Tungsten Carbide	For cutting
Small Targets	.001”	.5-10	.001”-.004”	Nickel	Bendable, cat whisker, super flexible
Low Contact Resistance	.020”	1.0	.135”	Beryllium Copper	For low contact resistance
High Compliance	.005”	.35	.020”	Shank: Nickel Tip: Tungsten	Fine tip, very flexible, prevents “fishhooking”
Very Small Targets	.003”	.1	.008”-.013”	Shank: Nickel Tip: Tungsten	Bendable cat whisker, sharpest probe

Figure 13. Basic probe tips comparison.

This chart in Figure 13 shows some basic probe tips and their uses.

References

Figures 10,11: Images courtesy FormFactor
Figure 11: Images courtesy Celadon Systems, Inc.

Technical Tidbit

Advanced Process Control

In this month's technical tidbit, we will discuss Advanced Process Control. Advanced Process Control, or APC, is a collection of techniques to improve and automate feedback to a wafer fabrication process to increase the yield.

Traditionally, engineers used control charts to monitor a tool's performance. They would monitor an output parameter like film thickness, or possibly an input parameter known to affect the output like chamber pressure, create a control chart to keep track of the data, look for deviations in the behavior, and then work to control and center the process. With APC, the goal is to automate this process to provide better control. This requires more emphasis on monitoring the input parameters and more emphasis on the decision-making process to help correct the problem in real-time.

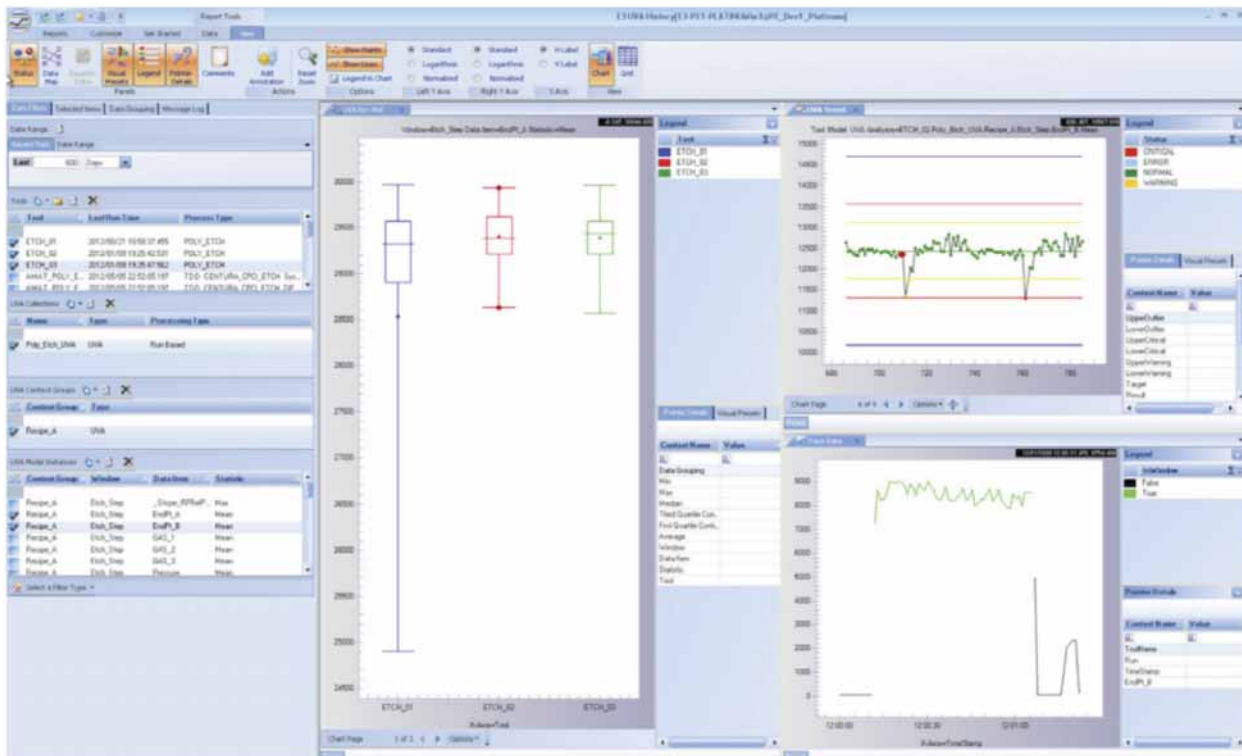


Figure 1.

Fault Detection and Classification, or FDC, is typically used as a part of advanced process control. FDC incorporates sensor data into a decision-making algorithm to allow the engineer to identify tool faults that can result in yield loss. This approach can be used on a variety of tools, such as plasma etch, lithography, and so forth. The algorithms used for this work can be simple. For example, one can use an

exponentially-weighted moving average, and look for data points that stray a certain distance away, such as one or two standard deviations. Today, some of those algorithms are more complex, such as a neural network that is trained to identify particular problems. Companies like Applied Materials now produce software that allows engineers to model and construct those algorithms. We show a screen shot of the software here in Figure 1.

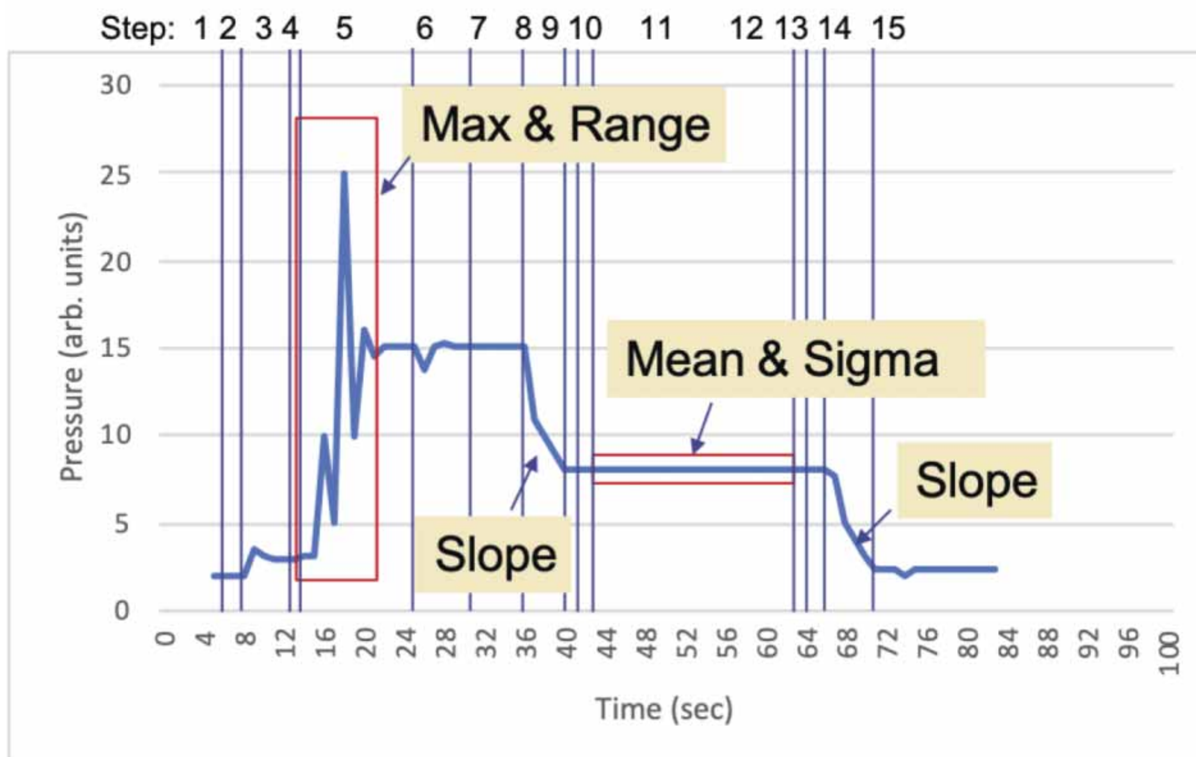


Figure 2.

Let's illustrate this problem in further detail. We show an example sensor dataset here in Figure 2. With just this single sensor trace, the Fault Detection engineer must investigate several features and develop multiple models, each with limits. We show an example of the types of event one might need to monitor, like: maximum values and ranges, mean values and standard deviations, and slopes. For the entire fab, there are often thousands, if not millions of models and limits to manage. Clearly, an opportunity exists for improvement in Fault Detection setup, execution and maintenance capabilities.

Ask the Experts

Q: How often do you sharpen a wafer dicing blade?

A: There are several factors involved. An important parameter that plays a role is the type of cut one is performing, like: a single cut, dual cut, or step cut. There are other parameters like feed rate and RPM that factor into the frequency of sharpening. With that said, you sharpen the dicing blade roughly every 10 meters or so.

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Spotlight: IC Packaging Technology

OVERVIEW

Overview: Integrated Circuit packaging has always been integral to IC performance and functionality. An IC package serves many purposes: (1) pitch conversion between the fine features of the IC die and the system level interconnection, (2) chemical, environmental and mechanical protection, (3) heat transfer, (4) power, ground and signal distribution between the die and system, (5) handling robustness, and (6) die identification among many others. Numerous critical technologies have been developed to serve these functions, technologies that continue to advance with each new requirement for cost reduction, space savings, higher speed electrical performance, finer pitch, die surface fragility, new reliability requirements, and new applications. Packaging engineers must fully understand these technologies to design and fabricate future high-performance packages with high yields at exceptional low-costs to give their company a critical competitive advantage.

This two-day class will detail the vital technologies required to construct IC packages in a reliable, cost effective, and quick time to market fashion. When completed, the participant will understand the wide array of technologies available, how technologies interact, what choices must be made for a high-performance product vs. a consumer device, and how such choices impact the manufacturability, functionality, and reliability of the finished product. An emphasis will be given to manufacturing, processes and materials selection tailoring and development. Each fundamental package family will be discussed, including flip chip area array technologies, Wafer Level Packaging (WLP), Fan-Out Wafer Level Packaging (FO-WLP), and the latest Through Silicon Via (TSV) developments. Additionally, future directions for each package technology will be highlighted, along with challenges that must be surmounted to succeed.

WHAT WILL I LEARN BY TAKING THIS CLASS?

1. **Molded Package Technologies.** Participants learn the fundamentals of molding critical to leaded, leadless, and area array packaging, enabling them to eliminate problems such as flash, incomplete fill, and wire sweep.
2. **Flip Chip Technologies.** Participants learn the fundamentals of plating, bumping, reflow, underfill, and substrate technologies that are required for both high performance and portable products.
3. **Wafer Level Packages.** Participants learn the newest technologies that enable the increasingly popular Wafer Chip Scale Level Packages (WCSPs) and Fan-Out Wafer Level Packages (FO-WLPs).
4. **Through Silicon Via Packages and Future Directions.** Participants will know the latest advances in the recently productized TSV technology, as well as future directions that will lead to the products of tomorrow.

COURSE OBJECTIVES

1. The course will supply participants with an in-depth understanding of package technologies current and future.
2. Potential defects associated with each package technology will be highlighted to enable the student to identify and eliminate such issues in product from both internal assembly and OSAT houses.
3. Cu and solder plating technologies will be described with special emphasis on package applications in TSVs and Cu pillars for FO-WLPs. Emphasis will be placed on eliminating issues such as reliability, non-uniformity, void free thermal aging performance, and contamination free interfaces.

4. New package processes employed in Through Silicon Via production will be described, along with current cost reduction thrusts, to enable the student to understand the advantages and limits of the technologies.
5. Temporary bonding and wafer thinning processes will be highlighted, as well as the cost reduction approaches currently being pursued to enable wider adoption of TSV packages.
6. The trade-offs between silicon, glass, and organic interposers will be highlighted, along with the processes used for each.
7. Participants will gain an understanding of the surface mount technologies that enable today's fine pitch products.
8. The class will provide detailed references for participants to study and further deepen their understanding.

COURSE OUTLINE

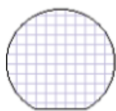
1. The Package Development Process as a Package Technology:
    a. Materials and Process Co-Design
2. Molded Package Technologies:
    a. Die Attach
        i. Plasma Cleans
    b. Wire Bonding
        i. Au vs. Cu vs. Ag
        ii. Die Design for Wire Bonding
    c. Lead Frames
    d. Transfer and Liquid Molding
        i. Flash
        ii. Incomplete Fill
        iii. Wire Sweep
        iv. Green Materials
    e. Pre- vs. Post-Mold Plating
    f. Trim Form
    g. Saw Singulation
    h. High Temperature and High Voltage Materials
3. Flip Chip and Ball Grid Array Technologies:
    a. Wafer Bumping Processing
        i. Cu and Solder Plating
        ii. Cu Pillar Processing
    b. Die Design for Wafer Bumping
    c. Flip Chip Joining
    d. Underfills
    e. Substrate Technologies
        i. Surface Finish Trade-Offs
        ii. Core, Build-up, and Coreless

  f. Thermal Interface Materials (TIMs) and Lids
  g. Fine Pitch Warpage Reduction
  h. Stacked Die and Stacked Packages
  i. Material Selection for Board Level Temperature Cycling and Drop Reliability

4. Wafer Chip Scale Packages:
   a. Redistribution Layer Processing
   b. Packing and Handling
   c. Underfill vs. No-Underfill
5. Fan-Out Wafer Level Packages:
   a. Chip First vs. Chip Last Technologies
   b. Redistribution Layer Processing
   c. Through Mold Vias
6. Through Silicon Via Technologies:
   a. Current Examples
   b. Fundamental TSV Process Steps
      i. TSV Etching
      ii. Cu Deep Via Plating
      iii. Temporary Carrier Attach
      iv. Wafer Thinning
   c. Die Stacking and Reflow
   d. Underfills
   e. Interposer Technologies: Silicon, Glass, Organic
7. Surface Mount Technologies:
   a. PCB Types
   b. Solder Pastes
   c. Solder Stencils
   d. Solder Reflow

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).



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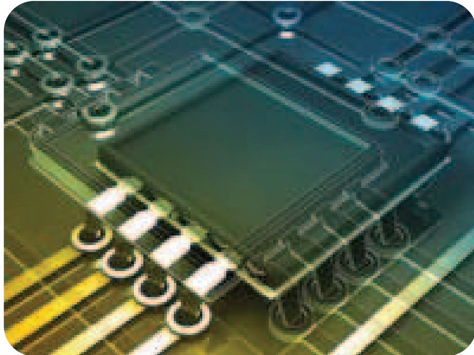

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Failure and Yield Analysis
April 20 – 23, 2020 (Mon – Thur)
Munich, Germany

IC Packaging Technology
April 27 – 28, 2020 (Mon – Tue)
Munich, Germany

Advanced CMOS/FinFET Fabrication
April 30, 2020 (Thur)
Munich, Germany