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Overview of Statistical Process Control Part 1

By Christopher Henderson

In this article, we begin to provide a four-part overview of statistical process control.

Here is the outline. First, we'll introduce the basics of statistical process control, including the motivation for statistical process control. We'll discuss control chart basics, including how to set up a control chart, and how to monitor a control chart. We'll then discuss process capability index.

We begin by introducing statistical process control. Statistical Process Control, or SPC, is a collection of problem-solving tools the industry uses to achieve process stability and reduce variability in a process. This could be a manufacturing or testing process. The primary visualization tool for SPC is the control chart. This chart was developed by Dr. Walter Shewhart, who worked at Bell Laboratories back in the 1920s.

Why is statistical process control important? If we back up for a minute to think about the problem from a philosophical point of view, we can't fix problems unless we first understand them. The question then would be, "okay, how do we understand them?" We do this by taking measurements, and in particular, measurements of pertinent parameters. We may not know which parameters are important priority ahead of time, so this may require trial and error. Once we have our measurement values, what do we do with them? The next

In this Issue:

step is to utilize mathematical models—in particular, statistics—to organize the data, track it, and look for changes. This activity is what we call Statistical Process Control.

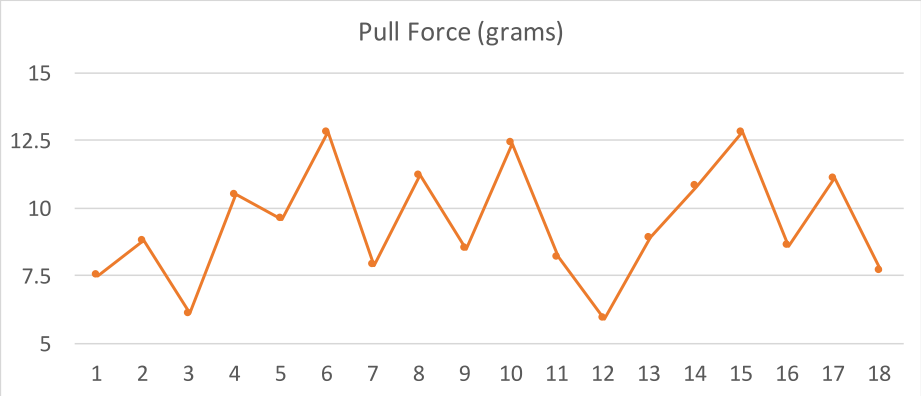


Figure 1. Control chart example.

Let's move to a more practical discussion of the control chart. The control chart provides a means to measure a quality characteristic from a sample vs. the sample number or time. Once we have the data, we typically apply limits to the chart—known as control limits—to determine if the data points lie outside the limits. A typical range for the control limits would be ± 3σ. We show an example of a control chart here in Figure 1, with 18 data points. This chart might represent the pull force on wirebonds, for example.

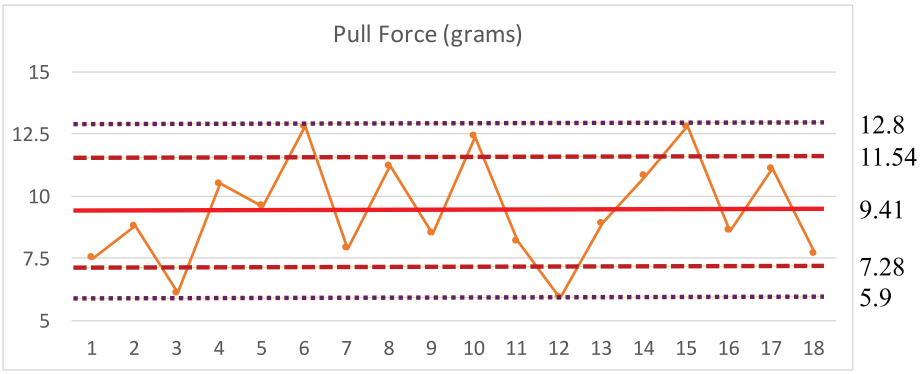


Figure 2. Control chart: $\bar{x}$, *R*, and *S*.

In control chart terminology $\bar{x}$ refers to the sample mean, shown here in Figure 2 as a red line through the chart. R refers to the sample range, or x_{max} - x_{min}, shown here as the upper and lower dotted magenta lines. S refers to the standard deviation, shown here as the two dashed red lines. In this example, we're showing one standard deviation above and below the mean, but we might choose other amounts, like three standard deviation units. The standard deviation is 2.13 for this data set.

Now that we have our data plotted on a control chart, we need to think about how to monitor the chart. First, we need to choose the appropriate control chart for your data. Determine the appropriate time period for collecting and plotting data. Collect data, construct your chart and analyze the data. Look for "out-of-control signals" on the control chart. When one is identified, mark it on the chart and investigate the cause. Document how you investigated, what you learned, the cause and how it was

corrected. Continue to plot data as they are generated. As each new data point is plotted, check for new out-of-control signals. Remember that when you start a new control chart, the process may be out of control. If so, the control limits calculated from the first 20 points are conditional limits. When you have at least 20 sequential points from a period when the process is operating in control, recalculate control limits.

Many times, patterns might be evident in a control chart, and these patterns can indicate something about the process. The more common patterns have names. For instance, a pattern of points on one side of the centerline is called a "run." This would normally be a low probability event in a random chart. Other types of patterns include mixtures, or points from 2 or more distributions; shifts, or an abrupt change in the data; and stratification, or charts that exhibit extremely low variability.

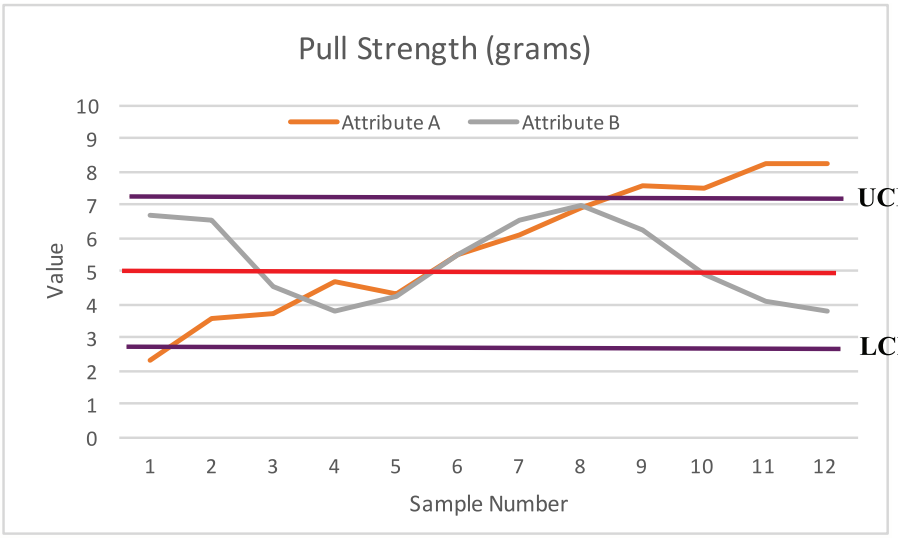


Figure 3. Example patterns in a control chart.

Here are some examples of patterns in a control chart in Figure 3. In this example, Attribute A is a trend, since the typical data point slowly increases in value in the chart. Attribute B is a cycle, since the typical data point varies back and forth in a regular pattern around the mean.

How do we know we have an actual pattern and not simply random variation in the data? There are criteria for how to determine this. This slide lists the typical patterns we might be interested to detect. Any single point plots beyond the 3σ limits; 2 out of 3 consecutive points plotted beyond the 2σ warning limits; 4 out of 5 consecutive points plot beyond 1σ; 9 consecutive points plot on the same side of the centerline; 6 consecutive points increase or decrease; 14 consecutive points alternate up and down; and 15 consecutive points plot on either side of average. This criteria were developed by Western Electric and published in their Statistical Quality Control Handbook in the mid-1950s.

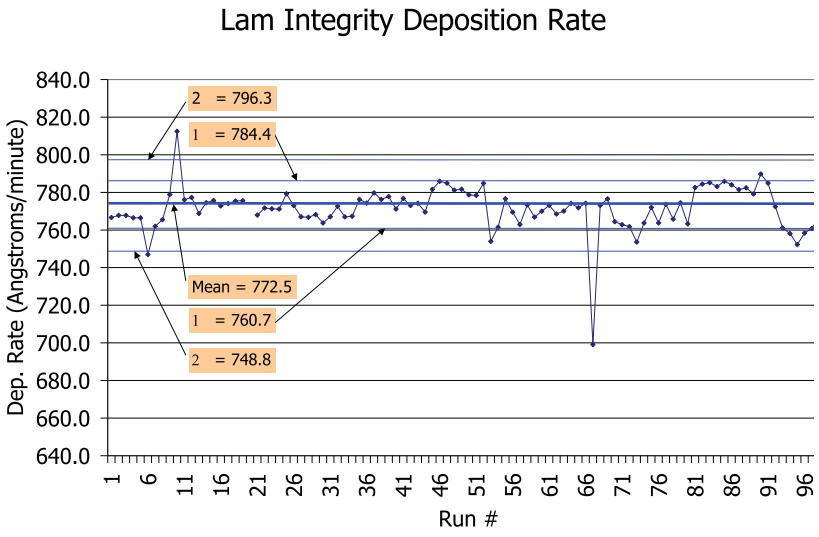


Figure 4. Example control chart.

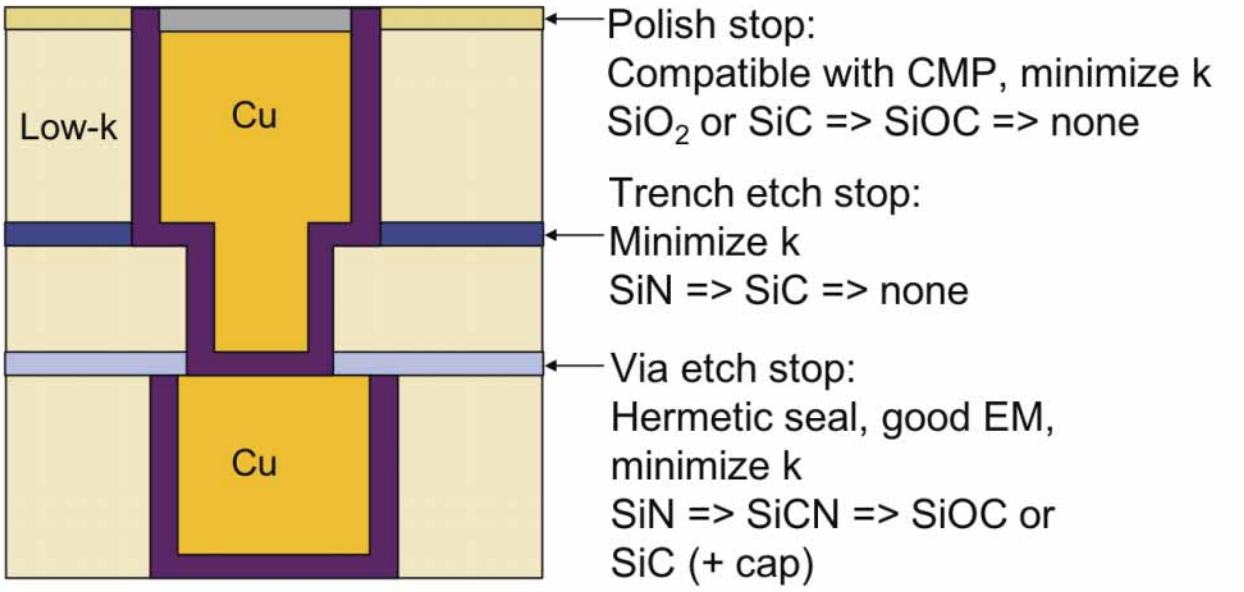
Let's look at an example control chart in Figure 4. Is this process in control? The answer is no. Notice that there are two significant spikes—one around run number 12, and another one around run number 67—that exceed the 3σ limits. There is also a run of about 10 points above the trend line around runs 82 through 92. These conditions are patterns that indicate the overall process is not in control.

To be continued next month…

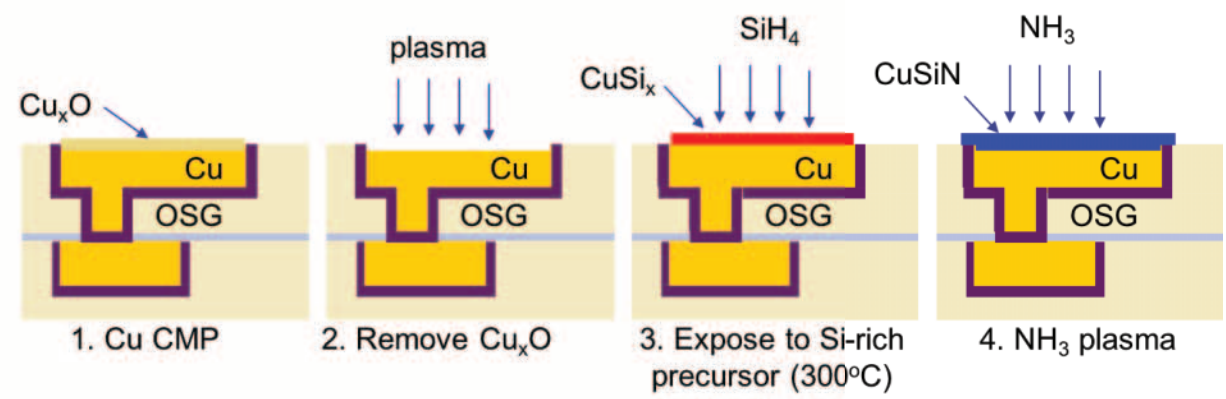
Technical Tidbit

Copper Capping Layers

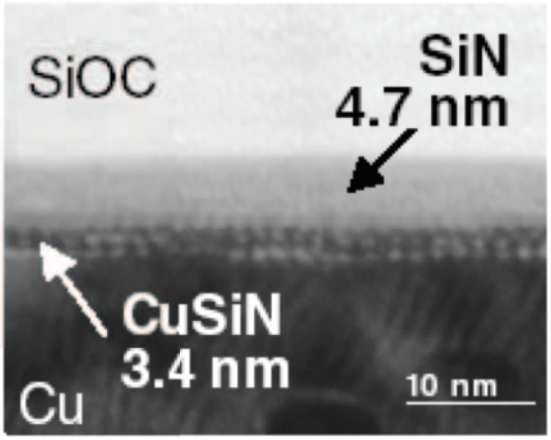
In this technical tidbit, we will discuss capping layers for copper metallization. Uncapped copper layers typically do not perform well. They exhibit increased surface scattering, which leads to higher resistance, and lower electromigration strength. Therefore, capping the copper layer can help improve the performance of the copper metal interconnect.



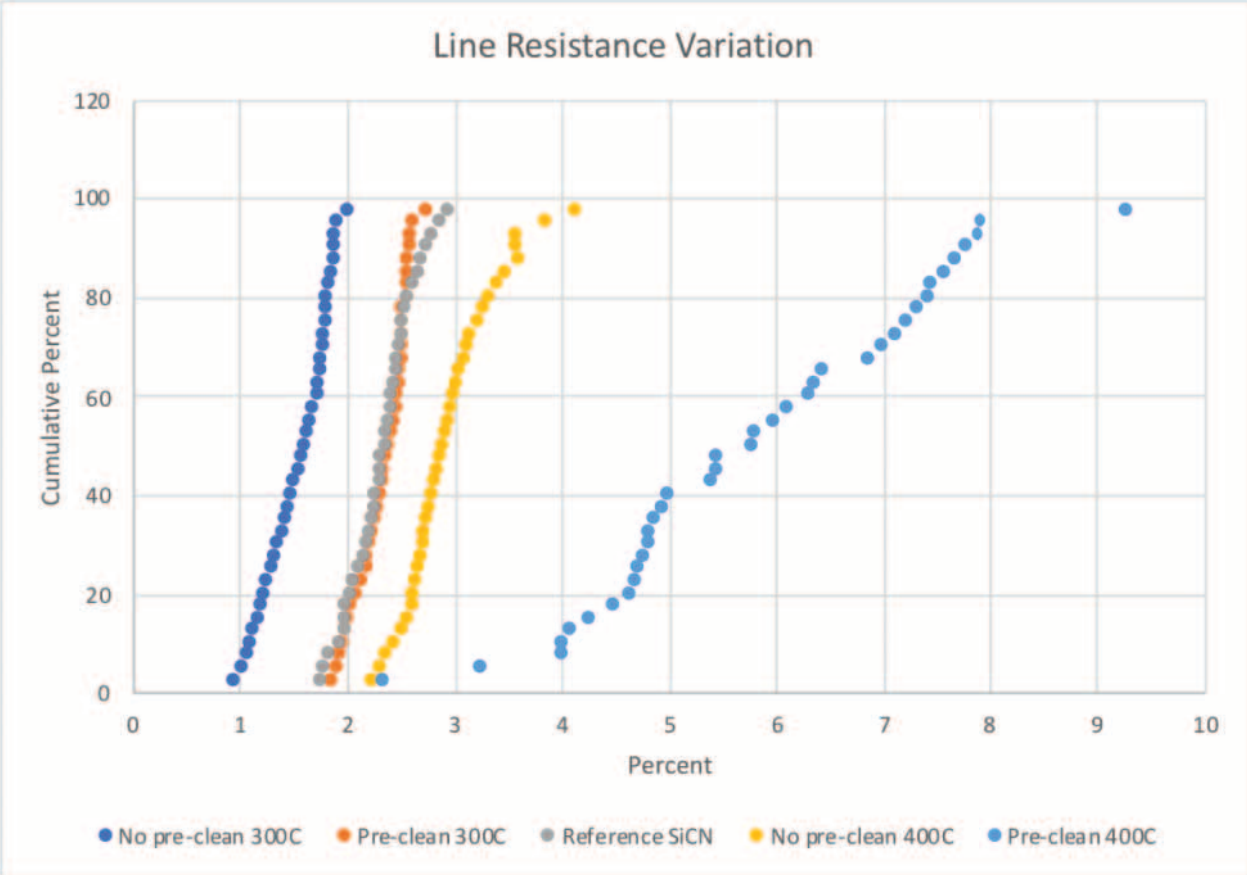
This cross section view shows the typical material structure for a copper/low-k interconnect scheme. The low-k dielectrics are shown in light tan. Low-k dielectrics might use a polish stop. The industry started with materials such as silicon dioxide or silicon carbide, and then migrated to a silicon oxycarbide, and then to no polish stop. Low-k dielectrics might require a trench etch stop. The goal would be to minimize the dielectric constant of this layer, so the industry started with silicon nitride, then migrated to silicon carbide, and then to no trench stop. Low-k dielectrics might also require a via etch stop. This layer must provide a hermetic seal, good electromigration resistance, both while minimizing the dielectric constant. The industry started with silicon-nitride, then migrated to silicon carbon nitride, then to silicon carbide with an optional capping layer.



- Selective SiH_4 reaction with Cu
- Need Cu_xO removal to achieve uniform CuSiN layer
- Need low temperature SiH_4 to keep low resistance



In these figures we show the typical process steps associated with a copper-silicon-nitride capping layer. First, we perform chemical mechanical planarization to planarize the copper metallization layer and surrounding dielectrics. During this process and immediately afterwards, the copper surface will oxidize. We use a plasma etch to remove this oxide layer. Next we expose the surface to silane, which acts as a precursor to deposit silicon, react it with the surface, and improve bonding. We then immediately follow this step with an ammonia surface reaction to create the copper-silicon-nitride layer. There are a couple of important points to emphasize about this process. First, we need to remove the copper oxide to achieve a uniform copper-silicon-nitride layer. Second, the silane reaction is a selective reaction with the copper; it doesn't react with the dielectric layers. And third, we use a low-temperature silane reaction to maintain a low resistance in the copper material. We show a transmission electron microscope image of the interface here.



This graph shows the line resistance variation as a function of capping layer. Notice that the pre-clean leads to an increase in line resistance, as well as a wider variation in the process. Plasma preclean is standard, so this is a knob the fab can adjust, but it is not a knob that the design team can adjust.

Ask the Experts

Q: Why is there a diamond-shaped structure on the source and drains of FinFETs?

A: This diamond shape is due to the deposition of additional material (either silicon or silicon-germanium) on a [110] crystal surface. Quite often, process engineers deposit additional material to help lower the source and drain resistances. The deposition process leads to the formation of the diamond structure due to the crystal structure on the sidewalls of the fins, which exhibit a [110] crystal structure.

IRPS

International Reliability Physics Symposium

2019 IEEE International Reliability Physics Symposium

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March 31- April 4, 2019
Hyatt Regency Monterey,
Monterey, CA, 93940-4908, USA

Registration is available at www.irps.org

Chris Henderson, Semitracks President

Chris would be happy to meet with you and discuss any training needs you have. Contact him at henderson@semitracks.com anytime before the symposium!

Spotlight: Advanced CMOS/FinFET Fabrication

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" Advanced CMOS/ FinFET Fabrication is a 1-day course that offers detailed instruction on the processing used in a modern integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

WHAT WILL I LEARN BY TAKING THIS CLASS

By concentrating on the latest developments in CMOS and FinFET technology, participants will learn why FinFETs and FD-SOI are fast becoming the technologies of choice at feature sizes below 20nm. Our instructors work hard to explain semiconductor processing without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants learn basic but powerful aspects about FinFET technology. This skill-building series is divided into four segments:

1. Front End Of Line (FEOL) Overview. Participants study the major developments associated with FEOL processing, including ion implantation, Rapid Thermal Annealing (RTA) for implants and silicides, and Pulsed Plasma Doping. They also study alternate substrate technologies like SOI as well as High-k/Metal Gates for improved leakage control.
2. Back End Of Line (BEOL) Overview. Participants study the major developments associated with BEOL processing, including copper metallization and Low-k Dielectrics. They learn about why they're necessary for improved performance.
3. FinFET Manufacturing Overview. Participants learn how semiconductor manufacturers are currently processing FinFET devices and the difficulties associated with three-dimensional structures from a processing and metrology standpoint.
4. FinFET Reliability. They also study the failure mechanisms and techniques used for studying the reliability of these devices.

COURSE OBJECTIVES

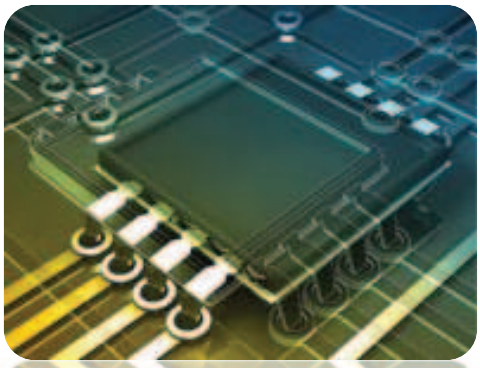
1. The seminar will provide participants with an in-depth understanding of SOI technology and the technical issues.
2. Participants will understand how Hi-K/Metal Gate devices are manufactured.
3. Participants will also understand how FinFET devices are manufactured.

4. The seminar provides a look into the latest challenges with copper metallization and Low-k dielectrics.
5. Participants will understand the difficulties associated with non-planar structures and methods to alleviate the problems.
6. Participants will be able to make decisions about how to evaluate FinFET devices and what changes are likely to emerge in the coming years.
7. Participants will briefly learn about IC reliability and the failure modes associated with these devices.
8. Finally, the participants see a comparison between FD-SOI (the leading alternative) and FinFETs.

COURSE OUTLINE

1. Advanced CMOS Fabrication – Introduction
2. Front End Of Line (FEOL) Processing
    a. SOI and FD-SOI
    b. Ion Implantation and Rapid Thermal Annealing
    c. Pulsed Plasma Doping
    d. Hi-K/Metal Gates
    e. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology
3. Back End Of Line (BEOL) Processing
    a. Introduction and Performance Issues
    b. Copper
        i. Deposition Methods
        ii. Liners
        iii. Capping Materials
        iv. Damascene Processing Steps
    c. Lo-k Dielectrics
        i. Materials
        ii. Processing Methods
    d. Reliability Issues
4. FinFET Manufacturing Overview
    a. Substrates
        i. Bulk
        ii. SOI
    b. FinFET Types
    c. Process Sequence
    d. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology

5. FinFET Reliability
   a. Defect density issues
   b. Gate Stack
   c. Transistor Reliability (BTI and Hot Carriers)
   d. Heat dissipation issues
   e. Failure analysis challenges
6. Future Directions for FinFETs
   a. Comparison of FD-SOI and FinFETs – Are FinFETs a better choice?
   b. Scaling



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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Failure and Yield Analysis
April 23 – 26, 2019 (Tue – Fri)
Munich, Germany

Wafer Fab Processing
April 23 – 26, 2019 (Tue – Fri)
Munich, Germany

EOS, ESD and How to Differentiate
April 29 – 30, 2019 (Mon – Tue)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 6 – 9, 2019 (Mon – Thur)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 13 – 16, 2019 (Mon – Thur)
Tel Aviv, Israel

Introduction to Processing
June 3 – 4, 2019 (Mon – Tue)
San Jose, California, USA

Advanced CMOS/FinFET Fabrication
June 5, 2019 (Wed)
San Jose, California, USA

Interconnect Process Integration
June 6, 2019 (Thur)
San Jose, California, USA

Failure and Yield Analysis
June 3 – 6, 2019 (Mon – Thur)
San Jose, California, USA