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Underfills, Part 2

By Christopher Henderson

Underfill materials can be categorized as either flow or no-flow materials. There are two types of underfill materials: reworkable and non-reworkable. Despite some potential reliability problems, the industry appears to be moving towards reworkable underfills.

After the flip chip or chip-scale package has been reflowed onto the system board, the fluid underfill is dispensed. The fluid underfill is drawn under the device by capillary action. Curing takes place at a temperature typically between 130°C and 160°C, although "snap cures" may cure in a few seconds. Most underfills consist of about 70 percent filler particles by weight. The epoxy resin itself—without filler particles—has a coefficient of thermal expansion (CTE)

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of 50 to 70 ppm/°C. Filler particles bring the CTE of the cured underfill close to that of the solder bumps—21 ppm/°C.

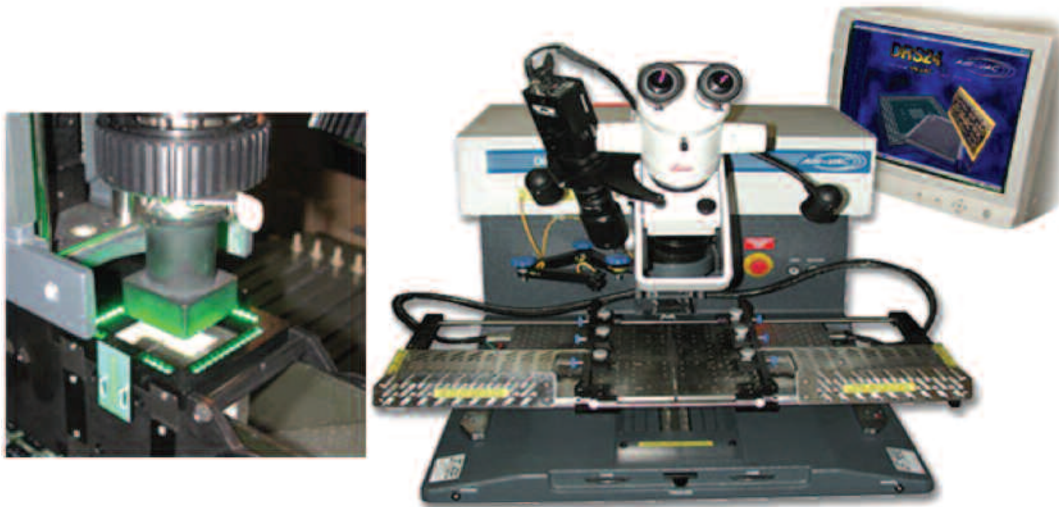
No-flow underfill materials are deposited on the system board before the flip chip or chip-scale package is attached and reflowed. The flip chip or chip-scale package solder bumps push downward through the no-flow underfill to make contact with the pads. Since they have no filler particles, no-flow underfills have higher CTEs. Using a no-flow underfill may increase throughput because underfill cure and solder reflow take place simultaneously. No-flow underfills are especially useful with RF devices that are covered by shields. No-flow underfills act as a flux, and it is important for flip chips (but less important for chip-scale packages) that the acidic flux be completely converted to resin during cure. Thermal analysis via DSC and TGA can determine the state of cure. Without full cure, acidic chlorine compounds may damage the chip face in spite of the passivation layer. For flip chips, a one-hour bake at 125°C may be necessary to completely convert the flux in a no-flow underfill. In chip-scale packages though, the no-flow underfill contacts the interposer board, which is relatively insensitive to chlorine. Chip-scale packages may even be able to use less costly adhesive materials rather than true underfills.

Non-reworkable underfills have no filler materials and therefore exhibit a faster flow rate. This means that the capillary action is quicker allowing the underfill to more efficiently flow around even fine-pitched solder ball arrays. In addition—since a non-reworkable underfill has no filler materials—it can be applied to the entire surface of a die and will more easily move out of the way when the package is pressed to the board. This reduces the possibility of electrical opens. Non-reworkable underfills can be cured quickly, normally in less than five minutes. Loctite and other manufacturers make a variety of underfill materials. Loctite 3566 is an example of a popular non-reworkable underfill. This class of underfills is used in high volume production where through-put is an issue.

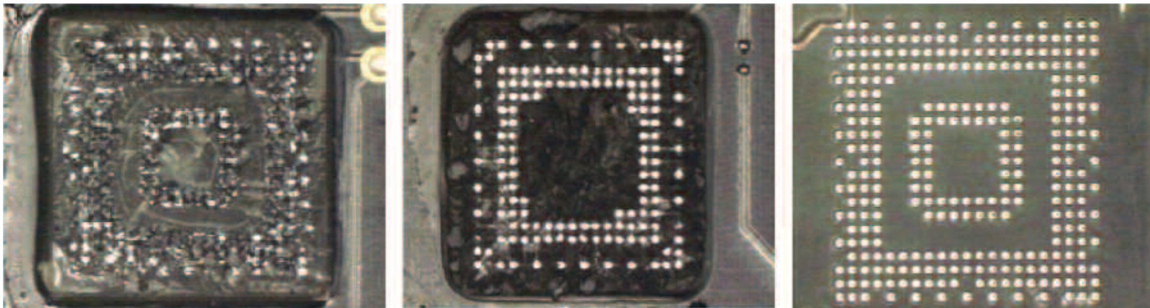
A variety of research groups are currently working on reworkable underfills. Reworkable underfills fall into four different groups: chemically reworkable, thermally-reworkable, chemical additives to existing materials, and thermoplastic materials. Chemically reworkable underfills are currently the leading contenders. They have an acetal group in the center of the diepoxide. They are stable to the application of heat, but tend to break apart in an acid or solvent solution. One can then use an acid safe to the chip, package, and board that will attack the acetal group, causing the underfill to soften and dissolve. High temperature removal underfills are also being investigated. Their use will probably be limited to ceramic or other high temperature substrates. Furthermore, the remaining chips would have to have their underfill replaced because of the difficulty associated with limiting the heat to a single component. Researchers have also been investigating chemical additives and thermoplastic materials. In a chemical additive, the idea is to include a chemical in the underfill that—when heat is applied—migrates to the interfaces causing the underfill to lose adhesion to the package, board, and solder balls. Both chemical additive work and thermoplastic material work are in their infancies, and so there is no published reliability data at this time.

One method for making an underfill reworkable is to add a component into the diepoxide that is chemically unstable in the presence of heat. To date, most reach has focused on using monomers, since

they have a special chemical linkage that breaks down when heated. The problem with this approach is that these materials do not adhere to the board as well once they are heated. A rework operation can leave the underfill weak and susceptible to delamination, reducing the reliability of the assembly. Second, this class of material requires longer cure times. This can substantially increase the assembly times, driving up the cost of a product. An example of this type of material is Loctite 3567. It has been successfully used in rework situations.



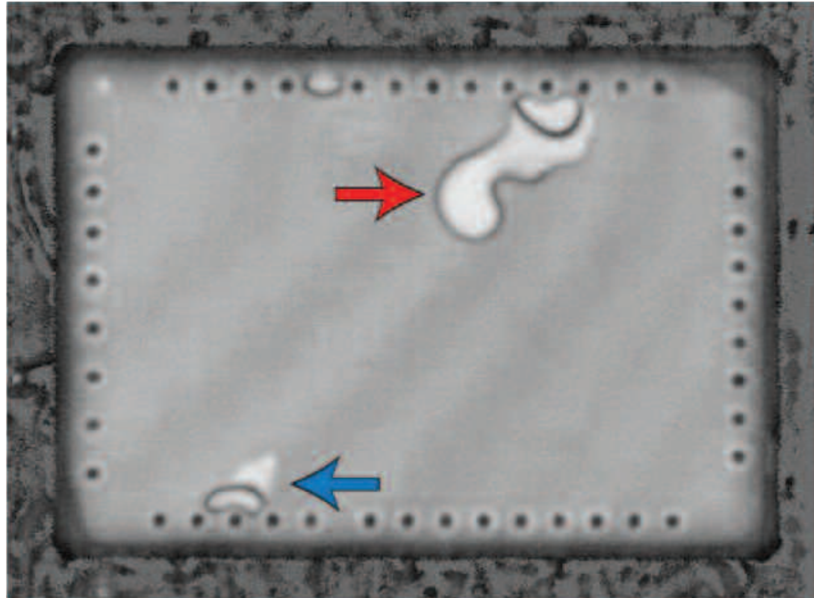
Here we show an example of a ball grid array underfill rework station. These machines—like the one shown here from Air-Vac Engineering—heat the sample with hot air to loosen the solder and the underfill. A vacuum chuck holds the assembly in place. Once the materials are soft, the system twists the BGA with respect to the board to remove it.



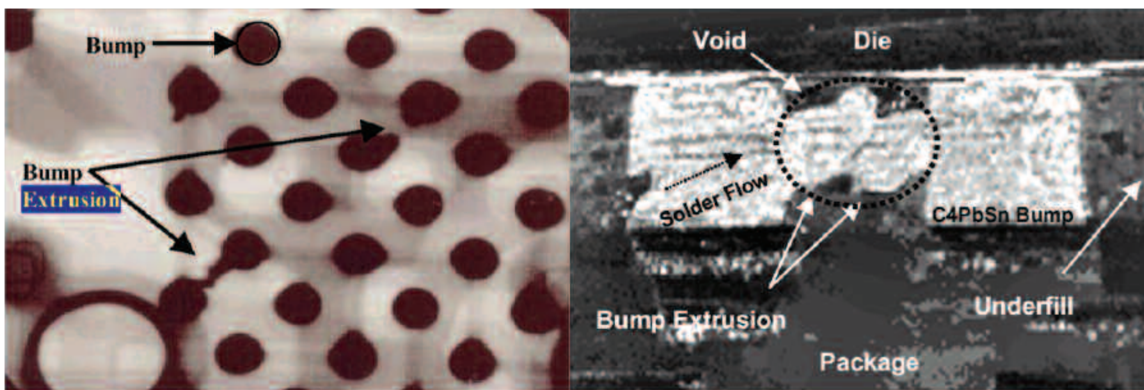
Here are some images showing the BGA surface after the machine has removed the component. Immediately after removal, the landing pads and underfill can be quite uneven. This means that a cleaning step is required to remove the underfill material and prepare the landing pads on the board to accept a replacement component. The center image shows the landing pads after cleaning on the rework station, while the image on the right shows the area after a final clean. Done correctly, this process can allow the replacement of many surface mount components.

The industry is currently assessing the advantages and disadvantages of both reworkable and non-reworkable underfills. A non-reworkable underfill can be deposited and cured more quickly, allowing for faster production times and lower production costs. This advantage is offset by the fact that a non-reworkable underfill can make it difficult to remove the chip from the board. In fact, one is likely to damage the board trying to remove the component. There is no ability for rework in this scenario. Using a

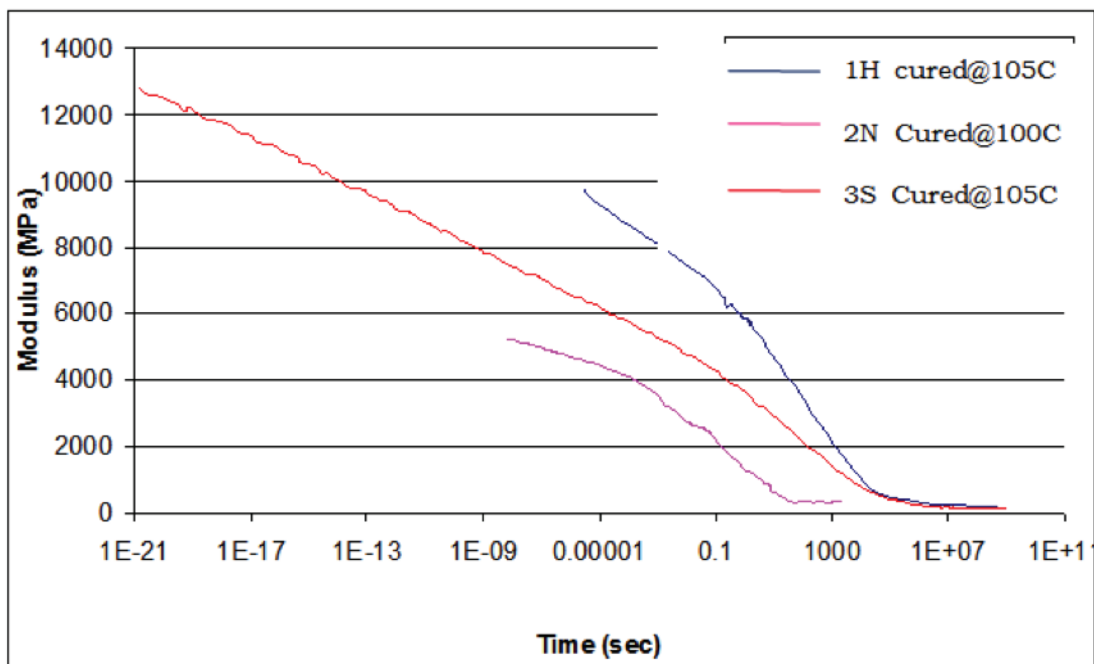
non-reworkable underfill requires a known good die, so extensive electrical test and characterization must be performed before placing the component on the board. Because of these problems, the industry appears to be moving away from non-reworkable underfills towards reworkable ones.



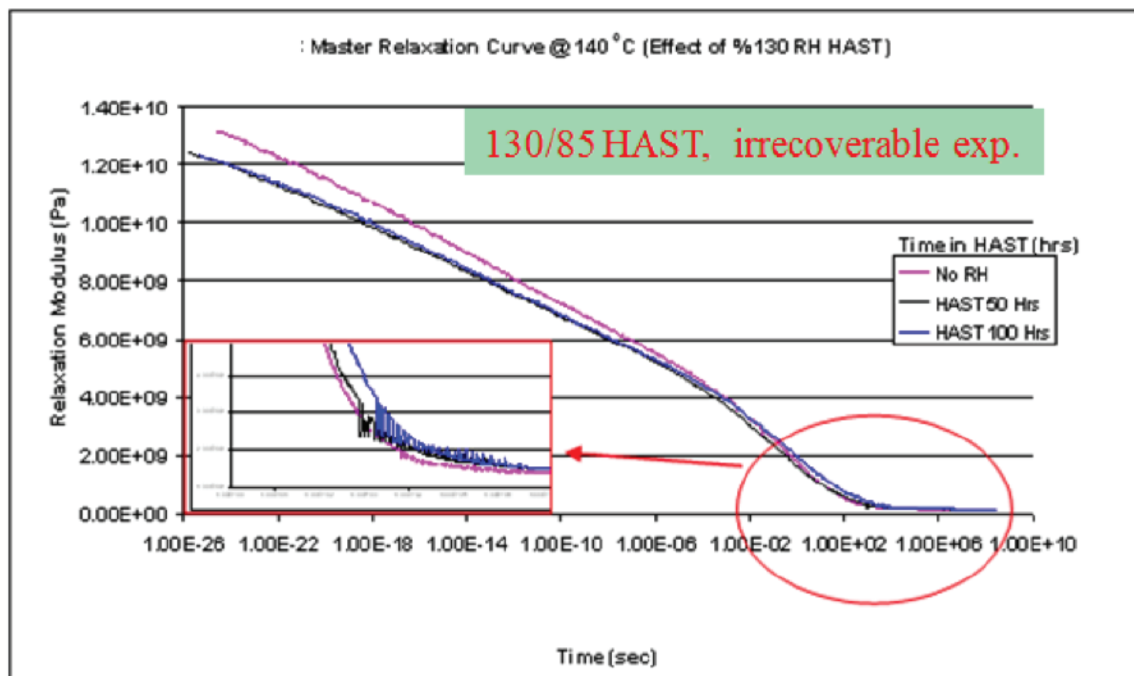
Some common problems with BGA underfills from a quality standpoint include bubbles, incomplete coverage, and delamination. Bubbles tend to be more of a concern with a direct epoxy application, where incomplete coverage tends to be more of a problem with a capillary flow-deposited underfill. There are four surfaces involved in the BGA underfill process. These five surfaces are the die, the solder bumps, the passivation layer, the system board, and the solder mask on the system board. The bonding of the underfill to the four surfaces is vital in establishing the integrity of the flip chip or chip-scale package. The solder mask presents two challenges for successful underfill bonding. The solder mask may have an irregular topography. While flowing over these irregularities, the fluid underfill may trap air that voids in the cured underfill. Second, both the solder mask and the board can absorb moisture. The heat of reflow can convert this moisture into steam and create voids. Delaminations can occur if there is excessive shock to the assembly, contamination at an interface, or improper wetting of the epoxy to the package or to the board.



A major issue with underfill materials is voiding. Solder can then extrude into these voids under certain conditions. During temperature cycling, the solder is under compressive stress. If there are voids in the underfill close to the solder, it then can extrude into these voids. If enough solder extrudes into the void—and if the void bridges between solder bumps—then a short can occur. An open can occur as well if the solder volume goes down significantly. The good news is that one can detect these voids using scanning acoustic microscopy, and detect the extrusion using x-ray radiography, both non-destructive techniques. The solution is to create a void-free underfill process. This can be a big challenge with fine pitches, low standoff heights, and underfill materials that are more closely matched to the die and substrate.



The ability of an underfill to withstand the shock associated with a drop test is closely related to the underfill's behavior in the Linear Viscoelastic—or LVE—regime. The graph shown here shows the LVE response for three different underfills. Notice that at short time durations, the modulus of each underfill is substantially different. The long time duration values are also somewhat different as well. The impact of this can be hard to understand. A higher modulus translates into more rigidity during the drop test. This can be both good and bad: good from the standpoint of preventing shear within the bump, bad from the standpoint of preventing shear at the underfill interfaces.



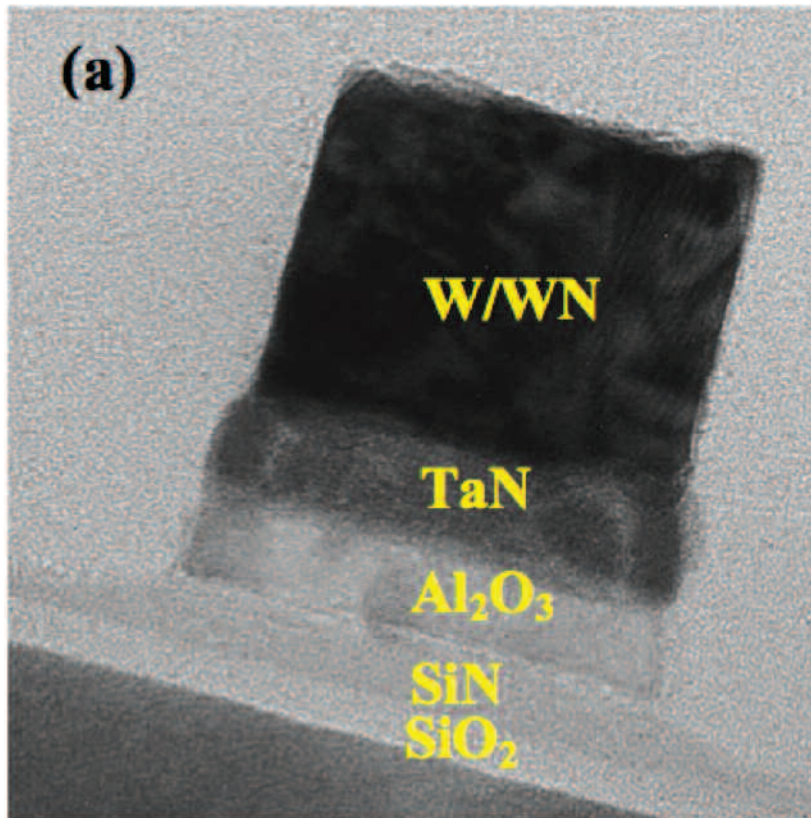
The presence of moisture further complicates the underfill performance. In this graph, the specimens subjected to HAST condition yield lower instantaneous modulus than the base line sample with no relative humidity (13 GPa vs. 12 GPa). Furthermore, the short term viscoelastic properties did not recover. The long term modulus seems to be not affected by HAST. Also 50 hrs HAST and 100 hrs HAST did not yield any difference on the viscoelastic properties of the underfill.

In conclusion, underfills provide the opportunity for improved mechanical strength at the chip-board interface, and reliability of that interface. This is particularly important for mobile phones and other portable electronics where flexing or dropping may occur. The industry uses both flow and no-flow materials in production. No-flow is faster, but solder joint integrity can be more challenging. The industry also uses both reworkable and non-reworkable materials. Reworkable materials allow for easier repair and chip replacement, but take longer to cure. Some major concerns with underfills include voiding and the risk of solder bump shorts, incomplete coverage, and materials property changes related to shock timeframe and humidity. There is still development work going on in research labs with these materials, so expect to see improvements and changes in the future.

Technical Tidbit

TANOS Memory

TANOS is a type of nitride charge trapping memory that shows some promise for certain applications. TANOS stands for Tantalum Nitride – Aluminum Oxide – Silicon Nitride – Silicon Dioxide – Silicon. It is similar to SONOS (Silicon – Oxide – Nitride – Oxide – Silicon), but uses a metal gate and aluminum oxide to change the energy band characteristics, leading to better data retention times.



Charge trapping memory cells have the advantage over floating gate cells in terms of multi-level cell operation because the floating- gate interference effect hurts the cell distribution severely in sub-50nm regime. However, the conventional SONOS cell programmed and erased by Fowler-Nordheim (FN) tunneling cannot be applied for high-density NAND flash memory for its poor data retention characteristics.

The use of thicker (>30A) tunnel oxides are an important method for improving data retention without losing erase speed. The TANOS memory was developed by Chang-Hyun Lee and his colleagues at Samsung Semiconductor in the early 2000's decade. The first TANOS device structure used a high-k dielectric as a blocking layer and a higher work function metal gate to allow for a thicker tunnel oxide. Samsung developed a 4 Gb single-level NAND flash memory with TANOS cells using a 63 nm process technology back in 2005. They designed the erase threshold to be positive for the single-level NAND flash memory architecture. Today, several companies are pursuing TANOS memories, including Infineon Technologies and Cypress Semiconductor. One recent development has been the use of a sealing oxide between the aluminum oxide and nitride layers (a so-called TAONOS device). This helps charge retention characteristics, but can degrade the erase times of the memory. Look for devices containing the TANOS stack in the market in the near future.

Ask the Experts

Q: What are some methods to reduce autodoping in the epitaxy?

A: One way is through reduced pressure. Researchers have studied the deposition process of epitaxial layers on Si substrates under low-pressure conditions for bipolar integrated circuits. They performed epitaxial deposition in a temperature range from 850 to 1060"C and in the pressure range from 30 to 760 torr with SiH_4 (silane) and SiH_2Cl_2 (dichlorosilane) as sources for silicon. By reducing the reaction pressure from 760 to 40 torr, the reaction temperature can be lowered about 100 to 150°C, which reduces autodoping significantly.

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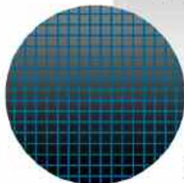

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Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

Spotlight: Failure and Yield Analysis

OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Your industry needs competent analysts to help solve these problems. ***Advanced Failure and Yield Analysis*** is a four-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a ***Do It Right the First Time*** approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

Participants learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. **The Process of Failure and Yield Analysis.**Participants learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.
2. **The Tools and Techniques.** Participants learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools, light emission, electron beam tools, optical beam tools, decapping and sample preparation, and surface science tools.
3. **Case Histories.** Participants identify how to use their knowledge through the case histories. They learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.
2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.
3. The seminar will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.
4. The seminar offers a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic technology features on semiconductor devices.
6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

One unique feature of this workshop is the video segments used to help train the students. Failure and Yield Analysis is a visual discipline. The ability to identify nuances and subtleties in images is critical to locating and understanding the defect. Many tools output video images that must be interpreted by analysts. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

1. Introduction
2. Failure Analysis Principles/Procedures
   a. Philosophy of Failure Analysis
   b. Flowcharts
3. Gathering Information
4. Package Level Testing
   a. Optical Microscopy
   b. Acoustic Microscopy
   c. X-Ray Radiography
   d. Hermetic Seal Testing
   e. Residual Gas Analysis
5. Electrical Testing
   a. Basics of Circuit Operation
   b. Curve Tracer/Parameter Analyzer Operation
   c. Quiescent Power Supply Current
   d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
   e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
   f. Automatic Test Equipment
   g. Basics of Digital Circuit Troubleshooting
   h. Basics of Analog Circuit Troubleshooting
6. Decapsulation/Backside Sample Preparation
   a. Mechanical Delidding Techniques
   b. Chemical Delidding Techniques
   c. Backside Sample Preparation Techniques
7. Die Inspection
   a. Optical Microscopy
   b. Scanning Electron Microscopy

8. Photon Emission Microscopy
    a. Mechanisms for Photon Emission
    b. Instrumentation
    c. Frontside
    d. Backside
    e. Interpretation
9. Electron Beam Tools
    a. Voltage Contrast
        i. Passive Voltage Contrast
        ii. Static Voltage Contrast
        iii. Capacitive Coupled Voltage Contrast
        iv. Introduction to Electron Beam Probing
    b. Electron Beam Induced Current
    c. Resistive Contrast Imaging
    d. Charge-Induced Voltage Alteration
10. Optical Beam Tools
    a. Optical Beam Induced Current
    b. Light-Induced Voltage Alteration
    c. Thermally-Induced Voltage Alteration
    d. Seebeck Effect Imaging
    e. Electro-optical Probing
11. Thermal Detection Techniques
    a. Infrared Thermal Imaging
    b. Liquid Crystal Hot Spot Detection
    c. Fluorescent Microthermal Imaging
12. Chemical Unlayering
    a. Wet Chemical Etching
    b. Reactive Ion Etching
    c. Parallel Polishing
13. Analytical Techniques
    a. TEM
    b. SIMS
    c. Auger
    d. ESCA/XPS
14. Focused Ion Beam Technology
    a. Physics of Operation
    b. Instrumentation
    c. Examples
    d. Gas-Assisted Etching
    e. Insulator Deposition
    f. Electrical Circuit Effects
15. Case Histories

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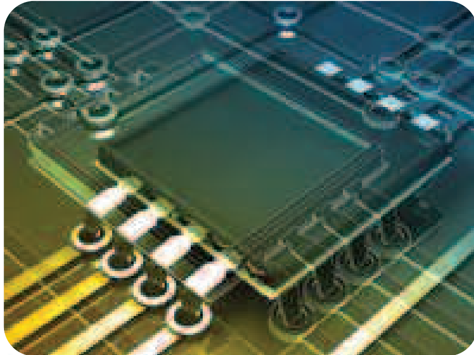
Chris Henderson, IRPS General Chair

Chris would be happy to meet with you and discuss any training needs you have. Contact him at henderson@semitracks.com during the symposium!



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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

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Upcoming Courses

(Click on each item for details)

CMOS, BiCMOS and Bipolar Process Integration
March 21 – 22, 2016 (Mon – Tue)
Albuquerque, New Mexico, USA

Failure and Yield Analysis
May 17 – 20, 2016 (Tue – Fri)
Munich, Germany

EOS, ESD and How to Differentiate
May 23 – 24, 2016 (Mon – Tue)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 30 – June 2, 2016 (Mon – Thur)
Munich, Germany

Advanced Thermal Management and Packaging Materials
June 7 – 8, 2016 (Tue – Wed)
Albuquerque, New Mexico, USA

Wafer Fab Processing
June 27 – 30, 2016 (Mon – Thur)
San Jose, California, USA

Semiconductor Reliability
July 11 – 13, 2016 (Mon – Wed)
Singapore