Issue 57 March 2014

InfoTracks

Semitracks Monthly Newsletter

Bump Processes—Part I

By Christopher Henderson

This month we begin a three-part series on the bumping process. Engineers use this process to electrically connect the die to a substrate, to a printed circuit board, and sometimes to connect one die to another. Here is the outline for this section. We begin by discussing the rationale for implementing bumping and why this approach is becoming quite common. We will then discuss the basic bumping process, describing the methods to attach a bump to the integrated circuit bond pad or pattern a copper pillar onto the pad. We will discuss redistribution layers that allow one to re-route the signals from the bond pads to a more area-efficient array. We will talk about bond over active circuitry, and other variants of this approach, like Bump On Pad, Bond Over Active Circuitry, and Bond Over Active Copper.

Probably the biggest driver moving the integrated circuit industry to bump processes for package connections is the need to fit into ever-tinier spaces. Many of today's consumer electronics have limited space for components, which precludes the use of components with lead frames. The second big driver is to maximize the amount of input/output connections for a given area. If the connections only happen at the edge of the package, then one can be very limited in the number of connections to the outside world. However, an array of connections on the bottom permits more connections. The redistribution layer and bump process helps to facilitate an array of input/output connections. The third driver is high frequencies. A

In this Issue:

SEMITRACKS, INC.
Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

bump process inherently yields a package with a lower inductance level than a package with a leadframe. This provides better signal integrity, and allows one to operate at higher frequencies.

Engineers use several bump techniques or methods in the semiconductor industry. Figure 1 shows these techniques. The oldest technique is solder bumping. This can be done with lead-tin solder balls, high-lead content solder balls, and lead-free solder balls. Pad redistribution is another technique that has been around for some time. Engineers use metals like copper, and insulators like polyimide, benzocyclobutance, and polybenzoxazole deposited on top of the wafer to re-route signals to more favorable locations. Gold Bumping is another technique used to provide standoff and connection. This uses interface materials like titanium tungsten gold, or gold chromium indium for chip-on-glass, chip-on-film, and tape carrier packages. Finally, because of the high price of gold, copper pillar bumping is proliferating. There are several types of copper pillar bumping that use eutectic, high-lead, and lead-free caps.

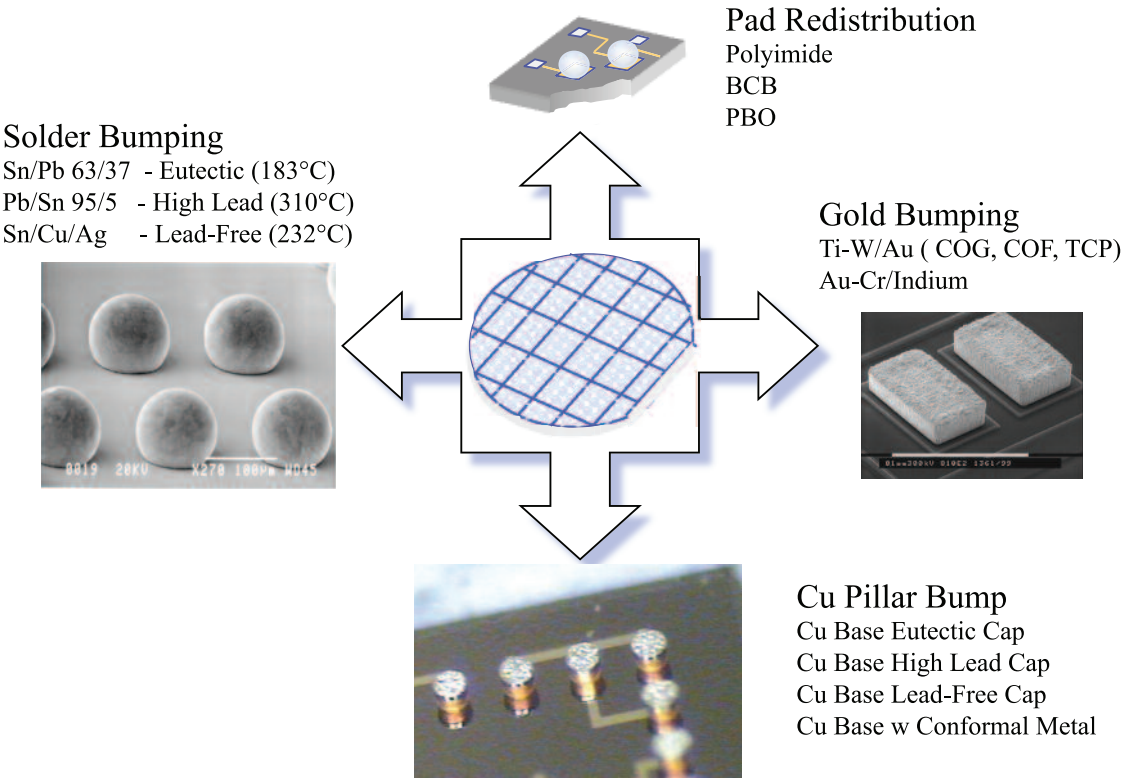


Figure 1. Common Wafer Bump Techniques.

Now let's look a little closer at the bonding techniques, specifically the solder bumps to the printed circuit board or substrate. Figure 2 helps to illustrate the two main techniques for standard flip-chip attach. The first is the solder mask defined technique. Here we use a 20 to 30 micron thick solder mask with openings defined down to the copper layer. We then place the chip face down and reflow the solder bumps. This creates a connection with a 40 to 50 micron gap between the die and the substrate. The sec-

ond is the pad defined flip-chip process. Here we have a bare copper pad on the substrate. We reflow the solder bump, which will then spread substantially, causing the standoff to collapse significantly. In this method, the gap is only 30 to 50 microns.

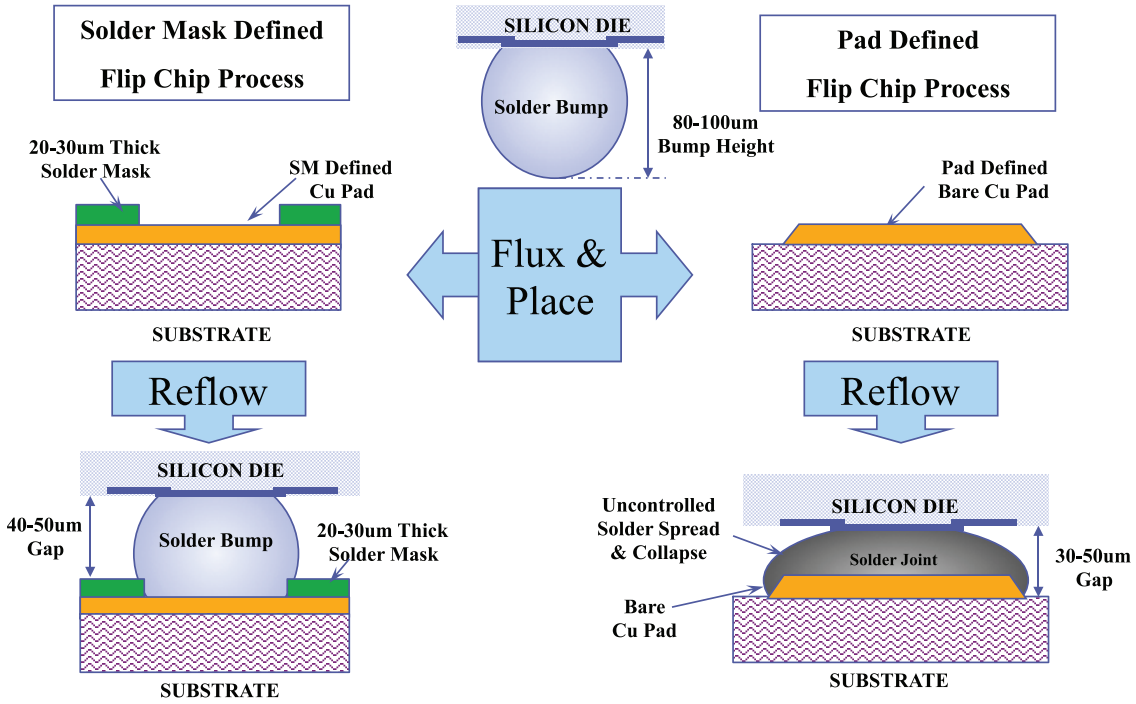


Figure 2. Standard Flip-Chip Attach Methods.

Let's continue by discussing the standard bumping process. There are two primary types. One involves using fully reflowable bumps like standard 63-37 tin-lead solder, or a lead-free solder. The other involves using rigid bumps formed from a higher melting temperature material, like a high-lead or lead-free solder. Scientists allow developed other related techniques like plated bumps, screen-print bumps and solder ball preforms. The pitch, or distance between the centers of adjacent pads, varies depending on the technique. The diagram and image below show the basic solder bumping process (see Figure 3).

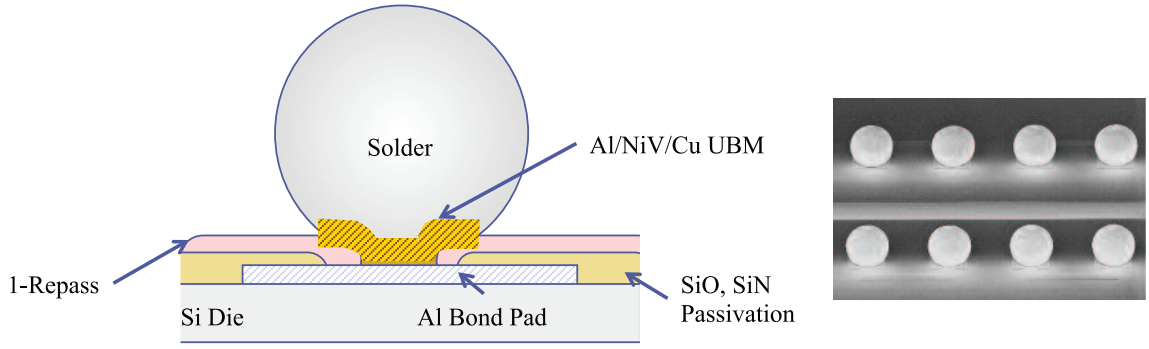


Figure 3. Standard Solder Bumping Process.

This sequence of steps (Figure 4) shows how one follows the standard solder bump process. This works for either a solder paste approach, or a solder ball placement approach. After wafer cleaning, one sputters the appropriate under bump metals on top of the chip and patterns these materials such that they only remain on the pads. After etching the UBM metals and removing the resist, one can place the solder ball or add the solder paste and reflow it to create the solder bump.

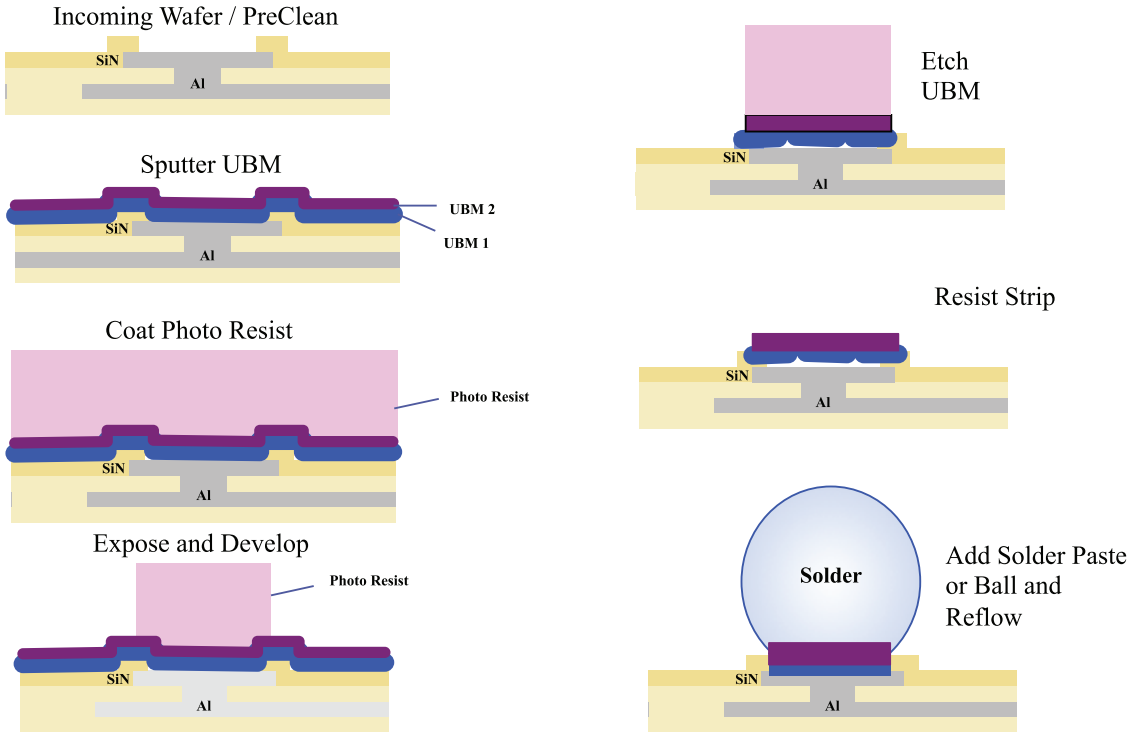


Figure 4. The Solder Paste/Ball Drop Bump Process.

This sequence of steps below (Figure 5) shows how one follows a plated solder bump process. After wafer cleaning, one sputters titanium and then copper on top of the chip and patterns these materials such that they only remain on the pads. After etching the UBM metals and removing the resist, one can then expose and develop an area above the bond pads and then electro-deposit the solder. Once the solder is deposited, one can remove the resist and reflow the solder to create the solder bump.

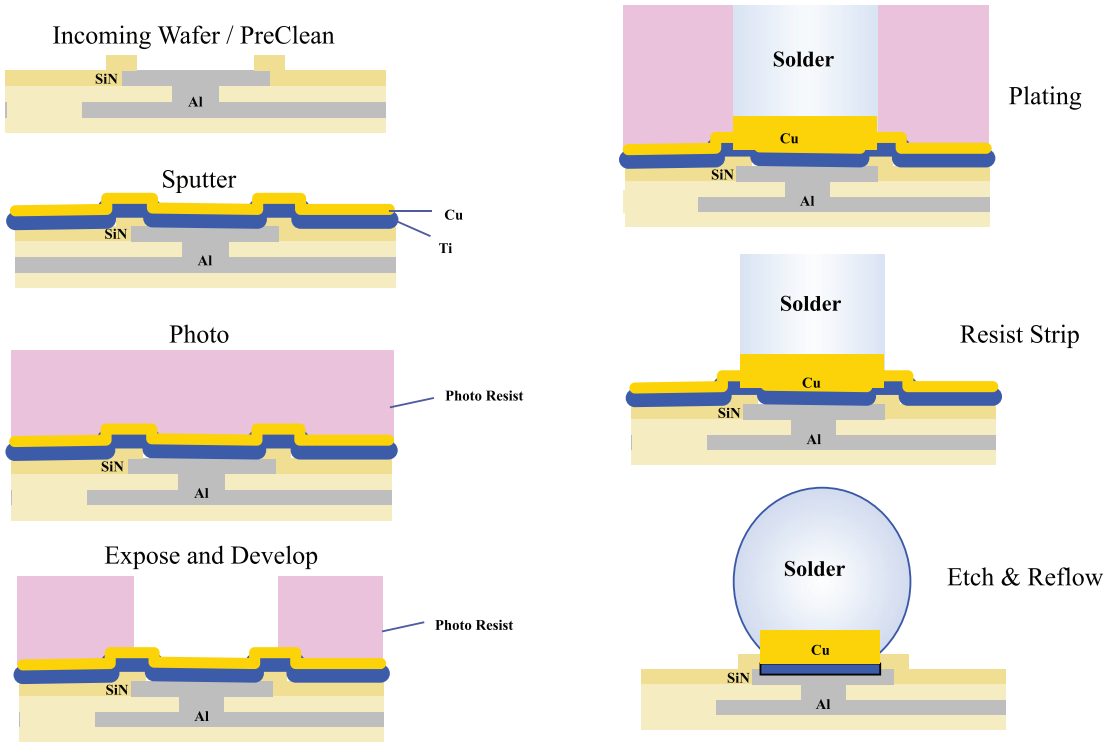


Figure 5. Plated Solder Bump Process.

An important consideration is the size and shape of the solder bump. With the drive towards smaller package footprints, engineers have been scaling the bumps to smaller pitches. The maximum solder bump height is typically 50% of the pitch when using standard round bumps. If one chooses plated bumps, then the pitch can be somewhat tighter due to their improved size and height consistency. However, screen print bumps are limited to the capabilities of the screen print equipment and processes. Another important aspect of the bump is the method by which one connects the bump to the pad. A solder bump does not by itself make a reliable connection to the aluminum or copper bond pad. To make a reliable connection, we need a metal system that guarantees good adhesion between the solder bump and the pad, and prevents material migration and degradation. We refer to this metal system as an under bump metallization or UBM layer. Common UBM materials include titanium-tungsten-gold for gold bumping, titanium-tungsten-copper for lead-free and lead-tin solder bumps, and titanium-copper for copper pillar bumps.

Next month, we'll continue our discussion on the bumping process.

Technical Tidbit

Lithography Alignment

Alignment during lithography is a critical activity. Any type of misalignment can lead to non-functional circuits. In order to print the features on the circuit, the mask must be aligned to the wafer features. How do engineers do this? They use alignment marks printed on the wafer from the previous mask step or steps. The image below (Figure 1) shows an example of alignment marks. Quite often, alignment marks consist of box-like structures with a cross internal to the box. The criticality of the alignment can be defined by the width of the cross in the box. A narrow cross indicates a more critical or closely aligned step. There are many types of alignment errors. The list includes mask errors, stage errors, and wafer chucking errors. These alignment errors are straightforward to understand and can usually be corrected through proper calibration and procedures. Another type of alignment error can occur from lens distortion or magnification. These alignment errors are straightforward to understand and can usually be corrected through proper calibration and procedures. Another type of alignment error can occur from lens distortion or magnification. This type of error can be more severe, requiring one to re-polish or even replace the lens. Some alignment problems result from wafer processing. Thermal processes and the use of stressed films can produce a bow in the wafer, which leads to alignment issues. An asymmetrical resist coating can lead to depth of focus issues or refraction problems that impair alignment. Chemical mechanical polishing can lead to a non-flat wafer surface which affects alignment. Overlay metrology errors can also impact alignment.

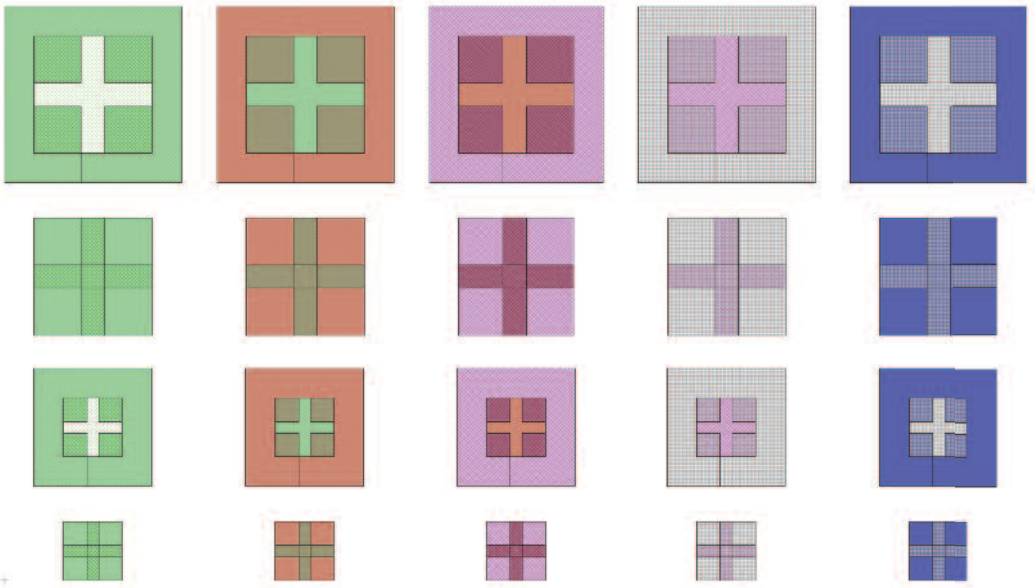


Figure 1. Example of alignment marks.

Here are some examples of overlay errors (see Figure 2). The blue lines represent the ideal grid and the red lines show the actual chip positions. Here we show eight different types.

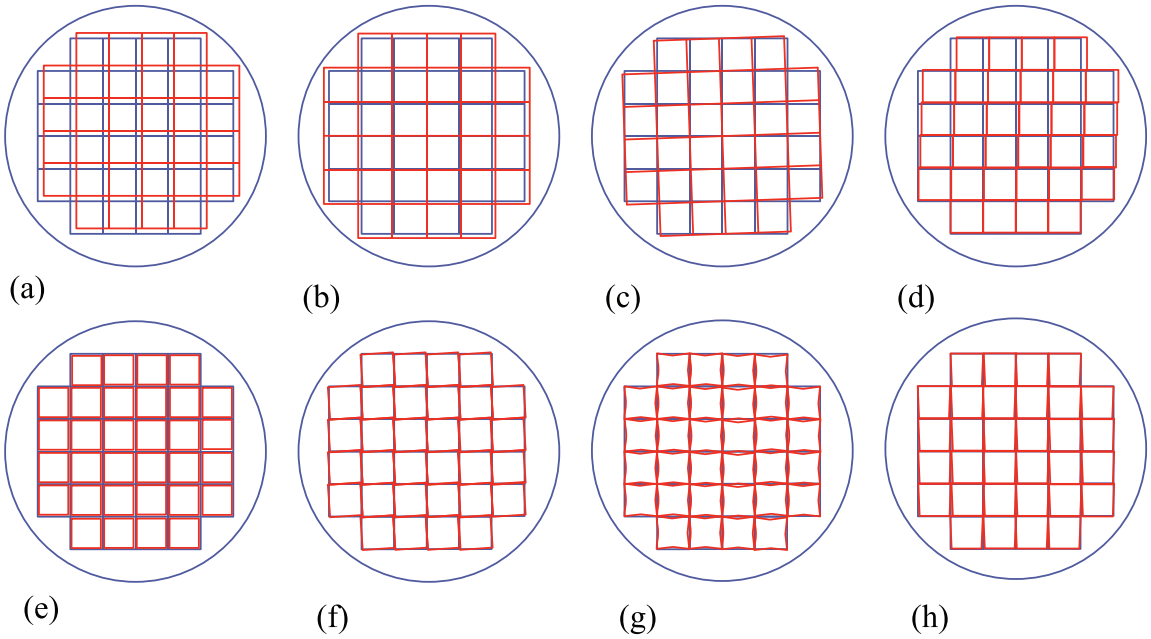


Figure 2. Examples of overlay errors: (a) global offset, (b) global scaling, (c) global rotation, (d) orthogonality, (e) field magnification, (f) field rotation, (g) distortion, (h) trapezoid.

Ask the Experts

Q: What is the Kooi effect?

A: The Kooi effect is also known as the white ribbons effect. It was first documented in the mid-1970s by Else Kooi, who worked at Philips Research in the Netherlands. It is the formation of a nitrogen-rich layer near the gate interface. Water oxidizes the silicon nitride mask layer, creating ammonia (NH_3). The ammonia can then diffuse to the silicon interface where it forms a silicon nitride or nitrogen-rich oxide layer. This can interfere with gate oxide growth, making the gate oxide too thin in regions where the nitrogen-rich layer exists.

Spotlight: Semiconductor Packaging Design, Simulation, And Technology

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The industry is also pushing to use semiconductor devices in an increasing array of applications. To accomplish this, the industry is also driving prices down. This has created a number of challenges related to the packaging of these components. ***Semiconductor Packaging Design*** is a three-day course that offers detailed instruction on the design and modeling of semiconductor packages. We place special emphasis on package interactions with the die. This course is a must for every manager, engineer, and technician working in semiconductor packaging, using semiconductor components in high performance applications or non-standard packaging configurations, or supplying packaging tools to the industry.

By focusing on the fundamentals of packaging design and modeling, participants will learn why advances in the industry are occurring along certain lines and not others. Our instructors work hard to explain semiconductor packaging without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor packaging. This skill-building series is divided into four segments:

1. **Packaging Technology Overview.** Participants learn the evolution of packaging technology. They learn how form factor and performance is driving semiconductor packaging for today's designs.
2. **Packaging Design Overview.** Participants learn the fundamentals of packaging design. They learn why modeling has become critical to semiconductor packaging for today's designs.
3. **Dealing with Sub-Contractors.** Sub-contractors do much of the packaging today. Participants learn how they work and how to deal with them.
4. **Modeling Semiconductor Packages.** Participants learn about the software used for modeling a variety of aspects of semiconductor packaging. They see a number of examples using current modeling tools used by Package Design experts.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of semiconductor packaging design and its technical issues.
2. Participants will understand the basic concepts behind the evolution of semiconductor packages.
3. The seminar will identify the key issues related to the continued growth of the semiconductor industry. This includes the need for high power dissipation, and designs that can mitigate the increasing fragility of the die because of low-k dielectrics.
4. The seminar offers a wide variety of sample modeling problems that participants work in class to help

them gain knowledge of the fundamentals of packaging modeling.
5. Participants will be able to identify basic and advanced principles for mechanical stress and thermal diffusion.
6. Participants will understand how package reliability, power consumption and device performance are interrelated.
7. Participants will be able to make decisions about how to evaluate sub-contractors for new packaging designs and technologies.
8. Participants will also be introduced to future package formats.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor packaging and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field.

COURSE OUTLINE

1. Package Technology
   a. Global Business Trends
   b. IC Technology and Implications on Packaging
   c. International Technology Roadmap for Semiconductors: What is it? What it says about Device Packaging?
2. Package Design
   a. CAD software
   b. Design Check Rules
   c. Best Practices
3. Packaging Materials
   a. Material science
   b. The Role of Polymers
   c. Failure Mechanisms
4. Working with Package Subcontractors
   a. Who are they?
   b. Building the relationship
   c. What to expect
5. Package Modeling
   a. Thermomechanical Modeling
   b. Thermal Modeling
   c. Process Modeling
   d. Package Reliability Simulations

6. Advanced & Future Packages
   a. MEMS, Sensors, & Actuators
   b. 3D Wafer Level Packages
   c. LEDs, Solar Module Packages, etc.

Semitracks will be present at the

2014 International Reliability Physics Symposium (IRPS)

June 1 – 5

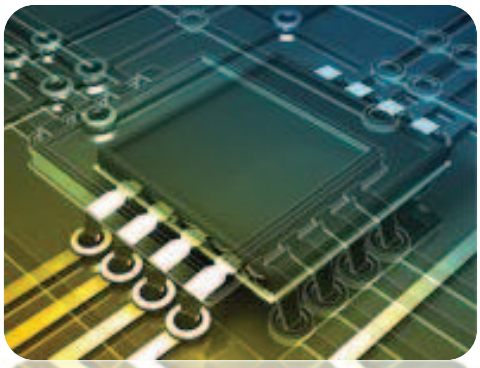
Hilton Waikoloa Village • Hawaii

Stop by and see us!

For more information on IRPS, please go to www.irps.org.

Please feel free to contact us to set up an appointment while you are there!

http://www.irps.org



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

~

For more information on Semitracks online training or public courses, visit our web site!

http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

CMOS, BICMOS and Bipolar Process Integraion
March 25 – 26, 2014 (Tue – Wed)
Austin, Texas, USA

Semiconductor Package Design, Simulation, and Technology
April 7 – 9, 2014 (Mon – Wed)
San Jose, California

Product Qualification
April 15 – 16, 2014 (Tue – Wed)
San Jose, California

Failure and Yield Analysis
May 5 – 8, 2014 (Mon – Thur)
Munich, Germany

MEMS Technology
May 12 – 13, 2014 (Mon – Tues)
Munich, Germany

Semiconductor Reliability
May 12 – 14, 2014 (Mon – Wed)
Munich, Germany

Product Qualification
May 15 – 16, 2014 (Thur – Fri)
Munich, Germany