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InfoTracks

Semitracks Monthly Newsletter

Ion Implantation Part I – Equipment

By Christopher Henderson

In this article we'll spend our time discussing the major subsystems that are part of an ion implanter. For more details, the reader is encouraged to read Microchip Manufacturing, and Silicon Processing Volumes 1 and 4 by Stan Wolf, and Semiconductor Manufacturing Technology by Robert Doering and Yoshio Nishi.

The major components of an ion implanter are listed here. They include:

- Ion Generation and Extraction
- Mass Analysis
- Acceleration
- Scanning
- Dose Measurement
- Charge Control
- Wafer Handling
- High Vacuum
- Monitoring and Control

We will cover each of the elements in more detail in the following slides.

In this Issue:

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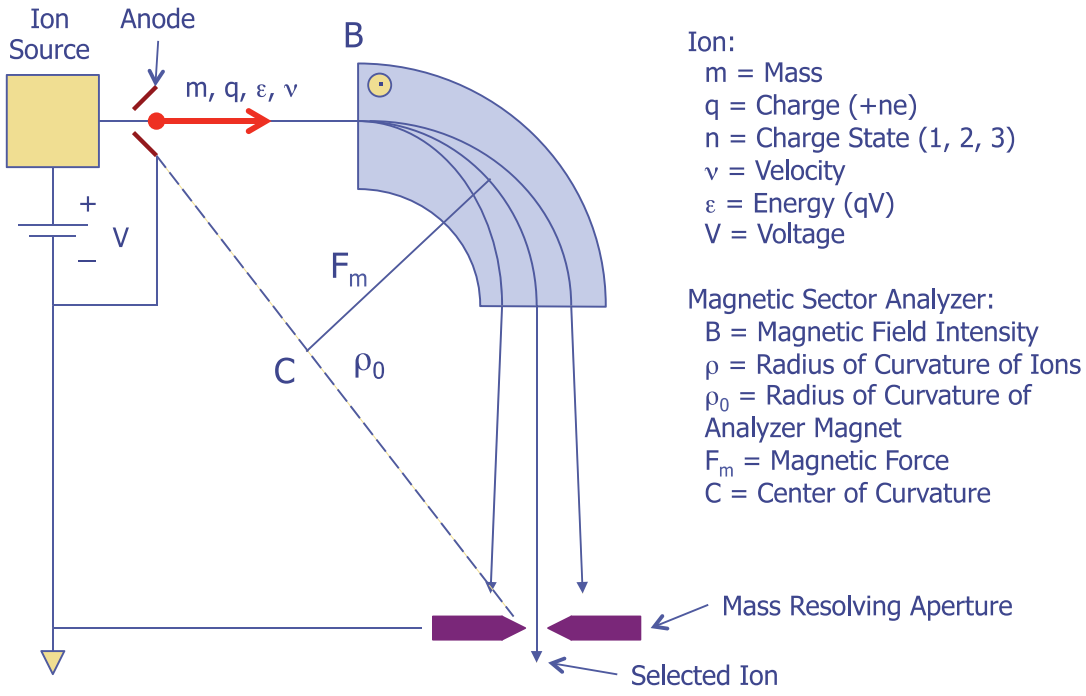
Figure 1. Model of a typical high current implanter (image courtesy Axcelis).

Let's begin with ion generation and extraction. An ion implanter requires a source of ions to implant into the wafer. This is typically done through a gas field ion source. One can use a low-pressure gas, or one can create a gas by heating solid materials. Some common gases include boron trifluoride and phosphine, while materials like arsenic and antimony oxide can be heated to create a gas. The ion source then ionizes the gas, creating plasma, which contains the dopant ions of interest. An extraction electrode uses an electric field to extract ions and focus the ion beam. The extraction energy of the beam is given by this equation, where q is the quanta of charge, which include ion charge state, and the extraction voltage in kilovolts.

The extraction field extracts all ion types, so it is then necessary to select the ion of interest. We do this using mass analysis. Mass analysis is the process of separating elements or isotopes by mass using an analysis magnet. This will depend on the mass-to-charge ratio. By placing an aperture at correct position at the end of the analysis magnet, one can choose the species of interest. We can identify the species of interest by using this basic equation:

$$r_0 = \left(\frac{143.95}{H}\right)\left(\frac{mV_e}{q}\right)^{1/2}$$

where r sub zero is the radius of curvature of the ion going through the analysis magnet, H is the magnetic field, m is the ion mass number, V sub e is the extraction voltage, and q is the ion charge state.



Mass-analyzer of an ion implanter

Figure 2. Schematic of the mass analyzer in an ion implanter.

Figure 2 shows the basic configuration of the mass analyzer. As the ion leaves the ion source and accelerates toward the anode, it gains a certain energy and velocity based on its mass, charge, and the accelerating voltage. The ion is steered by the magnetic force F sub m through the magnet to the mass-resolving aperture. The aperture can be moved to select the ion mass and charge of interest.

After emerging from the magnetic analyzer, ions can be accelerated or decelerated to the appropriate implant energy. This is also known as post acceleration. The total ion energy can be given as this equation,

$$E_t = q\left(V_e + V_a\right)$$

where q is the ion charge state, V sub e is the extraction voltage between the ion source and the anode, and V sub a is the accelerating voltage, or decelerating voltage on the electrodes.

The next major subsystem is the scanning elements. Once the appropriate ion has been selected, the beam must be rastered across the wafer surface. This needs to be done with a uniform density and a constant angle of incidence to give a parallel scan. This is important so that the channeling effects are consistent across the wafer. The ion beam can be rastered as either a spot beam or as a ribbon beam. A ribbon beam tends to work better for smaller technologies where beam spreading due to charging is a problem. The beam can be further shaped by electrostatic and/or electromagnetic lens. For instance, one might prefer an elliptical shape or a non-Gaussian beam for certain designs. The scanning can also be used to define the implant angle. Zero degrees and seven degrees are popular implant angles. For instance, 7° is used because it limits ion channeling significantly. Another popular technique is to use large angles

between 20 and 60°C for lateral asymmetrical channel and halo implants.

Ion implantation can be done with electrostatics, electromagnetics, mechanical scan, or a mixture. In electrostatic or electromagnetic scanning, the wafer is held stationary and the beam is scanned in the x- and y-axes. This is typically used in a single wafer process. In contrast, mechanical scan is used for batch wafer processing. The beam is fixed and the wafers are scanned through the beam in the x- and y-axes. There are also hybrid-scan systems that use electrostatic or magnetic scans in one axis and mechanical scans for the other axis. In a ribbon scan system, the ribbon beam is set to be greater than the wafer diameter and the wafer is scanned mechanically through the beam in the other axis. There are also newer techniques like radial scanning used today as well.

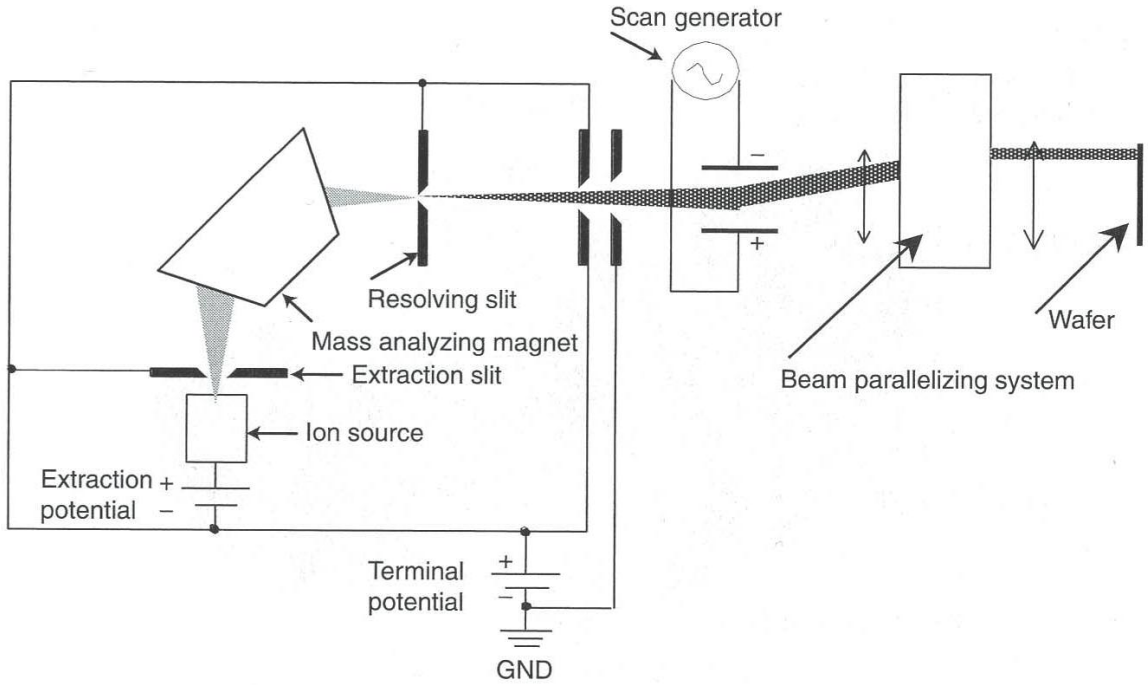


Figure 3. Electrostatic scanning.

Figure 3 shows a typical configuration for electrostatic scanning. After the beam emerges from the mass analyzing magnetic and resolving slit, the beam is focused and then passed through a scan generator. The beam is then run through a beam parallelizing system that creates a parallel beam for the wafer surface, resulting in a more uniform implant.

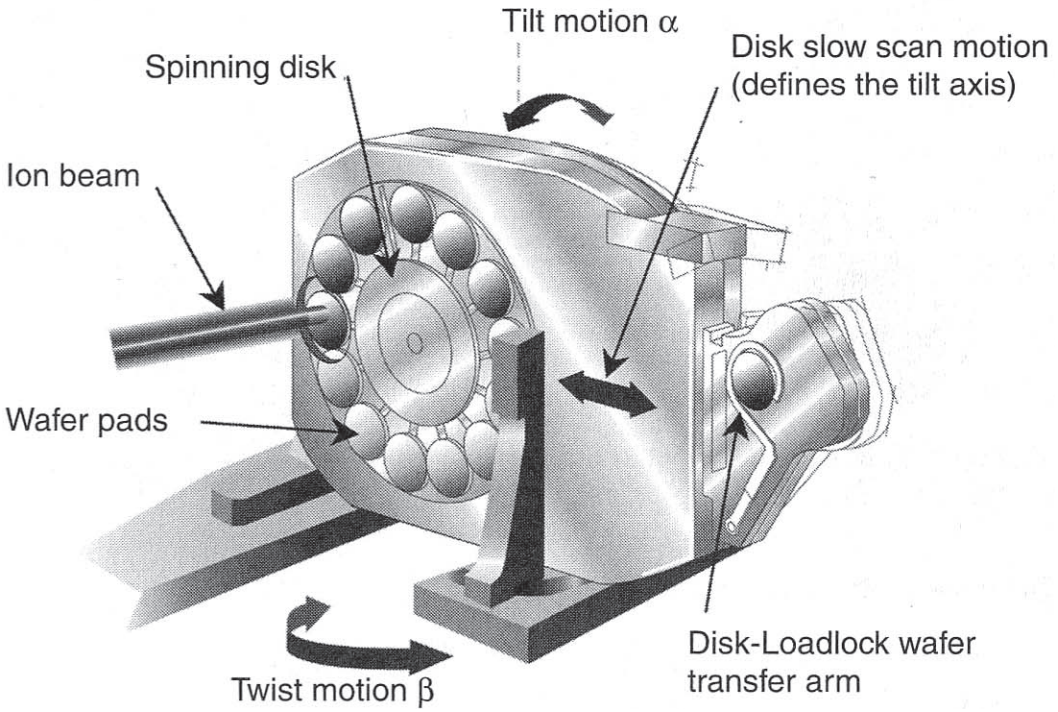


Figure 4. Spinning disk arrangement.

Figure 4 shows an example of a spinning disk arrangement for mechanical scanning. The wafers are placed on the pads and then rotated through the beam. Simultaneously, the disk moves back and forth to produce an additional axis of scan. The disk can also be tilted to produce an angled implant.

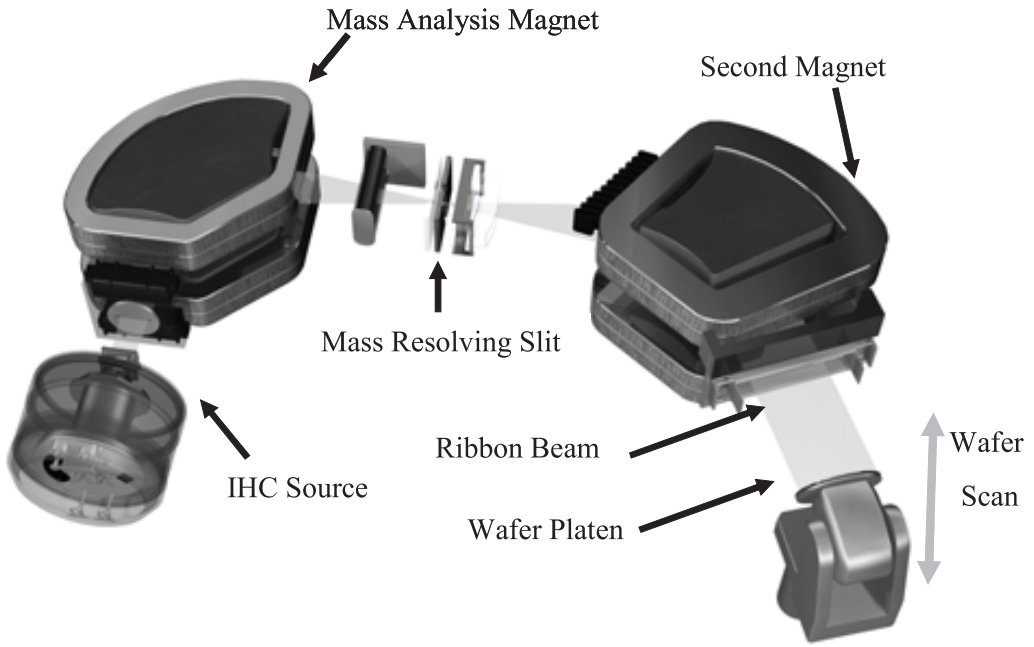


Figure 5. Drawing showing ribbon beam configuration.

Scanning can also be done through magnets. Figure 5 shows an example of a ribbon beam that is scanned using a magnet. The wafer holder shown at the bottom right provides a second axis of scan.

Dose measurement is usually done with a Faraday cup. A Faraday cup is a structure that captures the incoming electrons or ions and bleeds the charge off through a grounded plate to a current meter. One can integrate the current over time to compute the dose. The dose ϕ is given by this equation

$$\varphi = \frac{It}{qeA}$$

and is a function of the beam current, implant time, ion state, charge, and implant area.

Another important system in the ion implanter is the charge control system. This system minimizes charge build-up on the wafers, which can lead to ESD damage on sensitive gates. Excess charge can also lead to charge spreading, which creates non-uniform lateral and vertical doping profiles as well as dosimetry errors. Charge control is typically accomplished using a plasma tube, which creates numerous low energy electrons or ions in front of the wafers that neutralize the doping species.

Another important component of the system is wafer handling. Wafers are transferred from Front Opening Unified Pods, sometimes called FOUPS by industry personnel, into the implanter, where the machine performs the implant, and back out. Precision, repeatability, and minimal contamination generation are critical for this process. This photograph shows the interface for the FOUPS or cassettes on the front of the machine.

Another critical system is the high vacuum system within the implanter. It is important to minimize collisions between air molecules and the ions, so engineers maintain the vacuum at better than 10-7 – 10-8 torr to prevent these collisions. This also helps to minimize charge neutralization that can occur as a result of these collisions.

Finally, monitoring and control is a big component of today's ion implanters. Computer systems within the implanter monitor and control all aspects of the operation, including the user interface, recipe management, data management, preventive maintenance schedules and error logging. This is all essential for good process control within the fab.

Next month, we'll cover ion implantation process issues.

Technical Tidbit

Transene Etch

Some of you might have heard of the term Transene etch and wondered exactly what it was. Transene is actually a company based in Danvers, Massachusetts, that manufactures a variety of chemical etches (www.transene.com). In the semiconductor industry, labs make use of several of their etchants.

One of the more common etchants used in failure analysis work is their copper etch APS-100. APS 100 from Transene is a commercial mix of 15 – 20% $(NH_4)_2S_2O_8 + H_2O$. This reaction of ammonium persulfate and copper follows this equation:

$$Cu(s) + (NH_4)_2S_2O_{8(aq)} \rightarrow CuSO_{4(aq)} + (NH_4)_2SO_{4(aq)}.$$

It etches copper at a rate of approximately 80Å/sec at 40°C. This mixture works well to remove copper layers on an integrated circuit. It does not have the control necessary for removal during the fabrication process, but it does do a good job of clearing an area for inspection of lower layers. You can also use photoresist as a mask for the etchant.

Another common etchant used in FA is their aluminum etchant Type A. Type A is a mixture of 80% H_3PO_4 + 5% HNO_3 +5%CH_3COOH + 10% H_2O (phosphoric acid + nitric acid + acetic acid + water). It etches aluminum at a rate of approximately 80Å/sec at 40°C. You can also use negative photoresist as a mask for the etchant.

Industry Insights

The International Electron Devices Meeting (IEDM) recently occurred in Washington, DC. While IEDM showcases new technology and devices, I am always amazed at the variety of new technologies and the extent of the developments. While most of us are aware that Intel will incorporate FinFETs into the Ivy Bridge processor that will be sold next year, there are a number of developments in the pipeline to "hopefully" keep Moore's Law and scaling alive. Some of the more important developments include the incorporation of nanowires, III-V materials in the MOSFET channel, and Tunnel FETs.

IBM showed considerable progress on nanowire technology, with some simple working circuits like ring oscillators. Nanowires are important in that they represent the future for better electrostatic control of the channel. IBM has developed a top-down process for placing the wires through electron beam lithography, using hydrogen annealing to improve the sidewalls, and oxidation to thin the nanowires. While silicon nanowires are not going to be in production in the near future, there is a potential path forward. The biggest hurdle still to come will be developing a standard lithography process. E-beam lithography is not a process currently compatible with high-volume manufacturing.

Notre Dame showed progress with Tunnel FET or TFET devices. These structures can deliver a steeper subthreshold slope, so these devices will turn off better, with lower leakage. Tunnel FETs can be designed to provide oblique tunneling or in-line tunneling. In-line tunneling is preferable to create a steep slope device. These devices require considerable materials deposition development and bandgap engineering. They also operate at very low voltages, making them hard to integrate with traditional CMOS devices. However, the developments in this field are substantial.

The University of Tokyo showed developments in III-V and germanium channel materials. This work is probably the closest to becoming a reality in CMOS devices. The big challenge with these materials is the

lattice mismatch. This calls for buffer layers to reduce damage from TCE mismatch and lattice mismatch. These materials also require considerable bandgap engineering. Interface traps and Fermi-Level pinning are also big concerns. The leading candidate right now is to use InGaAs in the NMOS channel and Ge in the PMOS channel. I would speculate that this technology will be the first to make it into mainstream CMOS technology. It will be particularly useful in CMOS RF applications.

There were a number of other interesting developments, including important advancements in Phase Change Memory, Racetrack Memory, Silicon-Carbide, and Gallium-Nitride devices. There were also a number of papers on carbon nanotubes. Scientists have made considerable progress in aligning deposition and creating contacts.

Whenever I get concerned that we're running out of steam with Moore's Law, IEDM always provides interesting insights into how we might move forward. IEDM reminds me to be optimistic. There are smart engineers and scientists who will continue to move our industry forward.

Ask the Experts

Q: I need to distinguish unambiguously between LOCOS and STI, particularly in the case when you can not compare between them, but need to know which type. The "birds beak" effect is not very clear in most cases. Please, advice what other ways to certainly identify each of the types. I will appreciate your thoughts.

A: A couple of thoughts come to mind. Usually the trench for STI will be etched deeper into the silicon. Remember that LOCOS consumes silicon, so about 45% of the oxide grows down into the silicon while the upper 55% will be above the original surface. The trench sidewalls will be steeper than the LOCOS sidewalls. Of course, you'll need to cross-section the device to see these items. For a top-down assessment you might be able to determine this optically, but it will be difficult on a modern technology. Because the oxide extends above the surface, features on the oxide may not be in focus at the same time as features directly on the silicon. You could possibly see this effect on the polysilicon while viewing at high magnification.

A reader wrote in concerning last month's "Ask the Experts" column and brought up a good point regarding interpretation of the I-V curve. Here is his response:

I think you missed the obvious on your answer in the "Ask the Experts" question. It could be a lot of things, but if it was a CMOS device, then one thing that should be noted is that a CMOS inverter always shows this effect. The NMOS and PMOS transistors have their gates tied together in the CMOS inverter. If the common gate starts at zero and is ramped up, initially, the PMOS transistor is on but the NMOS is off showing little current through the two transistors in the inverter. As the gate voltage increases, the NMOS transistor turns on and current is then pulled between VCC and GND. Eventually, the PMOS transistor will turn off reducing the power supply current again. Thus, it is a common occurrence to see this "middle" area with higher current. The actual circuit analysis will be much more involved, so the full answer can not be given without knowledge of the circuit, but high current with the voltage between the NMOS Vt and the PMOS Vt is not unusual.

Spotlight on our Courses: Copper Wire Bonding Technology And Challenges

Our Copper Wire Bonding Course will be offered in Munich, Germany, May 7 – 8 this year. Here is more information about the course. If there is sufficient demand, we'll also offer it in the US later this year. If you're interested in having this course as an in-house course for your staff, please feel free to contact us at (505) 858-9813, or at info@semitracks.com.

OVERVIEW

The drive to reduce costs in semiconductor and integrated circuits remains a key challenge for the industry. For example, many of today's ICs use expensive gold wiring. As a result, the industry is pushing to use copper wires and copper pillar bumping in an increasing array of applications. This has created a number of challenges related to the bonding and packaging of these components. Copper Wire Bonding Technology and Challenges is a 2-day course that offers detailed instruction on the technology issues associated with today's semiconductor packages. We place special emphasis on current issues like bond formation, bumping, and tools for package analysis. This course is a must for every manager, engineer, and technician working in semiconductor packaging, using semiconductor components in high performance applications or non-standard packaging configurations, or supplying packaging tools to the industry.

By focusing on current issues in packaging technology, participants will learn why advances in the industry are occurring along certain lines and not others. Our instructors work hard to explain semiconductor packaging without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor packaging. This skill-building series is divided into four segments:

1. **Basic Semiconductor Wire Bonding Metallurgy:** Participants will study the phase diagrams that are most useful to IC packaging and learn about basic metallurgy topics such as melting, solidification, intermetallic compounds, oxidation, corrosion and welding.
2. **Important Copper Alloy Systems in IC Packaging:** The course presents metallurgical principles with selected alloy and materials systems that are key to the understanding and analysis of semiconductor (IC) packaging assembly and reliability.
3. **IC Mounting and Bonding:** Participants will learn about alloy mounts and Ag-filled die attach. Additionally, they'll learn about wire bonding, flip-chip soldering, and package mounting. Phase diagrams are used as a basis for examining what solid solutions, phases, and intermetallic compounds (IMC) should be expected in an assembled or PC-board mounted IC package, and where the phases should form in a well-built system. Oxidation/reduction potentials are the first steps toward resolving corrosion resistance issues, either in package design or failure analysis. Since assembly techniques join metals by soldering or thermo-compression/thermo-sonic methods, the behavior of melting and solidification and the formation of solid solutions and IMCs, as read from the phase diagrams, is presented as an important predictive and diagnostic tool.
4. **Reliability and Environmental Tests:** The last part of the class brings together the basic principles and selected alloy systems to analyze the results of reliability testing, interpret the observed failure modes to identify root causes, and predict behavior for materials or process changes implemented to

lower costs and/or improve reliability. The course covers moisture tests, thermomechanical tests, electromigration, and failure analysis methodology.

COURSE OBJECTIVES

1. At the end of the course, participants will know how to read and interpret phase diagrams for melting and solidification behavior.
2. They will also know the compositions of the solids and intermetallic compounds that should form.
3. Participants should be able to predict and identify potential corrosion products from environmental testing and field failures. They should also know how to interpret failure analysis results.
4. Finally, participants will gain methods to apply these principles to process and material changes to lower cost and produce increased reliability for IC packaging.
5. Participants will be able to make decisions about how to construct and evaluate new packaging designs and technologies.
6. The participant will see several case studies associated with copper wire bonding.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor packaging and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is application. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field.

COURSE OUTLINE

I. Basics of Al, Au, and Cu
   a. Melting & Solidification
   b. Phase Diagrams & Intermetallic Compounds
   c. Oxidation & Corrosion
   d. Diffusion & Welding
   e. Binary/Ternary Phase Diagrams and How to Interpret

II. Important Cu Alloy Systems (Intermetallic Growth Rates & Phases)
   a. Al-Au
   b. Al-Cu
   c. Cu-Sn
   d. Sn-Ag-Cu
   e. Pd-Cu on Al

III. IC Bonding
   a. Free Air Ball Formation
   b. Wire Bonding
      i. Loop Design
      ii. Loop Parameters

c. Flip-Chip Soldering
    i. Free air balls
d. Cu-Pillar Bump
e. Bond Pad Issues
    i. Metal Layers
ii. Via Design

IV. Package Mounting – Soldering
a. Pad & Lead Cleanliness
    i. Surface Contamination Test methods
b. Pad & Lead Finishes: IMC formation
    i. Cu/Cu
    ii. Cu/Ni
c. Interactions with molding compound

V. Reliability and Environmental Tests
a. FIT rates
b. Arrhenius Equation
c. Moisture tests
    i. HAST Testing
        1. Copper Oxidation
        2. Degradation
    ii. Voltage-Biased Tests
    iii. Autoclave
d. Thermomechanical tests
    i. Temperature Cycling
    ii. Flex Tests/Drop Tests
e. Mechanical and Electrical Tests
f. Electromigration
g. Special Cases: Failure Analysis Methodology
    i. Deprocessing Chips with Cu wires/Cu pillars
    ii. Identification of corrosion failures
    iii. Identification of oxidation failures
h. Test Vehicles/Test Chips

VI. Thermomechanical Stresses
a. Solder Bump Stress
b. Solder Joint Stress
c. Die Corner Stress
d. Low-K Dielectrics

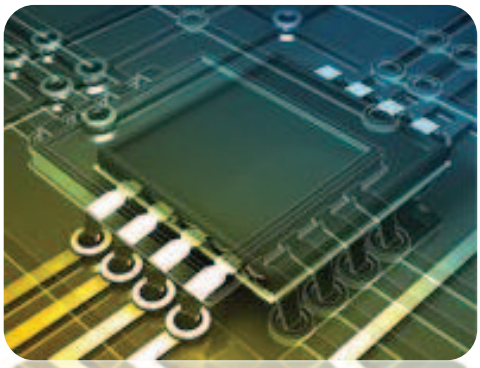
VII. Case Studies

Semitracks will appear at the

International Reliability Physics Symposium
April 15 – 19
Anaheim, California

Stop by and see us!

http://www.irps.org



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our web site!

http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Failure and Yield Analysis
April 9 – 11, 2012 (Tues. – Fri.)
Singapore

EOS, ESD and How to Differentiate
April 12 – 13, 2012 (Thurs. – Fri.)
Malaysia

ESD Design and Technology
April 22 – 24, 2012 (Sun. – Tues.)
Tel Aviv, Israel

Failure and Yield Analysis
April 22 – 25, 2012 (Sun. – Wed.)
Tel Aviv, Israel

Failure and Yield Analysis
May 7 – 10, 2012 (Mon. – Thurs.)
Munich, Germany

Copper Wire Bonding
May 7 – 8, 2012 (Mon. – Tues.)
Munich, Germany

Semiconductor Reliability
May 14 – 16, 2012 (Mon. – Wed.)
Munich, Germany

Wafer Fab Processing
June 5, 2012
San Jose, CA, USA

Reliability Characterization and Challenges
June 11, 2012
San Francisco, CA, USA