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INFOTRACKS

YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Semiconductor Cleanroom Technology

By Christopher Henderson

In this month's Feature Article, we continue our discussion of Semiconductor Cleanroom Technology. In this article, we will cover some additional considerations concerning Heating, Ventilation, and Air Conditioning, or HVAC, as it applies to Cleanroom Technology. As we mentioned last month, Semiconductor Cleanrooms require tightly controlled temperature and humidity levels, so the air conditioning requirements are quite stringent. We pick up this topic by starting with a discussion of laminar flow air systems.

In Figure 1, a class-100 room is shown with 100% High Efficiency Particulate Air, or HEPA, ceiling coverage. The make-up air handler, or MAH, is a fresh air unit that provides the room pressurization and is designed for a latent and sensible load of outside air. This unit feeds to two Recirculation Air Handlers, or RAH, that supply air into the cleanroom, like we show in Figure 1. The RAH are usually designed primarily for the sensible heat load generated indoors from the process equipment and occupancy.

WHAT'S INSIDE?

Want to take control of your learning? See page 10

Upcoming Courses:

- Product Qualification Overview
- Advanced CMOS/FinFET Fabrication
- IC Packaging Design and Modeling

See page 14 for more details

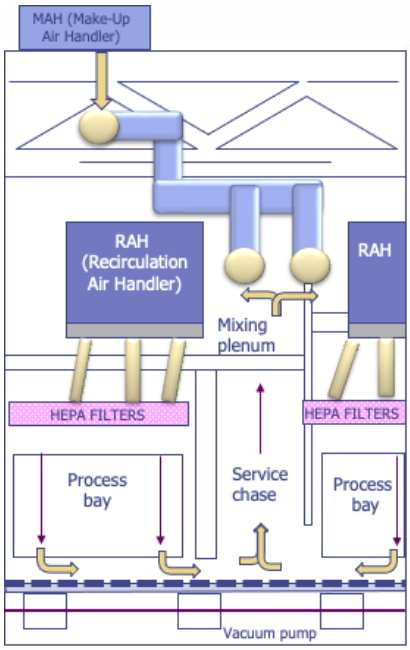

Figure 1- Cross section diagram of a Class 100 Clean Room with HVAC components identified.

The key characteristics of unidirectional air flow system are as follows:

1. Unidirectional airflow systems are designed for an air velocity of 60 to 90 feet per minute. This air velocity is sufficient to keep the contaminants directed downwards and remove particles before they settle onto surfaces.
2. For wider rooms, greater than 4.8 meters wide, it is best to provide raised floor returns so that the airflow tends to remain parallel (or within 180 degrees of parallel). Where the clean space is fairly narrow, on the order of 4.2 to 4.8 meters, from wall to wall, the raised floor can be eliminated in favor of low sidewall return grills. The air will move vertically downward to within 0.6 to 0.9 meters of the floor before splitting and moving toward the sidewall returns.
3. Unidirectional, or Laminar, airflow tends to become turbulent if it encounters obstacles such as people, process equipment and workbenches. Placing these obstructions in a manner that prevents dead air spaces from developing will minimize turbulence. Use of workstations with perforated tabletops will allow the air to pass through them uninterrupted. Equipment should also be raised on a platform (plinth) where possible to allow free air flows beneath it.
4. In a unidirectional arrangement, HEPA filter banks must be "pinhole" tight and checked for any pinhole leaks in the media, sealants, frame gaskets, and supporting frames.
5. In some designs, the supply air can be projected upwards from the floor void and drawn into a ceiling void. This arrangement is preferred in applications where the localized hardware or equipment has high heat dissipation. The conventional supply airflow from ceiling may not be directional enough to cool the equipment thus resulting in hot spots.

Positive pressurization of the sensitive areas is an effective means of controlling contaminant infiltration through any minor breaches in the room perimeter. Positive pressurization is achieved through supplying higher outside air than what is exhausted from the space. However, it is extremely important that air introduced for pressurization is adequately filtered and conditioned. Positive air pressure means the cleanroom is "pumped up" with more filtered air than the surrounding space outside the cleanroom(s). Generally, a value of 0.05 inch water column pressure, which is equivalent to12 Pascals, is recommended for the clean space relative to unrated areas. In clean spaces with multiple rooms, the most sensitive areas should be the most highly pressurized. The trend is to maintain a positive pressure of 0.02 inches water column, or 5 Pascals, between adjacent clean spaces of differing ratings, with the higher pressure in the space at the higher cleanliness rating. This ensures that the air does not transfer from less cleaner spaces to the more stringent cleanroom space. The only exception to using a positive differential pressure is when dealing with specific hazardous materials where the regulatory health and safety agencies require the room to be at a negative pressure.

Only a minimal amount of air should be introduced into the controlled environment. Make-up air is very expensive in that it must be tempered, humidity adjusted, and cleaned before being introduced into the cleanroom. Careful attention needs to be paid to NOT over-pressurize the area. With higher pressurization, the leakage velocity, leakage rates and processing costs would also increase. While make-up air is unavoidable, it should be minimized to the extent possible in the interest of energy conservation. Positive pressurization can be maintained only if the sealing integrity of the building is maintained. The building should be air tight for low air leakage rates. There are areas within the facility that require negative exhausts such as toilets, pantries, laboratory vent hoods and battery rooms, but these are controlled ventilation areas having a fixed amount of exhaust. Uncontrolled leakage areas in the building are door undercuts, pass throughs, walls, ceilings, duct joints, etc., and should be restricted as far as possible. As a rule of thumb, the quantity of make-up air can be determined by adding all the process exhaust volume in the space, and then adding two additional air changes per hour. This semi-empirically derived value has proven to be a safe value to use to help determine the size of the make-up air handler. Actual make-up air introduced at any one time will vary depending on door openings, leakage, and actual exhaust in operation. This provides the assurance that carbon dioxide and oxygen remain in balance, that formaldehyde and other vapors given off by building materials, paints, furniture, and so forth, are diluted, and that air changes occur with sufficient frequency to minimize the chance for high concentration of airborne pollutants within the building.

Over pressurization is a waste of energy that not only entails high capital costs, but also increases the operating costs. Let's look at a couple of examples. Before we begin, it is useful to know that one-inch water gauge pressure is equivalent to wind velocity of 4005 feet per minute, or approximately 45 miles per hour. High pressurization will result in higher leakage rates.

The amount of expected leakage can be calculated from these equations shown here:

$$\text{Leakage Velocity (fpm)} = (\text{Room pressure})^{1/2} \times 400$$

$$\text{Leakage rate} = \text{Opening Area(sq.ft.)} \times \text{Leakage Velocity(fpm)}$$

If we assume a 0.05 inch water column positive pressurization with a 2 square foot opening, we can calculate the Leakage Velocity and Leakage Rate, as shown here:

$$\text{Leakage Velocity} = (0.05)^{1/2} \times 4005 = 895 \text{fpm}$$

$$\text{Leakage rate} = 2 \times 895 \cong 1800 \text{ CFM}$$

The Leakage Velocity in this example is approximately 895 feet per minute. If we assume a 0.05 inch water column positive pressurization with a 2 square feet opening, then the Leakage Rate would be 1800 cubic feet per minute. Now let's see the impact on energy costs. For the same example above, assume the outside make-up air is at 34°C Dry Bulb and 21°C Wet Bulb temperature which needs to be conditioned to 21°C Dry Bulb and 15°C Wet Bulb temperature. From the psychrometric charts, the enthalpy difference, or the heat to be removed to bring outside air to cleanroom conditions, is 9.5 BTU per pound of air. The heat load is given by this equation shown here:

$$\text{Heat Load } Q(\text{BTU/hr}) = 4.5 \times \text{Airflow} \times \text{Enthalpy Difference}$$

For the case of 1800 CFM of leakage, the heat load would be 76,950 BTUs per hour, as shown here:

$$\text{Heat Load } Q(\text{BTU/hr}) = 4.5 \times 1800 \times 9.5 = 76{,}950 \text{ BTU/hr}$$

This is equivalent to 6.4 Tonnes of Refrigeration, where 1 Ton of Refrigeration, or 1 TR, is equivalent to heat removal rate of 12,000 BTU's per hour. Now, let's assume an increase in pressurization to 0.1 inch water column. This would result in a 40% increase to a 2530 CFM leakage rate. In this scenario, the heat load would be 108,234 BTU's per hour or 9.0 TR. Therefore, the fab will incur an extra capital cost equivalent to 9.0 - 6.4, or 2.6 TR. Not only is there an equipment capital cost, but for the second case, higher pressurization will cause recurring higher energy costs of nearly 4 kWh, if we use 1.5 kWh per TR of cooling load as a typical cost, which translates to 35000kWh per year on a 24 hours a day, 7 days a week fab operation.

Next, let's discuss air distribution strategies. Engineers have devised numerous air-management concepts over the years to supply and recirculate air in cleanrooms. Two common design strategies for the air handling system are the Single Pass System or Once-Through Air Handling System, and the Re-circulating System. The choice depends on a number of factors, such as the type of product being handled, the process operation, the process equipment design, toxicity of the product being produced, and impact on energy use. In a once-through air system, like we show in Figure 2, filtered air enters the room and is not re-circulated. All the air is exhausted outdoors. The system is used for cleanroom processes demanding 100% make-up air, or when ambient temperatures are favorable. As an example, when the potential of releasing dust or aerosolized materials exists, engineers recommend a "once-through" HVAC system.

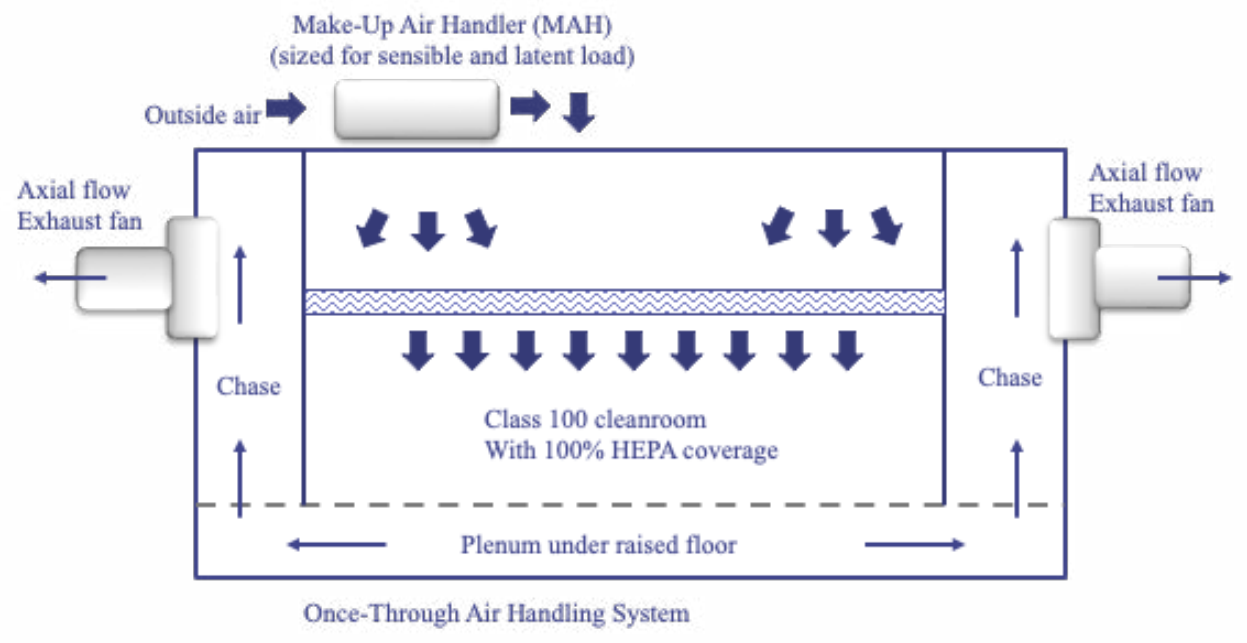

Figure 2- Diagram of a once-through air system.

Re-circulated systems are the most popular design for the reasons of economy of scale, size, and energy conservation. In these systems, filtered air enters the room, exits through plenum walls, and is re-circulated through a sealed plenum using motorized fan modules with HEPA filters. There are two fundamental recirculation system configurations: one, Centralized recirculation air-handling units, or RAHs; and two, Ceiling distributed fan-filter units, or FFUs. The selection of the system configuration is usually determined by the building configuration, initial investment cost, and ease of construction.

In next month's Feature Article, we will continue our discussion of HVAC technology for cleanrooms.

Technical Tidbit: Basic Integrated Circuit Floorplan Process Flow

This month's Technical Tidbit covers the basic process flow for creating an Integrated Circuit (IC) floorplan. The floorplan is basically the position of the major circuit blocks within the die area, along with the connections between those blocks.

Chip designers create the floorplan using a suite, or package, of automated software tools called "Place and Route" tools. Place and Route tools cover the spectrum from higher-level to lower-level software assistance leading to the final layout. As the name implies, these programs generally place the gates or circuit blocks and route the wires, in addition to other helpful functions. The first piece of software that the design team typically will use from the Place and Route tool suite is called the "Floorplanning" tool. It will help the design team create areas of functionality on the chip, determine the connectivity between these areas, determine the Input/Output, or I/O, pad placements, and give them feedback on how easy the floorplan might be to wire. The Floorplanning tool receives connectivity and gate information based on the netlist file, created by the compiler software.

Let's follow the Floorplanning tool in more detail, beginning with the initial assumptions and decisions. Typically, a chip will be divided into various functional areas. For example, if you are working on a large digital chip, there might be a microprocessor unit (MPU) in the chip, perhaps a floating point unit (FPU), and maybe a Random Access Memory (RAM) block and a Read Only Memory (ROM) block, as shown in Figure 1.

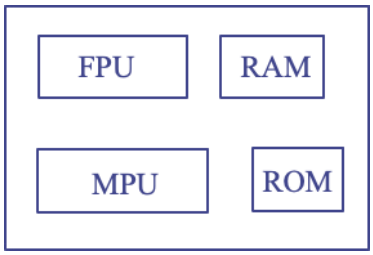

Figure 1 – Basic functional blocks in a complex digital IC

The location of each area of functionality is the decision of the design team, not the computer. For example, the design team might specify that all of the gates for the microprocessor go in the bottom left corner, all the gates for the RAM go in the top right corner, and so on. They will have a chance to change these decisions later, once they see how their decisions might affect the layout, and in particular, the wiring.

Once the design team specifies the areas of functionality, the first task would be to gather together, to some degree, the gates used in each block. For example, it would not be good to scatter the FPU gates throughout the ROM or RAM blocks. Associated gates should all be located near each other. The Floorplanning tool begins by helping to gather the gates together. The exact placement of each gate is not determined at this point. The designers do not yet need this level of detail. Besides, they might be changing their block placement decisions at some later point. A placement in the general vicinity is good enough for now. We show an example from a real IC block in Figure 2.

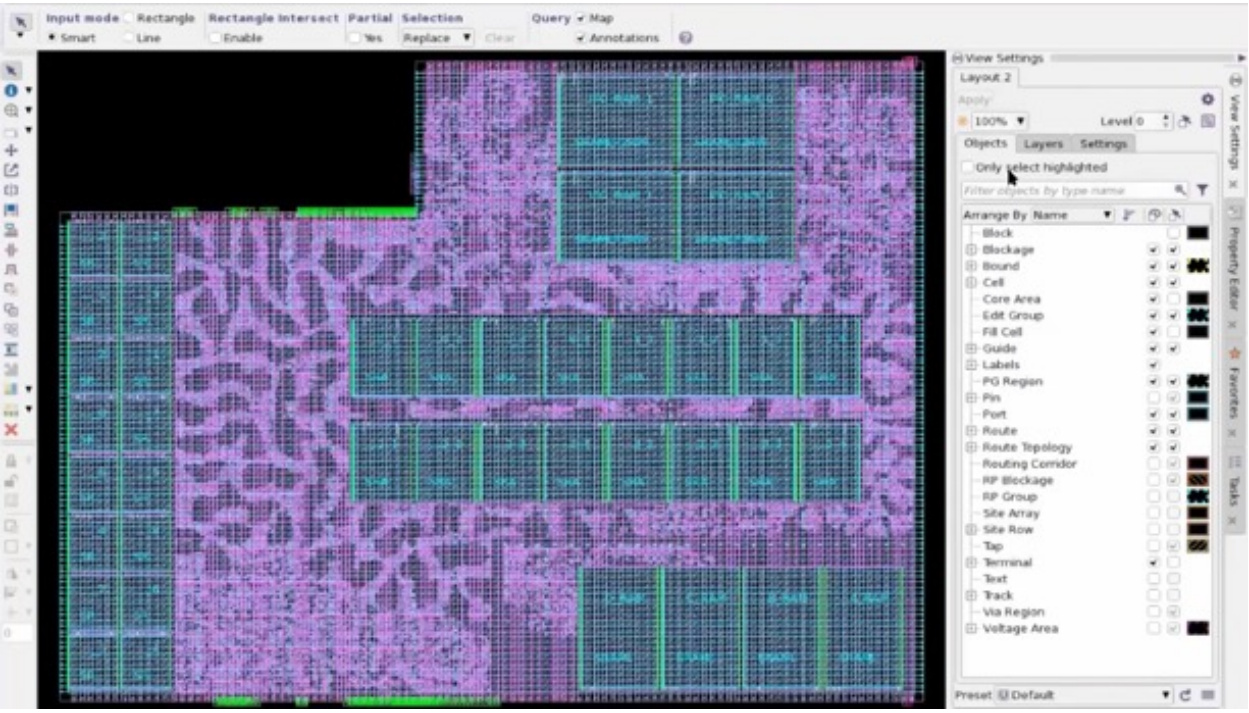

Figure 2- IC Floorplanning tool showing placement of blocks (in green) within a larger design area (Image Courtesy Synopsys).

Next, the Floorplanning tool will help the team place the Input/Output (I/O) cells for the chip, as seen in Figure 3. For instance, the designers may want all the inputs that go to the FPU close to the FPU block in the corner. To help them do this, some tools will actually place the I/O cells in the appropriate areas automatically; other tools will provide graphic feedback for them based on their placement decisions. The Floorplanning tool also shows basic wiring connections that must travel between blocks. It will show connections between the FPU and the RAM blocks, for example.

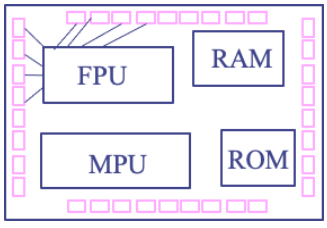

Figure 3- Placement of I/O cells and several connections between the FPU and the I/O cells.

The automated software programs such as the Simulator and Place and Route tools make choices a conscientious human with enough time would make, given the same information, at least in theory. However, in reality, one will see that constant human intervention and monitoring are essential. The software never operates without human supervision. The design team would have broadly defined where they wanted their high-level functional blocks, and their inputs and outputs. On their understanding of how the software operates, they would have predetermined some basic layout instructions for the software, depending on the chip specifications, the size of the final package in which the chip will be placed, and the specific circuitry. The tools never run completely by themselves. The human brain must oversee the working of the tools or the tools become useless.

Typically, the Floorplanning tool will show the designers all the wiring lines coming from each block connecting to the I/O pads and to other blocks. All these wiring lines are what most tools call rat's nests or flylines. As the designer clicks, drags, and resizes blocks around their computer monitor, they will see all these wiring connections moving around in real time with their cursor. One technique that works well is to look for crossovers. As you drag your blocks around with your cursor, watch the lines. If the lines become badly crossed-over and generally messy, you know that it will be tough to wire the circuitry. If there are no cross-overs of the flylines, then it will be easy to wire. Neat flylines indicate a good floorplan. Figure 4 shows an example of this.

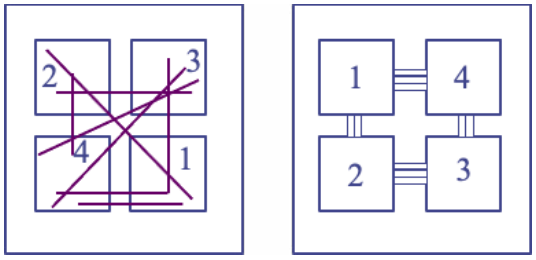

Figure 4- Many crossed flylines (left) and no crossed flylines (right).

The design team will make changes to their block floorplan so that the rat's nest eventually looks as clean, nice, and "wireable" as possible. They might decide to relocate entire areas of functionality. They might bring one small block across to the other side and fit it between two larger blocks. They might bring a center block to the outside, or an outside block to the center. When they finally have a block diagram which gives them nice, simple wiring, they would save their floorplan output files.

Since the output files from the Floorplanning tool specify where the gates will be generally located, the placement tool roughly knows how long all the wires will be. These wiring length estimations are based on the physical dimensions of the digital cell library. The digital cell library is a collection of information about the gates, or cells, used in the circuit design. Using this information, the Floorplanning tool can output an estimated wire length file that goes back into the digital circuit simulator. The design team can now run some simulations to determine how their estimated wiring lengths will affect their digital circuit. They must check the possibility that long wires will slow the circuit signals too much, affecting the circuit timing.

If the wire lengths are indeed negatively affecting the circuit timing, the design team will need to modify their design, based on their floorplan. They will change the netlist. They might place higher-powered cells in the block to drive the extra wiring capacitances, for example. As the design team works to better organize the design, not only is it easier to wire, but they will discover that the chip operates in a more robust manner in the end. The design team might go through this floorplan and timing check loop a couple of times. The Simulator will eventually let them know when they have met the timing criteria. At some point, the team will finally decide that they have a good design. They will then move on to fixing their circuits in place, so to speak. The fine-tuning now begins to finalize the design before tape-out.

Ask The Experts

Q: What are some items that can cause bottlenecks during the lithography process?

A: There are several items which can cause bottlenecks. We will discuss one in particular. The operators may need to wait for the lens to cool down to prevent the lens heating, since lens heating will cause a change in the aberration of the lens, causing the pattern on the chip to defocus. Due to this problem, operators may be unable to pattern critical logpoints like STI Isolation regions (sometimes referred to as moats), and Gate regions, back-to-back.

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Course Spotlight: PRODUCT QUALIFICATION OVERVIEW COURSE

OVERVIEW

Package reliability and qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can also involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. In particular, the proliferation of new package types can create difficulties. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. Customers expect fast, smooth qualification, but incorrect assumptions, use conditions, testing, calculations, and qualification procedures can severely impact this process. Your company needs competent engineers and scientists to help solve these problems. Product Qualification Overview is 1-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability and product qualification. This course is designed for every manager, engineer, and technician concerned with qualification in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

Participants learn to develop the skills to determine the best process for qualification, how to identify issues, and how to resolve them. This skill-building series is divided into four segments:

1. Qualification Principles. Participants learn how test structures can be designed to help test for a particular failure mechanism.

2. JEDEC Qualification. Participants learn how to perform a Joint Electron Device Engineering Council (JEDEC) Standard 47 Qualification. We cover the overall procedure and introduce the individual tests. We also discuss items related to requalification.

3. AEC Q-100 Qualification. Participants learn how to perform an Automotive Electronics Council (AEC) Q-100 Qualification. We cover the overall procedure and introduce the individual tests. We also discuss the important differences between the AEC Q-100 Qualification process and the JEDEC Qualification process.

4. JEDEC Tests. Participants learn about the JEDEC tests. We cover the more important individual tests used in the qualification of semiconductor components. These tests are common to both the JEDEC and AEC standards.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, equipment, and testing methods used to qualify today's components.

2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.

3. The seminar will identify major failure mechanisms; explain how they are observed, how they are modeled, and how they are handled in qualification.

4. The seminar will discuss the major qualification processes, including JEDEC JESD47, AEC Q-100, and other related documents.

5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.

6. Participants will be able to knowledgeably implement additional tests that are appropriate to assure the reliability of a component.

7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

COURSE OUTLINE – Lecture Time 8 Hours

1. Overview of Qualification
   a. Basic Concepts
   b. Knowledge-based Qualification versus Standards-based Qualification
   c. Components of a Qualification Plan

2. Statistics Concepts Used for Qualification
   a. Basic Statistics
   b. Distributions (Normal, Lognormal, Exponent, Weibull)
   c. The Poisson distribution
   d. Acceleration
   e. Number of Failures

3. Overview of JEDEC JESD47
   a. Scope
   b. General Requirements
   c. Qualification and Requalification
   d. Qualification Tests
   e. Process and Product Changes

4. Overview of AEC-Q100
   a. Scope
   b. General Requirements
   c. Qualification and Requalification
   d. Qualification Tests
   e. Qualification Families, Use of Generic Data
   f. Differences between JEDEC and AEC

5. JEDEC Tests
   a. Preconditioning/Moisture Sensitivity Level Testing
   b. High Temperature Operating Life
   c. Autoclave
   d. Highly Accelerated Stress Test (HAST)
   e. Unibased HAST
   f. Temperature Humidity Bias Test
   g. Temperature Cycling
   h. Power Temperature Cycling
   i. High Temperature Storage Life Test
   j. Electrostatic Discharge (ESD) Human Body Model and Charged Device Model Testing
   k. Latch-Up Testing
   l. Board-Level Testing (Bend Test, Drop Test)

6. Conclusions

Upcoming Courses:

Public Course Schedule:

Product Qualification Overview - September 11, 2023 (Mon.) | Phoenix, Arizona - $695

Advanced CMOS/FinFET Fabrication - September 25-26, 2023 (Mon.-Tues.) | Phoenix, Arizona - $995

IC Packaging Technology - January 23-24, 2024 (Tues.-Wed.) | Phoenix, Arizona - $1,295

Advanced CMOS/FinFET Fabrication - January 29-30, 2024 (Mon.-Tues.) | Phoenix, Arizona - $995

Wafer Fab Processing - February 26-29, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095

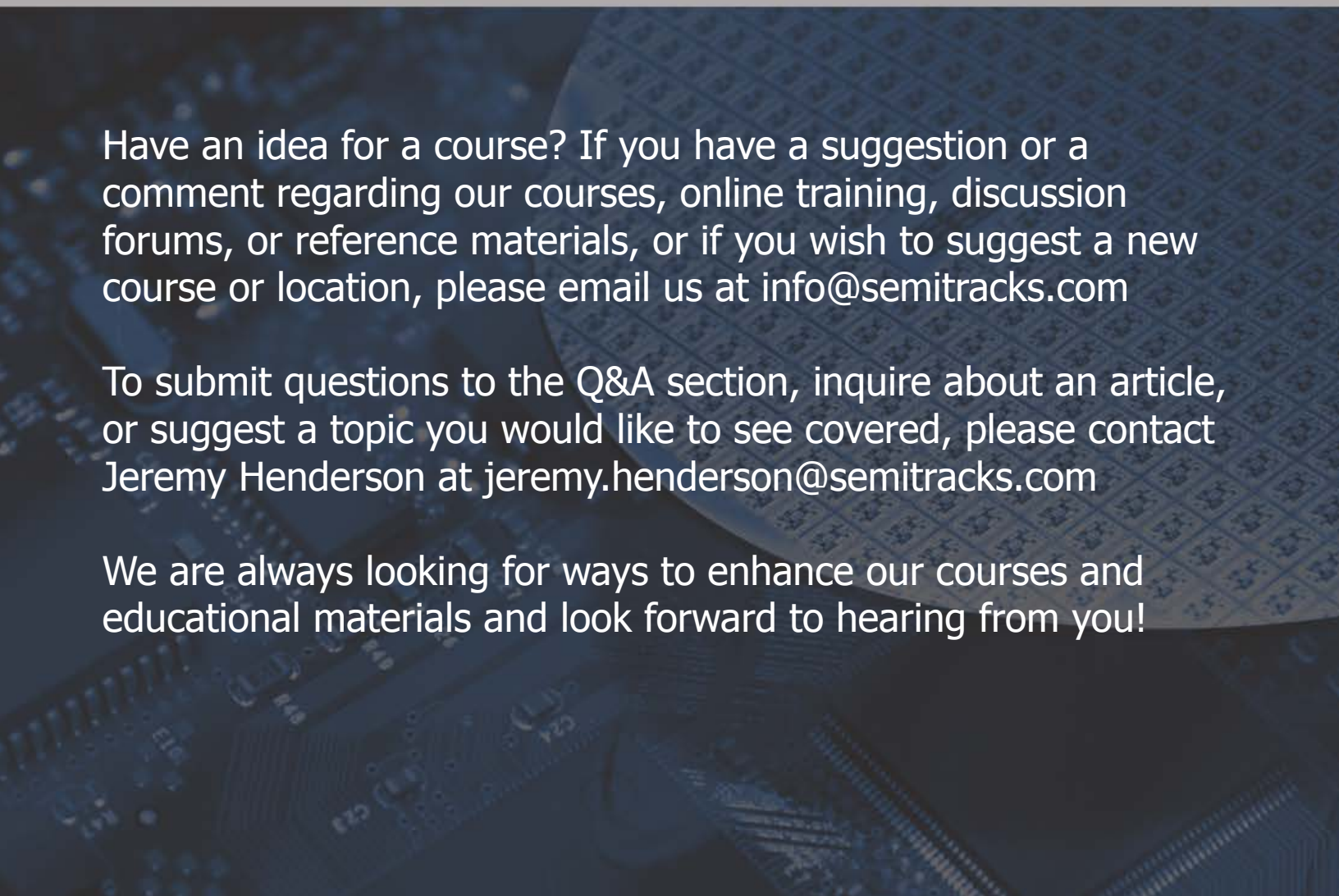
Failure and Yield Analysis - March 4-7, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095

Semiconductor Reliability and Product Qualification - March 11-14, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095

Defect-Based Testing - March 20-21, 2024 (Wed.-Thurs.) | Munich, Germany - $1,195

Webinar Schedule:

IC Packaging Design and Modeling - September 18 - 21, 2023 (Mon. – Thurs.) | - $600



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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!