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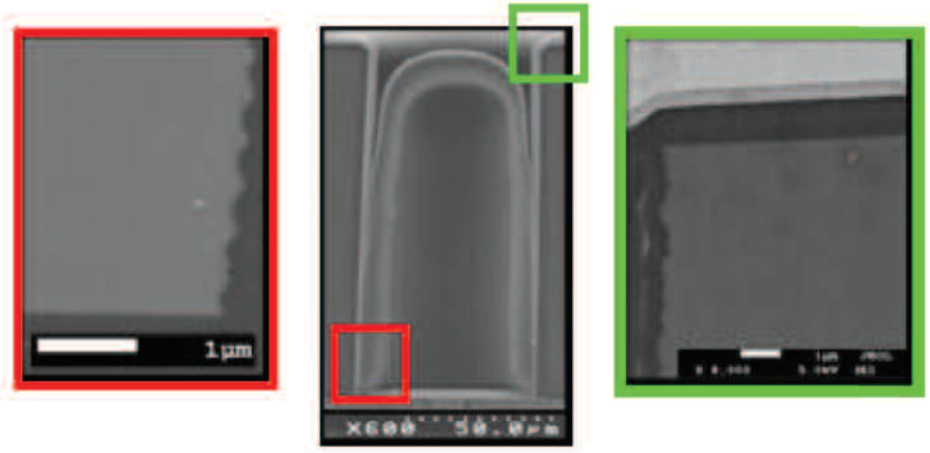
InfoTracks

Semitracks Monthly Newsletter

TSV Failure Mechanisms II

By Christopher Henderson

Another TSV failure mechanism is caused by etch-related problems. These images show examples of notching and undercutting due to micromasking. The notching is in red on the left, and the undercutting is in green on the right. This can lead to high electric fields in the liner materials, and earlier breakdown to the dielectric materials in the liners.



Yet another TSV failure mechanism is voiding. This can occur at the interface between the copper TSV and the metal layers. The voiding leads to increased resistance in the via, and the possibility of

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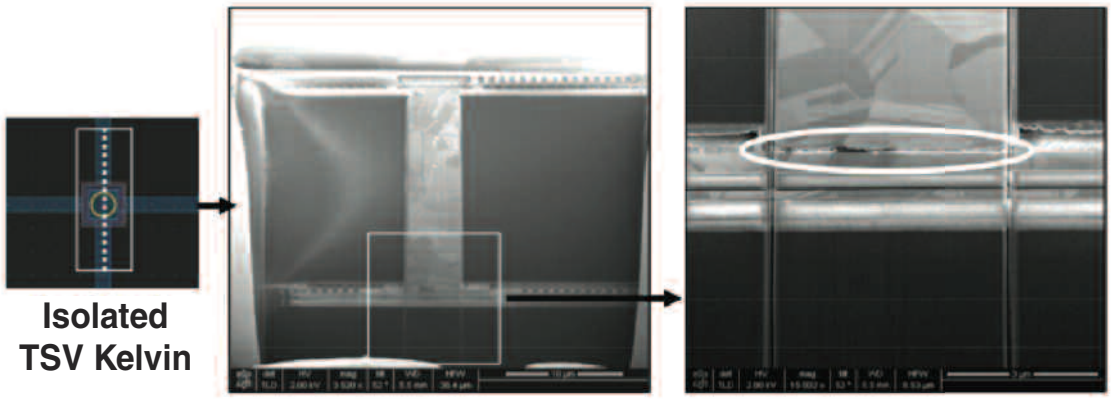
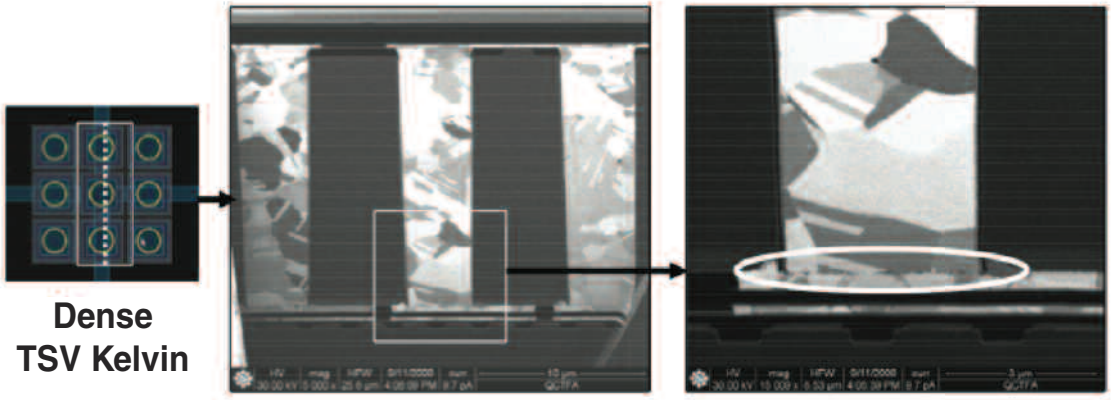
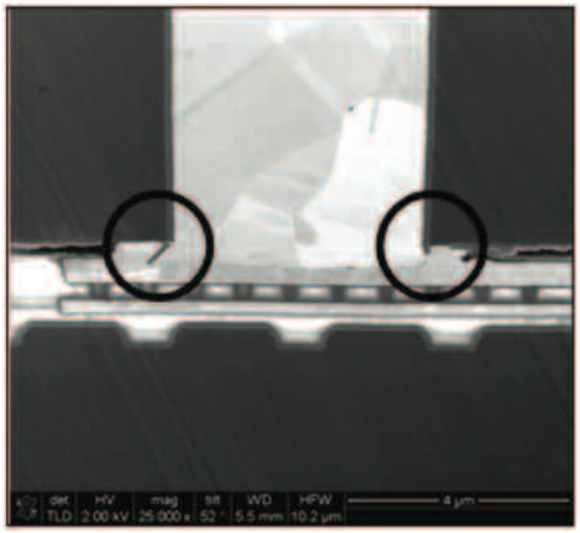
electromigration in the remaining material at the interface. The series of images above show voiding in an isolated TSV structure, and in a dense TSV structure.

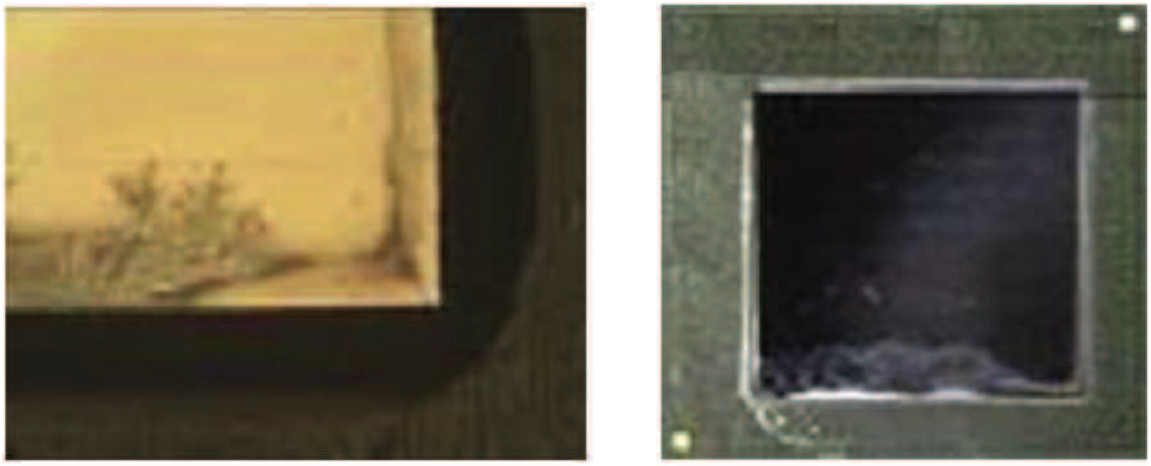




Another TSV failure mechanism is copper extrusion. This can happen when the compressive stress on the copper causes the copper to extrude into the surrounding layers. This can lead to a short. The image above shows an example of extrusions occurring on both sides of the TSV.



The final problem we'll discuss with TSVs is a problem known as underfill overflow, or bleedout. Typically, one uses TSVs in conjunction with thin die. The thin die may not lay flat, and this can lead to situations where the underfill can flow into the redistribution layer associated with the TSV. The underfill material reduces the cross-section area, and can lead to delamination at the interface, causing a catastrophic failure. The images above show examples where the underfill material is contaminating the RDL layer.



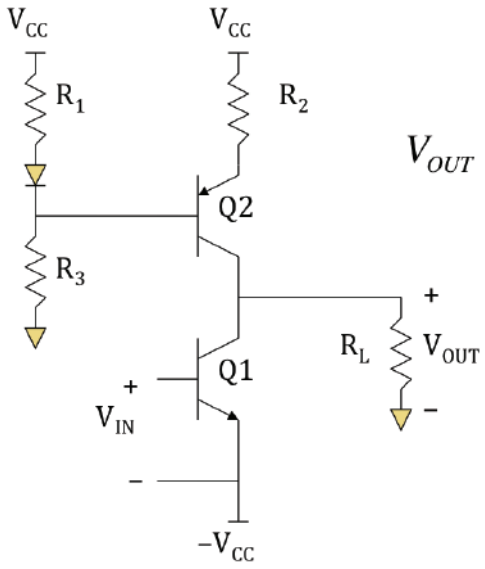
The flip chip die can be thin, so overflow may contaminate RDL layer of TSV

In summary, TSVs are becoming more important in today's chips as Moore's Law runs out of steam and chip designers turn to the 3rd dimension to increase density and performance. This is a relatively new area, so researchers may continue to discover new mechanisms. Many of the existing mechanisms can be minimized through the use of finite element analysis to identify regions of high stress, and modeling alternate configurations that can lower the stress.

Technical Tidbit

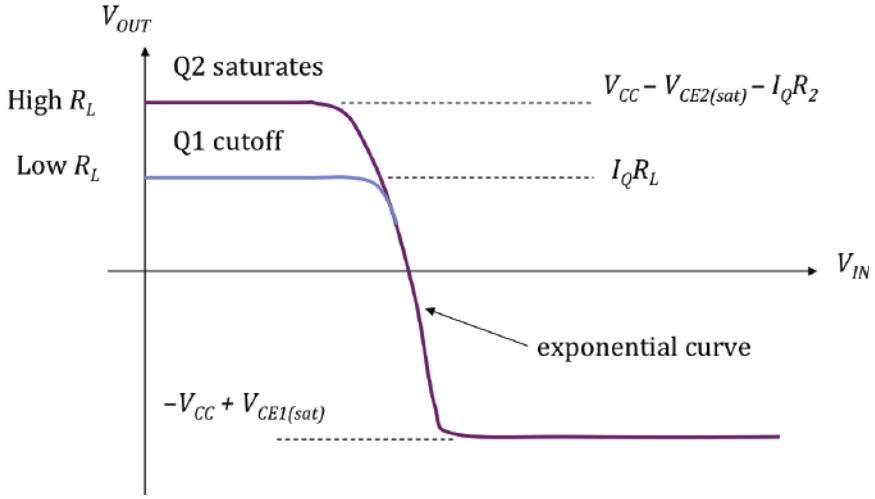
Class A Amplifiers

This month's technical tidbit discusses the class A amplifier. The Class A amplifier is one of the most common amplifier configurations. Designers use this circuit extensively in many amplifier applications, from basic op amps like the 741 op amp, to more sophisticated amplifiers that are used in complex mixed-signal applications.

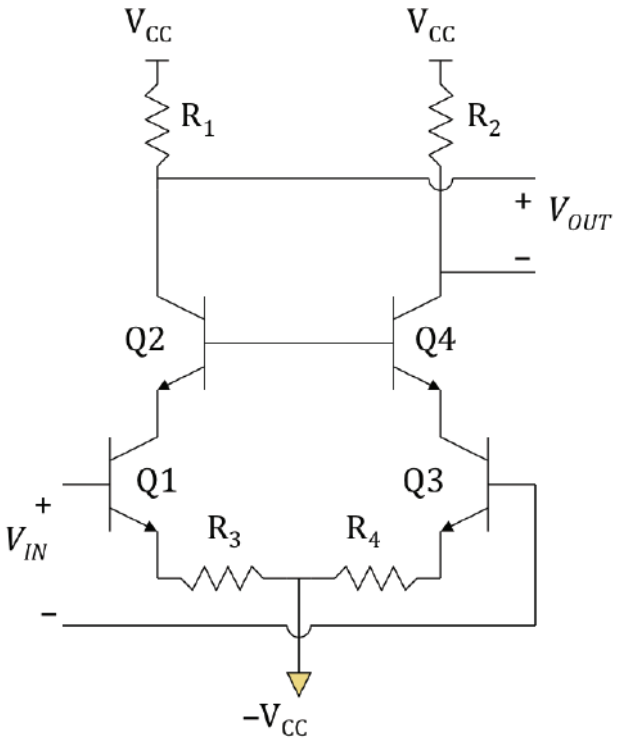


$$V_{OUT} = -R_L\left(I_S \exp\frac{V_{IN}}{V_T} - I_Q\right)$$

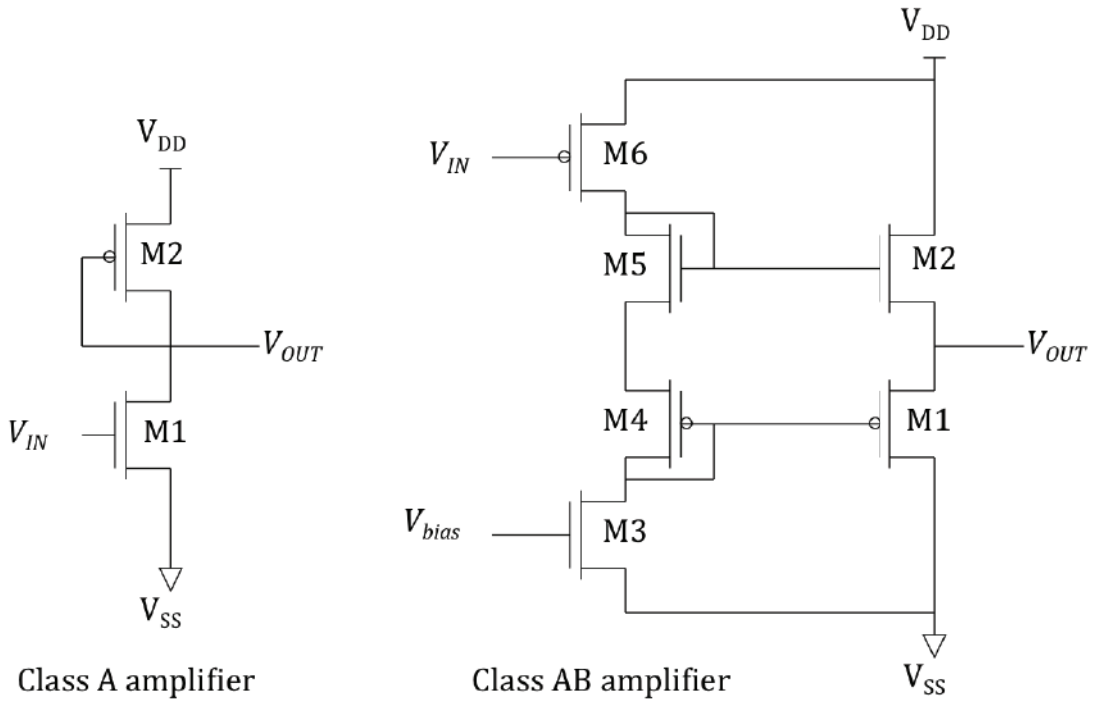
This slide shows the Class A common emitter output stage. Common emitter circuits are most often used as output drivers in larger circuits. The output voltage is a function of the resistive load, the input voltage on Q1, the thermal voltage, and the current through the output stage, and is given by this equation (see figure above, right). Common emitter circuits exhibit high gain characteristics. Because the transfer characteristic for this particular circuit is exponential in nature, the common emitter output stage exhibits more distortion than an emitter-follower output stage.



In this figure, we show the output voltage as a function of the input voltage for the common emitter stage. We also refer to this type of graph as the transfer characteristic. The slope of the transfer characteristic for the common emitter stage is exponential in nature. If the slope were linear, there would be no distortion in the gain. Since the slope is non-linear, distortion is introduced into the amplification stage. The transfer characteristic can also be affected by the load on the output. If there is a high resistance load, then Q2 will saturate, leading to a higher output voltage. If the resistance is low, then Q1 is forced into a cutoff condition. This lowers the output voltage on the positive side.



Let's look at a different, and more popular, way to implement the Class A amplifier. This slide shows an example of a Class A common base output stage. In this example the output voltage is the difference between the voltages on the collectors of Q2 and Q4. This is controlled by the input voltage, which is the difference between the voltages on the bases of Q1 and Q3. Although we show bipolar circuits in these figures, designers can implement Class A amplifiers in both bipolar and CMOS.



Class A amplifier Class AB amplifier

In many instances, a designer would prefer an amplifier that doesn't dissipate large quantities of power to achieve high levels of performance. In the class A amplifier on the left, the power dissipation increases as one tries to switch a capacitive load on Vout at higher frequencies. In other words, to switch V_{out} faster, M2 must draw more current, leading to higher power dissipation levels. The class AB amplifier can help solve these problems. In the class AB amplifier on the right, M1 and M2 can be biased using M4 and M5. M3 is simply a constant current source used to help bias M1 and M2 on. This configuration is useful as a output buffer in an operational amplifier. Note that the substrates of the NMOS transistors are tied to VSS while the n-wells of the PMOS transistors are tied to VDD.

Ask the Experts

Q: How do wafer manufacturers create such large single crystal ingots with the Czocralski method??

A: There are a number of factors, but the three major ones would be the slow speed with which they raise the seed crystal from the melt, the rotation speed of the seed crystal, and the rotation of the crucible.

Spotlight: Failure and Yield Analysis

OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Your industry needs competent analysts to help solve these problems. ***Advanced Failure and Yield Analysis*** is a four-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a ***Do It Right the First Time*** approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

Participants learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. **The Process of Failure and Yield Analysis.**Participants learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.
2. **The Tools and Techniques.** Participants learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools, light emission, electron beam tools, optical beam tools, decapping and sample preparation, and surface science tools.
3. **Case Histories.** Participants identify how to use their knowledge through the case histories. They learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.
2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.
3. The seminar will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.
4. The seminar offers a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic technology features on semiconductor devices.
6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

One unique feature of this workshop is the video segments used to help train the students. Failure and Yield Analysis is a visual discipline. The ability to identify nuances and subtleties in images is critical to locating and understanding the defect. Many tools output video images that must be interpreted by analysts. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

1. Introduction
2. Failure Analysis Principles/Procedures
   a. Philosophy of Failure Analysis
   b. Flowcharts
3. Gathering Information
4. Package Level Testing
   a. Optical Microscopy
   b. Acoustic Microscopy
   c. X-Ray Radiography
   d. Hermetic Seal Testing
   e. Residual Gas Analysis
5. Electrical Testing
   a. Basics of Circuit Operation
   b. Curve Tracer/Parameter Analyzer Operation
   c. Quiescent Power Supply Current
   d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
   e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
   f. Automatic Test Equipment
   g. Basics of Digital Circuit Troubleshooting
   h. Basics of Analog Circuit Troubleshooting

6. Decapsulation/Backside Sample Preparation
    a. Mechanical Delidding Techniques
    b. Chemical Delidding Techniques
    c. Backside Sample Preparation Techniques
7. Die Inspection
    a. Optical Microscopy
    b. Scanning Electron Microscopy
8. Photon Emission Microscopy
    a. Mechanisms for Photon Emission
    b. Instrumentation
    c. Frontside
    d. Backside
    e. Interpretation
9. Electron Beam Tools
    a. Voltage Contrast
        i. Passive Voltage Contrast
        ii. Static Voltage Contrast
        iii. Capacitive Coupled Voltage Contrast
        iv. Introduction to Electron Beam Probing
    b. Electron Beam Induced Current
    c. Resistive Contrast Imaging
    d. Charge-Induced Voltage Alteration
10. Optical Beam Tools
    a. Optical Beam Induced Current
    b. Light-Induced Voltage Alteration
    c. Thermally-Induced Voltage Alteration
    d. Seebeck Effect Imaging
    e. Electro-optical Probing
11. Thermal Detection Techniques
    a. Infrared Thermal Imaging
    b. Liquid Crystal Hot Spot Detection
    c. Fluorescent Microthermal Imaging
12. Chemical Unlayering
    a. Wet Chemical Etching
    b. Reactive Ion Etching
    c. Parallel Polishing

13. Analytical Techniques
    a. TEM
    b. SIMS
    c. Auger
    d. ESCA/XPS
14. Focused Ion Beam Technology
    a. Physics of Operation
    b. Instrumentation
    c. Examples
    d. Gas-Assisted Etching
    e. Insulator Deposition
    f. Electrical Circuit Effects
15. Case Histories

DESIGN AUTOMATION CONFERENCE 54

2017 Design Automation Conference

June 18-22, 2017
Austin Convention Center
500 E. Cesar Chavez St.
Austin, TX, USA 78701

Registration is available at www.dac.com

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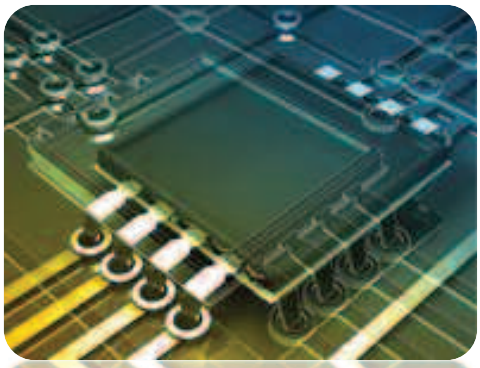
Semitracks will be at the Si2.org booth, and would be happy to discuss training needs, and creating training materials for your userbase.
Contact us at info@semitracks.com during the conference!



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Upcoming Courses

(Click on each item for details)

Failure and Yield Analysis
September 11 – 14, 2017 (Mon – Thur)
San Jose, California, USA

Semiconductor Reliability / Product Qualification
September 18 – 21, 2017 (Mon – Thur)
Portland, Oregon, USA

Failure and Yield Analysis
April 9 – 12, 2018 (Mon – Thur)
Munich, Germany

Wafer Fab Processing
April 9 – 12, 2018 (Mon – Thur)
Munich, Germany

Semiconductor Reliability / Product Qualification
April 16 – 19, 2018 (Mon – Thur)
Munich, Germany