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CMP – Applications and Issues Part 1

By Christopher Henderson

This article is the first in a series of three articles on Chemical Mechanical Planarization (CMP) applications and issues. Today, process engineers use CMP for a variety of planarization applications, including dielectrics, metals, and even shallow trench isolation integration steps.

In this series of articles, we will cover several uses for chemical mechanical polishing. We will start with an overview of the technology. We'll then discuss the oxide CMP process, followed by the tungsten CMP process, and the copper CMP process. Since each of these materials is somewhat different, the slurries and pads are different. Finally, we'll discuss the use of CMP for shallow trench isolation.

There are two major applications of CMP: global planarization and the formation of recessed structures. For global planarization one selectively removes film material from elevated regions to eliminate the steps, and then stops once the surface is planarized. Process engineers typically do this for the interlevel and intermetal dielectric layers, and can achieve a β of 0.95. For plug or recessed layers, the process engineers remove the blanket layer of film—leaving it only in the recessed areas—for structures like contacts, vias and damascene interconnect. These two applications facilitate modern processing. One can now achieve many layers of interconnect with a very high device packing density with advanced interconnect materials at nanometer linewidths.

Figure 1 shows the process of removing material by CMP from a graphical standpoint. There is removal of homogeneous material but stopping before the entire surface film is removed, like we might see

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with planarization of an interlevel dielectric. There is also removal of material—but not stopping until all the material is removed on some regions of the wafer surface—but other material is allowed to remain in recessed regions, like the formation of recessed copper lines by CMP in damascene interconnect structures.

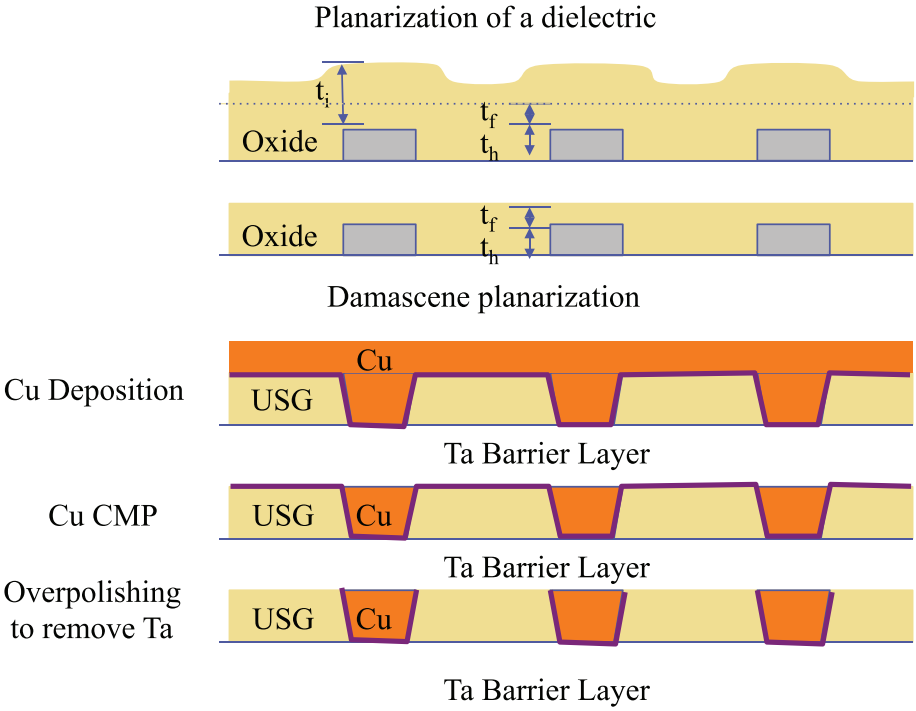


Figure 1. Graphic showing planarization of a dielectric (top), and damascene planarization (bottom).

Process engineers will use a formula called Preston's Law to make a rough calculation of the removal rates for CMP. Preston's Law states that for polishing optical glass the removal rate is given by Preston's coefficient K_p, the applied pressure P and the linear velocity of the pad v.

$$R = K_p P v$$

Preston's coefficient is a good first-order approximation for the removal of silicon dioxide on unpatterned wafers, but it does not explain how planarization occurs since the removal rate would be higher in elevated regions and lower in depressed regions. For a more accurate calculation, one must take into account a number of other factors like feature dimensions, density, the step heights, and the structure and conditioning of the pad.

Although CMP is easy to understand in principle, there are a number of complex mechanisms involved with the removal process. Process engineers also take advantage of different mechanisms for different film types. There are a number of variables involved. The types of films being polished—whether metal or dielectric—are important. The reactivity, hardness, presence of liner films and other properties and features complicates the process. The slurry is important. Its composition, hardness, particles sizes, shapes and pH factors all play a role. The pad is also important. The hardness, porosity and conditioning affect the outcome. And the operating variables like pad pressure, pad velocity, table velocity, slurry feed rate and other variables play a role as well. The desired process characteristics include a high removal rate, a high degree of planarity—both locally and globally, high selectivity, and low defectivity.

Let's now discuss CMP as applied to various materials. We begin with the metals. Metal CMP is a two-step process. Process engineers oxidize the metal through the chemical portion of the process, and use slurry abrasives to remove the oxidized metal through the mechanical part of the process. The slurry composition is important. Process engineers must balance the chemical reactivity with the mechanical abrasiveness to remove the material evenly. They must also match the hardness of the slurry to the hardness of the metal oxide. For aluminum interconnect one uses alumina particles, but for copper one uses softer slurries or even slurries with no abrasives. Figure 2 shows a schematic representation of the model for CMP processing of metal films. It begins with the formation of the passivating film through chemical oxidation, followed by the removal of the passivating film by mechanical abrasives. The unprotected metal is etched by the chemical action and the passivation reforms. This is a repetitive cycle.

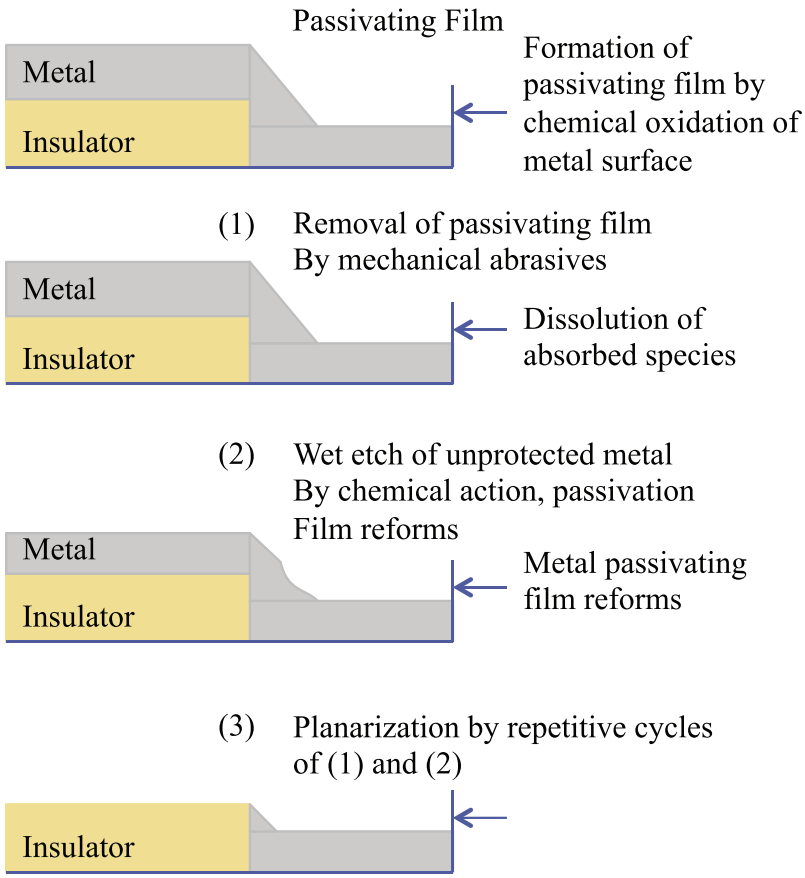


Figure 2. CMP Process represented schematically.

Tungsten is a hard metal that poses a unique challenge for CMP. The industry makes extensive use of tungsten vias, since they exhibit superior performance to aluminum vias. However, tungsten is a hard material, making it difficult to polish without overpolishing the surrounding oxides. It requires a three-step process to remove the tungsten, remove the liner, and smooth the oxide. To remove the tungsten layer, process engineers use electrochemical oxidation of the tungsten to produce tungsten oxide. They then use alumina slurry in hydrogen peroxide plus iron nitrate or potassium iodate to polish and etch the tungsten. Alumina is preferred over silica slurries, because it has a better selectivity to the oxide layers. They then remove the titanium nitride/titanium liner with alumina slurry and smooth the oxide with silica slurry.

The drawing in Figure 3 on the left shows tungsten plug formation using CMP. First, tungsten is deposited over the titanium/titanium-nitride barrier layers. Next, the tungsten and titanium/titanium-nitride is removed by CMP. Finally, an oxide buff eliminates the plug recess. The scanning electron microscope image in Figure 3 on the right shows a tungsten plug after the CMP and oxide buff steps.

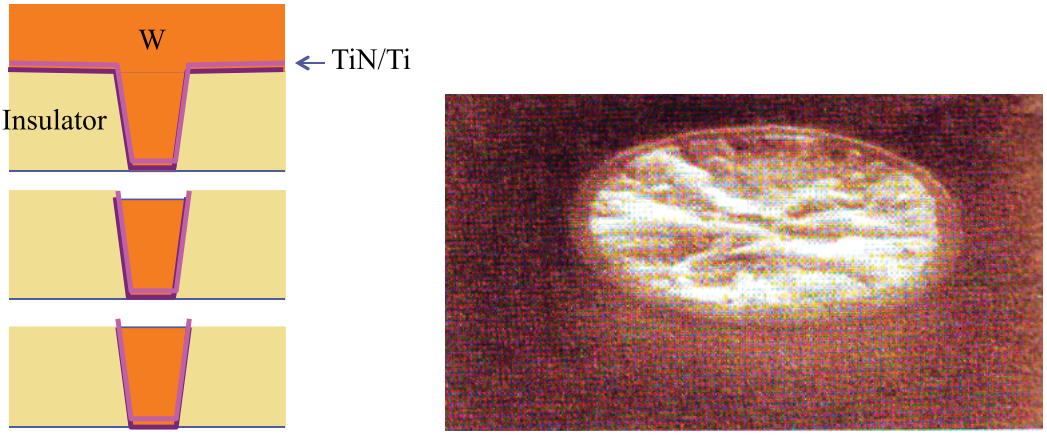


Figure 3. Tungsten CMP Process (left), and image of plug after CMP (right).

Let's now turn our attention to copper. Copper by itself is easy to remove by CMP since it is soft and oxidizes easily. The most common slurries for copper polishing are alumina-ammonium hydroxide mixtures. The ammonium hydroxide facilitates the dissolution of the copper. Other oxidizing agents like hydrogen peroxide are occasionally used in conjunction with ammonium hydroxide to increase dissolution. The removal rate is quite high, and the selectivity to the underlying oxide is also quite high. If there is a problem, it is usually related to smearing of the copper while polishing. The liner materials, however, are a different story. The most common liner, tantalum, is quite hard like tungsten and difficult to oxidize. The removal rate ends up being quite slow. The mismatch between these two metals leads to CMP dishing of wide interconnect. Process engineers also use a three-step process to remove copper: they remove the copper layer, then the liner, and then buff and smooth the oxides. This requires different platens with different slurries. And in some applications, the engineers may want to remove a top layer of oxide to remove facets in the oxide from prior processing.

A newer technique for planarizing copper metal structures is ECMP, or Electrochemical Mechanical Polishing. Process engineers press water against a polishing pad to achieve what is in essence, the reverse of electroplating. To do this, they apply a bias between the wafer surface and the cathode, causing the copper to dissolve into an electrolyte solution. The advantages of this approach are lower costs, since this requires no abrasives, and better process control, since there are no pattern dependencies. However, one still must deal with the liners, so ECMP must be followed by conventional copper CMP steps to remove the remaining copper layer, remove the tantalum liner film, buff and smooth the oxide.

Another newer technique is abrasive-free polishing. This approach uses non-abrasive material to remove the oxidized metal like a high molecular weight organic polymer. The term "abrasive-free" polishing is a bit of a misnomer, since there is still mechanical abrasion between the wafer and the pad. The advantages of this technique include higher selectivity to the barrier metals and dielectrics, less erosion and dishing due to lower pad pressures, and easier post CMP cleaning, since there are no particles to remove from the surface.

Next month we'll cover CMP of oxide layers.

Technical Tidbit

Zero Mode Waveguides

A zero mode waveguide is a structure designed to designed and fabricated in such a way as to look at features below the wavelength of the light being used. This is an approach that Pacific Biosciences is using to examine DNA structures. One creates sub 100 nanometer holes by patterning structures on an aluminum thin-film with electron beam lithography and then using a reactive ion etch to etch through the aluminum layer. Process engineers bond the aluminum layer to glass so that one can image the waveguide through the glass layer.

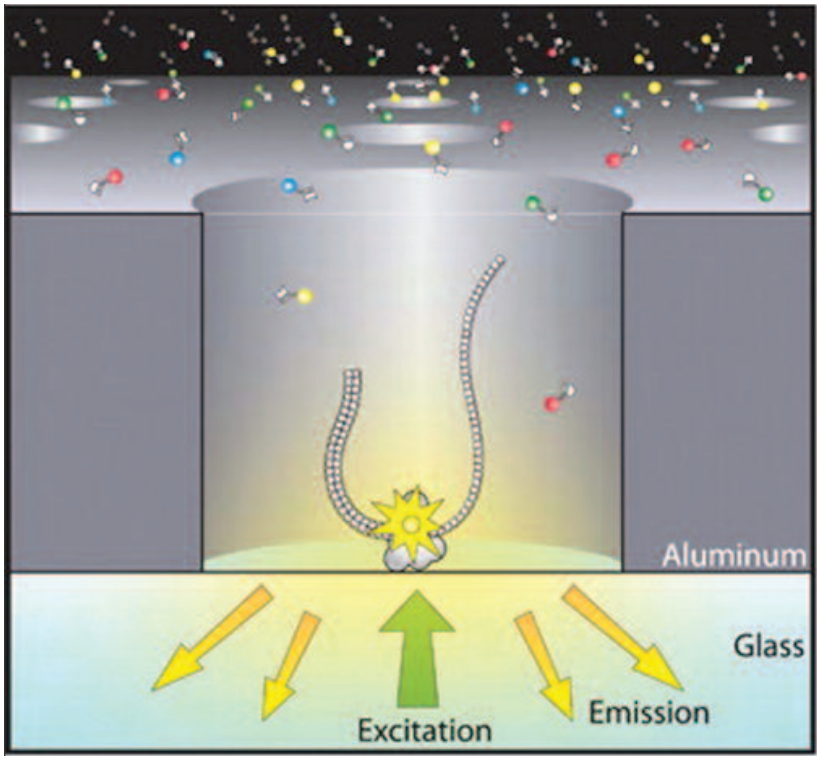


Figure 1. A Zero-Mode Waveguide and its conceptual use for DNA sequencing and identification.

Since the holes are smaller than the wavelength of the light used for sample analysis, the first order light, or the normal viewing light, is unable to pass through the tiny hole. However, the zero-order light, or the near field effect light can penetrate a small distance into the hole. This provides the ability to examine both small lateral and vertical dimensions. The image and graphs at the bottom illustrate this point. The image on the left shows a three-dimensional finite element time-domain simulation of the intensity distribution on a log scale for a zero-mode waveguide that is 50 nanometers in diameter and 100

nanometers long. The graph at the center shows the effective observation profile as a function of depth into the waveguide, and the graph on the right shows the effective observation volume as a function of the waveguide diameter.

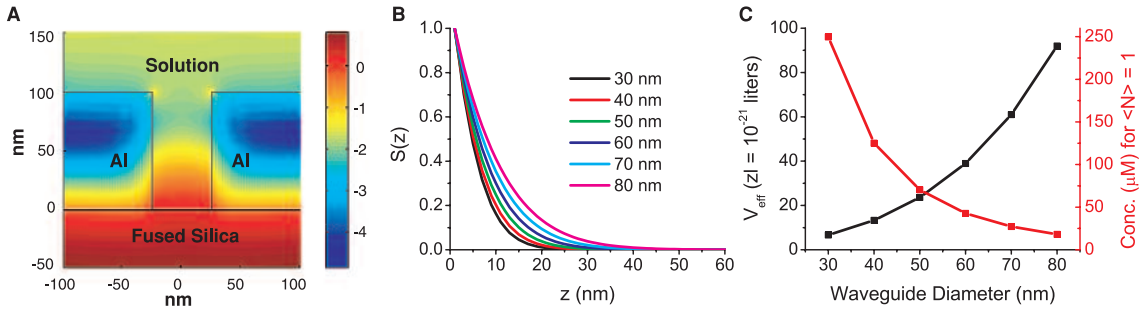


Figure 2. Simulation of intensity distribution for a 50nm waveguide, and the effective observation profile and the effective observation volume as a function of the waveguide diameter.

Ask the Experts

Q: How do I etch down to the polysilicide layer without damaging it?

A: For failure analysis purposes a recipe like this would work decently. It's based off of one of the main patents for opening contact windows over titanium silicide.

Power 200W
Pressure 100 mTorr
Gas 1 CHF_3 50 sccm
Gas 2 CF_4 10 sccm
Gas 3 Ar 100 sccm

TEOS Etch Rate	494 Å/min
Annealed TEOS	450 Å/min
Photoresist Etch Rate:	117 Å/min
Thermal Oxide Etch Rate:	441 Å/min
Silicon Etch Rate	82 Å/min
$TiSi_2$ Etch Rate	1 Å/min

The etch rate for CoSi or NiSi might be somewhat different, but I think this would give sufficient selectivity to expose the polysilicide layer cleanly without damaging the layer. Where problems might occur is if there are silicon-rich regions in the polysilicide, they can be leached out by the RIE process.

Spotlight: Changes to Come

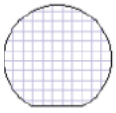
In the next month we will be upgrading our Online Training System Platform. Part of the reason to upgrade is to take advantage of some newer database technology features available in PostGreSQL and improve the implementation of some administrator functions, but another reason is to improve the user experience. The new system will allow us to incorporate more types of content. For example, we will now be able to directly post videos without the need to put them into a Flash player. This will allow users to see the videos on devices that do not have a built-in Flash player. It will also provide better support for embedding questions or short quizzes into presentations. The new system will also allow us to upload more interactive presentations in non-Flash format, so that they can be viewed on devices like the iPad for instance. For those of you who currently access the system, you will see some new features.

- You will no longer need to enter the characters from the image "Captcha" at the login screen. We have implemented a more robust security system that invalidates the need for this second level of identification.
- In the new system, Workspaces will now be called Classrooms, and Courses will be called Classes. This will provide consistency between our public-facing system and the custom-built systems we operate.

For those of you who currently have accounts, you will receive an email message with some more details about the rollout and change over.

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).



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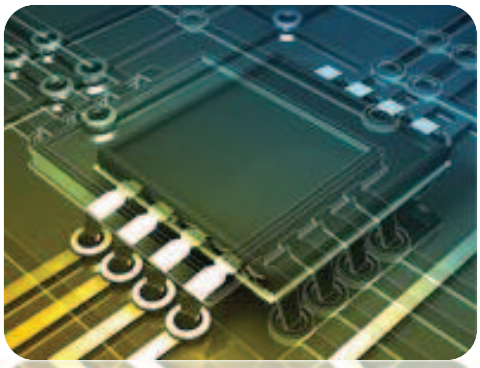

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If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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September 17 – 18, 2013 (Tue – Wed)
San Jose, California, USA

Reliability and Characterization Challenges for Advanced Semiconductor Devices
September 23 – 24, 2013 (Mon – Tue)
Penang, Malaysia

IC Packaging Metallurgy
October 28 – 30, 2013 (Mon – Wed)
Penang, Malaysia

Advanced Thermal Management and Packaging Materials
November 19 – 20, 2013 (Tue – Wed)
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