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InfoTracks

Semitracks Monthly Newsletter

Analog Building Blocks

By Christopher Henderson

This month, we will continue our series of Feature Articles with further discussion of amplifier circuits by first, contrasting Class A amplifiers with Class AB amplifiers, then discussing Differential amplifiers and Source Cross-Coupled Pairs. But first, let's make a couple of statements about the Class B amplifier. The Class B amplifier, also referred to as the push-pull configuration, is an improvement over the Class A amplifier in that it has zero power dissipation with zero input signal. Furthermore, its efficiency can be as high as 80%, but there is a distortion effect near the zero-input voltage in the bipolar Class B amplifier. To remedy this, there is the Class AB amplifier, which reduces crossover distortion.

Now to contrast Class A amplifiers with Class AB amplifiers. In many instances, a designer would prefer an amplifier that doesn't dissipate large quantities of power to achieve high levels of performance. In the Class A amplifier on the left of Figure 1, the power dissipation increases as one tries to switch a capacitive load on V_{out} at higher frequencies. In other words, to switch V_{out} faster, M2 must draw more current, leading to higher power dissipation levels. The Class AB amplifier can help solve these problems. In the Class AB amplifier on the right of Figure 1, M1 and M2 can be biased using M4 and M5. M3 is simply a constant current source used to help bias M1 and M2 on. This configuration is useful as an output buffer in an

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operational amplifier. Note that the substrates of the NMOS transistors are tied to VSS while the n-wells of the PMOS transistors are tied to VDD.

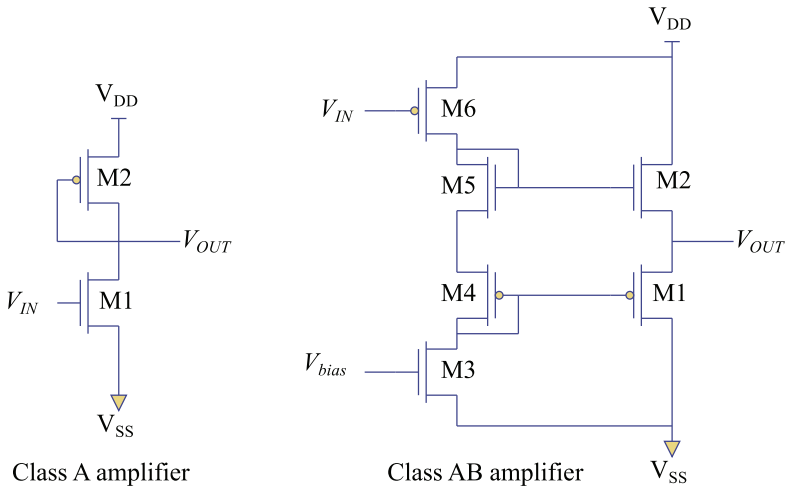


Figure 1. MOS amplifiers.

Let's now consider a class of amplifiers called differential amplifiers, of which we will discuss the CMOS (n-channel) and the CMOS (p-channel). These amplifiers amplify the difference between two signals, shown in Figure 2 as V_{IN1} and V_{IN2}. A basic differential amplifier can be constructed from a current source and a differential pair. In the example shown in Figure 2, the differential pair is a source-coupled pair, where the sources of M1 and M2 are tied together.

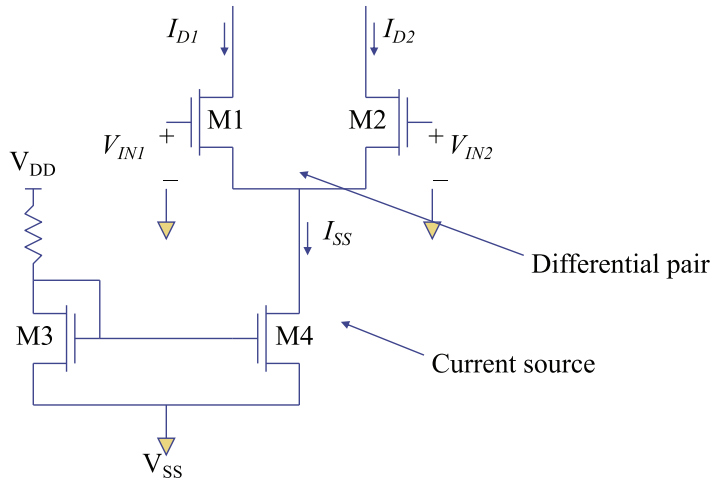


Figure 2. Differential amplifier example.

A CMOS differential amplifier is typically implemented as shown in Figure 3. The current sources (I_{D1} and I_{D2}) that we showed in Figure 2 are replaced with p-channel transistors M5 and M6 that produce the current for the circuit. We sometimes refer to this circuit as an n-channel differential amplifier.

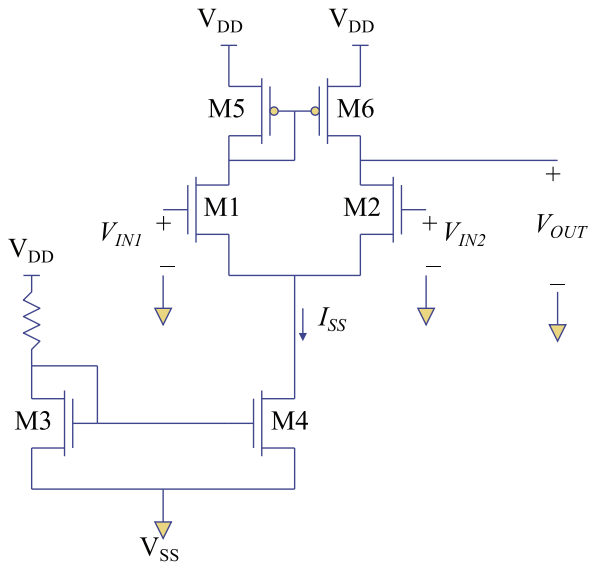


Figure 3. CMOS (n-channel) differential amplifier.

In Figure 4, we show a CMOS differential amplifier that uses the n-channel transistors as the amplification stage, and transistors M3 and M4 as the current load. We sometimes refer to this circuit as a p-channel differential amplifier.

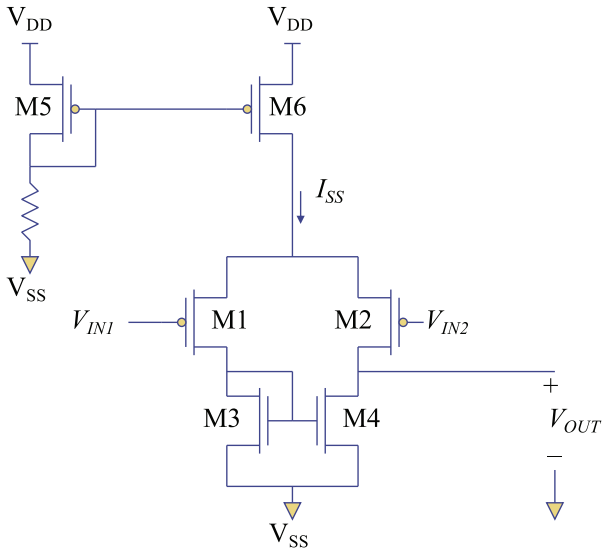


Figure 4. CMOS (p-channel) differential amplifier.

Now onto the Source Cross-Coupled Pair which is a commonly used amplifier in circuit design. One important characteristic of this amplifier design is that the circuit operates as a class AB amplifier where neither of the output currents is zero as long as their magnitudes remain less than ISS. In order that neither output current is zero, the maximum potential difference between the two inputs is the p-channel threshold voltage plus the n-channel threshold voltage minus the bias voltage on M8, as shown in Figure 5.

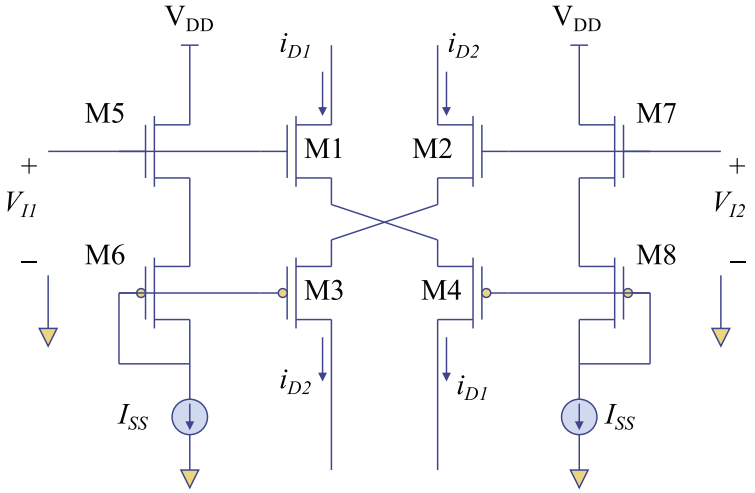


Figure 5. Source cross-coupled pair (n-channel inputs).

Figure 6 is a p-channel version of the Source Cross-Coupled Pair. A circuit designer will choose the p-channel version or the n-channel version based on the common mode range or CMR. The n-channel version has the best positive CMR, while the p-channel version has the best negative CMR.

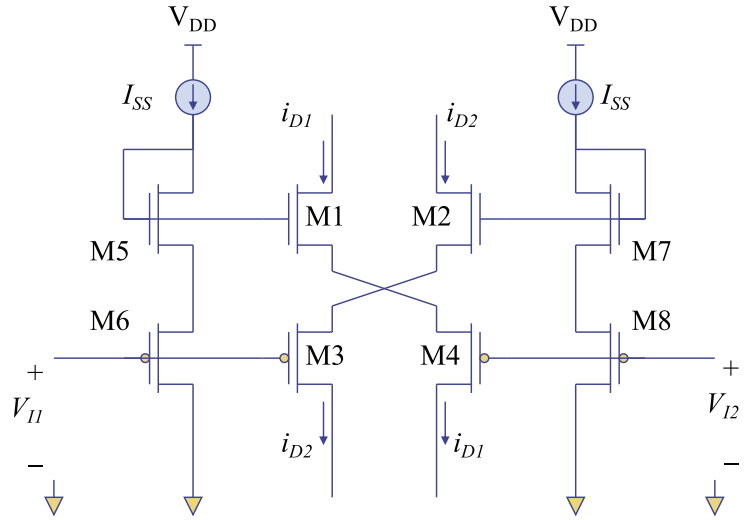


Figure 6. Source cross-coupled pair (p-channel inputs).

The circuit in Figure 7 represents a Source Cross-Coupled differential amplifier with active current loads. Transistors M9, M10, M11, and M12 form the active current loads. One can easily turn the output into a differential output by adding a pair of active loads at points A and B.

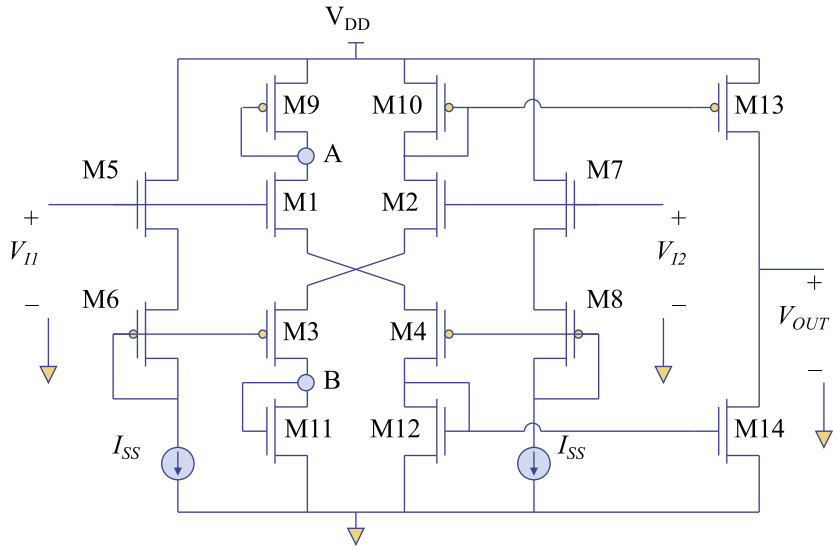


Figure 7. Source cross-coupled differential amplifier with active current loads.

In next month's Feature Article, we will conclude our discussion of amplifier circuits by examining operational amplifiers.

Technical Tidbit

Developing FIB Gas-Assisted Etching Recipes

This month's Technical Tidbit covers the development of focused ion beam gas-assisted etching recipes. In many ways, this activity tends to be done as an art by the FIB operator, rather than as a science. However, there are aspects of the process that can be quantitatively described, as we will see. First, we will discuss yield enhancement and the milling rate criteria for characterizing gas-assisted etching processes. Next, we will discuss choosing the appropriate beam raster parameters to maximize the milling rate. We will show some numerical and image examples, and then make some concluding remarks.

The existing theory for gas-assisted etching, or GAE, was developed with an emphasis of yield enhancement criteria. Researchers such as Edinger[1] and Utke[2], published work on this topic during the first decade of the 2000s. Typically, we wish to generate a milling rate that is suited for practical applications. Engineers desire recipes with maximized milling rates for high aspect ratio vias, as well as recipes with minimized milling rates for uniform deprocessing of copper with minimal dielectric over-etch. They also desire recipes with a high ratio of chemical milling to physical sputtering to deliver a high material selectivity.

To understand gas-assisted etching, let's start with the yield equation. The yield is given by

$$Yield = \frac{\frac{Removed\ Atoms}{Incident\ Ions}}{} = \frac{AR + AS}{Jt_D}$$

where AR (Atoms Reacted) – Fast, parameter sensitive, not limited by aspect ratio
AS (Atoms Sputtered) – Slow, limited by aspect ratio
J – Ion Beam Current Density
t_D – Time of beam dwell within the pixel

Table 1 describes the reactive yield versus mill parameters. The parameters and limits are listed in the top row, and the effect on the reactive yield (AR) is listed in the bottom row. As the pixel dwell decreases, the reactive yield increases. As the pixel overlap approaches zero, the reactive yield increases to a point, and then levels out. Similarly, as the pixel refresh increases, the reactive yield increases to a point, and then levels out.

Parameter and Limit	↓ Pixel Dwell 50 nsec	↓ Pixel Overlap ~0	↑ Pixel Refresh 1~10 mSec
Effect on AR (Reactive Yield)	↑	→	→

Table 1. Reactive yield versus mill parameters.

In the dwell point, where the ion beam strikes the surface, chemical reactions will occur on a picosecond scale. The FIB dwell times, however, are slower, on the order of tens to hundreds of nanoseconds. The equation below relates the dwell time to the reacted time and the sputtered time.

Essentially, the dwell time is the sum of the reacted and sputtered times. In a high-rate gas-assisted etching process, the dwell point requires the shortest possible dwell time that is practical. In other words, the dwell time converges to the atoms reacted time frame, and the atoms sputtered time converges to zero. From the perspective of the dwell point, the GAE process occurs within the dwell point, and the replenishment of the gas begins once the primary beam moves away from the dwell point. Therefore, the refresh time of each dwell, as opposed to the raster, is the parameter that is critical for gas replenishment. A raster time that is equivalent to the optimal refresh time will provide the most efficient GAE process.

$$t_{Raster} = t_{Refresh} = \sum_{i=0}^{n} t_{Di}$$

For modern FIBs, the practical minimum dwell time is in the range of 50 to 200 nanoseconds. This equation shows the number of dwell points as a function of the minimum dwell time and the refresh time.

$$N_{DP} = \frac{t_{Refresh}}{t_{D(Min.)}}$$

Another important factor is the size of the opening, or via, one plans to create. Dwell points will be desirable on the edges of the via. This equation shows the change in X, which will also be equivalent to the change in Y, as a function of the number of dwell points.

$$dX = dY = \frac{L}{\sqrt{(N)} - 1}$$

Therefore, the via size will define the dwell point distance. In order to ensure a high reactive yield, the beam diameter, D_{Beam}, will be equivalent to the pixel distance, or D_{Beam} = dX = dY. The corresponding beam current value will be controlled by the ion optics, and a diffused beam is desirable.

Let's now look at an example high aspect ratio recipe. If one mills a 2×2 µm via in silicon with chlorine for GAE and a refresh rate of 1 msec on a system with a minimal dwell time of 200 nsec, the optimal number of dwell points would be 1000 µsec divided by 200 nsec, or 5000 pixels per raster. From the previous equation, the optimal beam diameter would then be 2 µm divided by the square root of 5000 pixels per raster minus 1, which is approximately 30 nm. The corresponding beam current depends on the FIB system, but typically will be around 20 pA to 10 pA or even lower in some instances. The beam current can be increased for low (less than 5:1) aspect ratio work (e.g., surface micromachining)

Figure 1 shows the results from a specific instance use of the high aspect ratio recipe. The FIB image shows a cross-section through a high aspect ratio via using a needle gas injector system. The precursor gas is trifluoroacetic acid and the material being removed is silicon dioxide. The approximate etch time for this operation was 10 minutes, and the etch rate was approximately 0.6 µm/min for this via, which has close to a 10:1 aspect ratio.

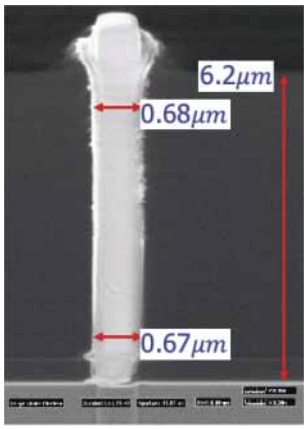


Figure 1. High Aspect Ratio via etching example.

Let's look at another example. Figure 2 shows the etch times for vias into a silicon dioxide layer with various dimensions, ranging from 0.5 µm down to 0.2 µm. There are two different dose configurations, labeled: "penta" and "beehive". The "beehive" dose is a flat 0.7 µm/min milling rate with a gas concentrator for aspect ratios from 10:1 up to 25:1. This work was performed on an FEI Vectra 986+ Focused Ion Beam system using xenon-difluoride for the gas assisted etching.

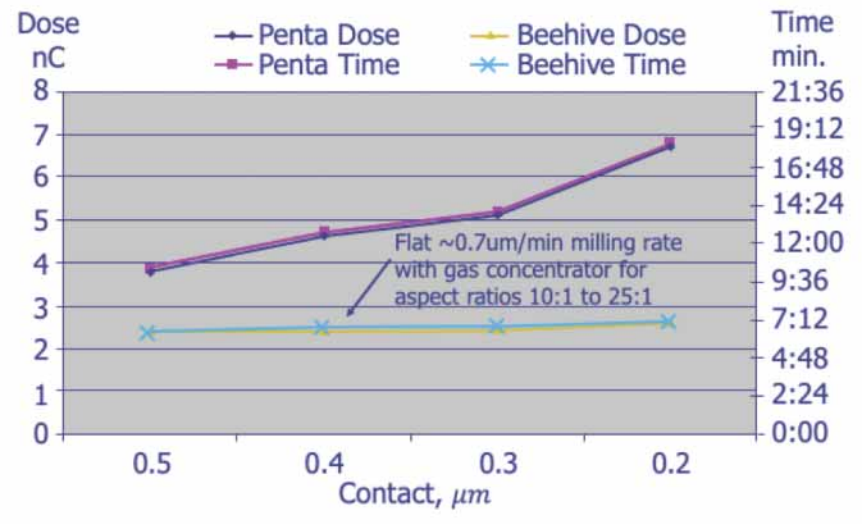


Figure 2. Etching times and doses as a function of contact size for two different dose configurations.

In conclusion, milling rate criteria is typically better suited to characterizing practical gas-assisted etching processes than simply using "engineering judgment". We reviewed the GAE milling rate criteria from the perspective of beam dwell point. This allows one to convert from a yield-based theory to rate-based practical applications. A rate-optimized GAE process establishes a direct relationship between the size of the repair and the beam diameter.

References:

1 K. Edinger, JVST B 18(6) 2000 and Microelectron. Eng. 57 – 58, 2001
2 I. Utke et. al. JVST B 26(4) 2008)

Ask the Experts

Q: What is the purpose of using only 2 metal layers as opposed to 6 metal layers?

A: Actually, the number of metal layers depends on how many transistors we need to wire together. For a chip with only a few transistors, like a Low Dropout Regulator (LDO) for example, only 1 or 2 layers of metal would be necessary. For a chip with hundreds of millions of transistors, like a special purpose microprocessor, it will take 6 or more layers to connect all of those transistors together. These transistors are simply too small and packed too close together to do it with only 1 or 2 metal lines.

Spotlight: IC Packaging Design and Modeling

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The industry is also pushing to use semiconductor devices in an increasing array of applications. To accomplish this, the industry is also driving prices down. This has created a number of challenges related to the packaging of these components. ***IC Packaging Design and Modeling*** is a 3-day course that offers detailed instruction on the design and modeling of semiconductor packages. We place special emphasis on package interactions with the die. This course is a must for every manager, engineer, and technician working in semiconductor packaging, using semiconductor components in high performance applications or non-standard packaging configurations, or supplying packaging tools to the industry.

By focusing on the fundamentals of packaging design and modeling, participants will learn why advances in the industry are occurring along certain lines and not others. Our instructors work hard to explain semiconductor packaging without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor packaging. This skill-building series is divided into four segments:

1. **Packaging Design Overview.** Participants learn the fundamentals of packaging design. They learn why modeling has become critical to semiconductor packaging for today's designs.

2. **Mechanical Simulations.** Participants learn the fundamentals of displacement, strain, stress, and energy. They learn how to leverage St. Venant's Principle and apply fracture mechanics to a problem.

3. **Thermal Simulations**. Participants learn heat transfer modeling. They also learn about steady-state and transient thermal modeling. The instructor also explains industry standard and compact thermal models.

4. **Modeling Semiconductor Packages.** Participants learn about the software used for modeling a variety of aspects of semiconductor packaging. They see a number of examples using current modeling tools used by Package Design experts.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of semiconductor packaging design and its technical issues.
2. Participants will understand the basic concepts behind thermal and mechanical simulations of packages.
3. The seminar will identify the key issues related to the continued growth of the semiconductor industry. This includes the need for high power dissipation, and designs that can mitigate the increasing fragility of the die because of low-k dielectrics.
4. The seminar offers a wide variety of sample modeling problems that participants work in class to help them gain knowledge of the fundamentals of packaging modeling.
5. Participants will be able to identify basic and advanced principles for mechanical stress and thermal diffusion.
6. Participants will understand how package reliability, power consumption and device performance are interrelated.
7. Participants will be able to make decisions about how to construct and evaluate new packaging designs and technologies.
8. Participants will also be introduced to wafer-level simulations, which are increasingly necessary with the advent of low-k dielectrics.

INSTRUCTIONAL STRATEGY

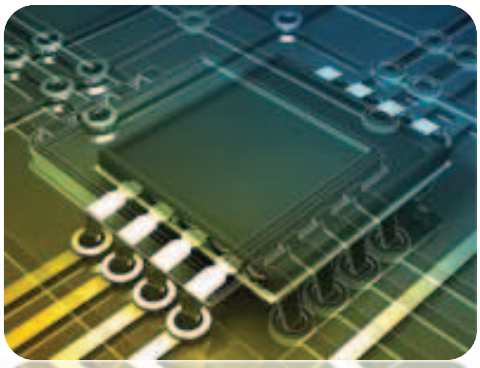
By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor packaging and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field.

COURSE OUTLINE

1. Package Design Principles
   a. Background
   b. ITRS Roadmap Issues
   c. JEDEC Standards for Packaging
   d. Semiconductor Package Designs: What is a Good Packaging Design?
   e. Modeling Software
2. Assembly and Packaging Processes
   a. Assembly and Packaging Processes
   b. Selecting Package Materials
   c. Advanced Packaging
   d. Stacked Die & Stacked Packages
   e. Through Silicon Via (TSV) Interconnects

3. Stress Simulations
    a. Solid Mechanics Concepts
        i. Basics of Displacement, Strain, Stress and Energy
        ii. Leveraging St. Venant's Principle
        iii. Applying Fracture Mechanics
    b. Manufacturability
        i. Thermomechanical Modeling Metrics
        ii. To Model or Not to Model
        iii. Assembly Process Simulations
4. Thermal Simulations
    a. Heat Transfer Principles
    b. JEDEC Thermal Test and Simulations
    c. Steady-State and Transient Thermal Modeling
    d. Application-Specific Thermal Simulations
    e. Using Compact Thermal Models
5. Reliability and Coupled Mechanics
    a. Thermomechanical Reliability
        i. Solder Joint Reliability (SJR)
        ii. Single Chip & Multiple Chip Package SJR
        iii. Solder Joint Shape Predictions
    b. Coupled Mechanics
        i. Moisture Diffusion
        ii. Plastic Package "Popcorn" Cracking
6. Wafer-Level Simulations
    a. Venturing into New Territory (Submodeling)
    b. Chip-Package Interactions
        i. Interfacial Fracture Mechanics
        ii. Bridging IC Interconnect and Package Gaps
    c. Microelectromechanical Systems (MEMS)
        i. Device Operations
        ii. MEMS Packaging

7. Drop Tests Simulations
   a. Drop Test & Structural Dynamics
   b. Solder Selection & Performance
      i. Leaded Solders
      ii. Lead-Free Solders
      iii. Surface Finishes, Solder Pastes, & Metallization
   c. Package Design Effects
      i. Stand-Off Heights
      ii. Ball Array Pattern
      iii. Single Chip & Multiple Chip Packages



Upcoming Webinars

(Click on each item for details)

Semiconductor Reliability / Product Qualification WEBINAR

4 sessions of 4 hours each
US: August 15 – 18, 2022 (Mon – Thur),
8:00 A.M. – 12:00 NOON PDT

Wafer Fab Processing WEBINAR

4 sessions of 4 hours each
US: October 3 – 6, 2022 (Mon – Thur),
8:00 A.M. – 12:00 NOON PDT

IC Packaging Design and Modeling WEBINAR

4 sessions of 4 hours each
US: October 10 – 13, 2022 (Mon – Thur),
8:00 A.M. – 12:00 NOON PDT

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We are always looking for ways to enhance our courses and educational materials.

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To post, read, or answer a question, visit our forums.
We look forward to hearing from you!