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Basic Failure Mechanisms

By Christopher Henderson

This month we continue our series of Feature Articles on Failure Mechanisms. In last month's Feature Article, we discussed Die Reliability-Related Failure Mechanisms. This month we discuss Package-Related Failure Mechanisms.

Package-Related Failure Mechanisms

Package failure mechanisms fall loosely into three categories: moisture-induced problems, thermomechanical stress-induced problems, and thermal degradation. We will also discuss tin whiskers, which is a packaging-related failure mechanism that does not fall cleanly into one of these three categories.

Moisture

Moisture can cause failures at the package exterior, package interior, or even at the die level. One of the big problems with moisture is the combination of moisture and a metal system that produces a galvanic reaction. Galvanic reactions are common with materials like tin, lead, copper, and silver. One example of a galvanic reaction is the occurrence of dendrites. Dendrites grow during the galvanic reaction process and form individual fern-like particles that extend out from the cathode metallization, as shown in Figure 1.

In this Issue:

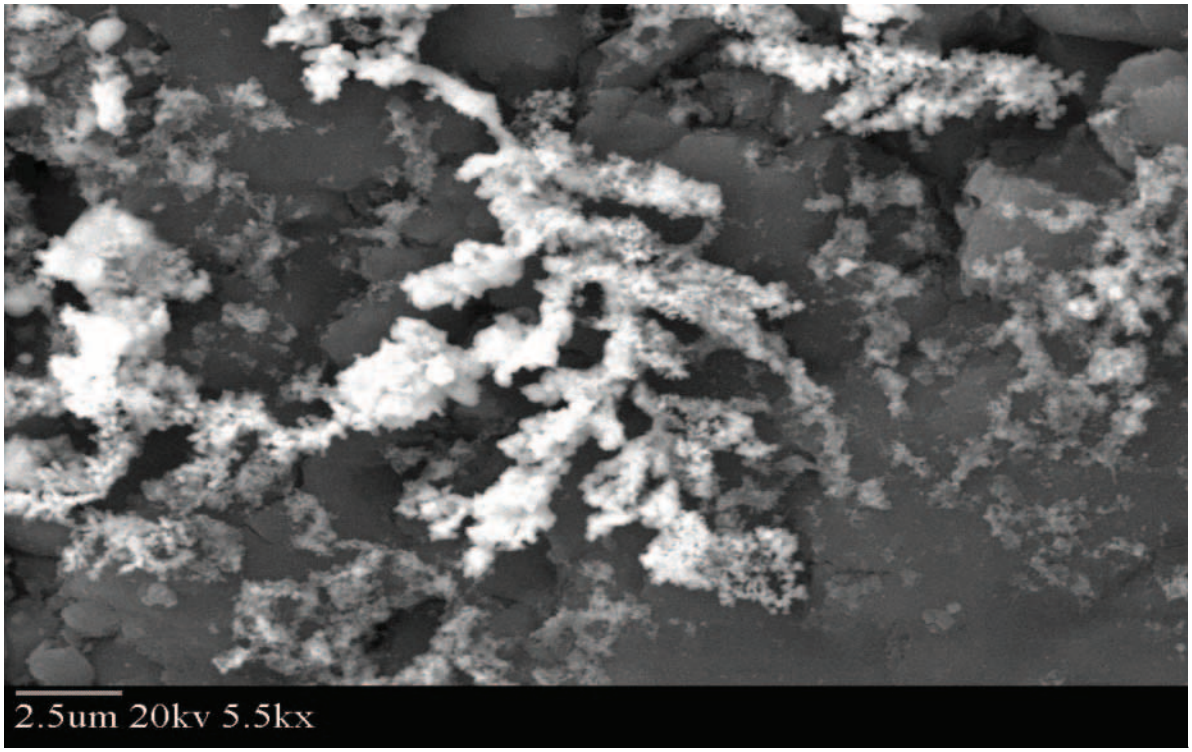

Figure 1. Silver dendrites on the surface of the package.

Additionally, moisture, in conjunction with a contaminant like chlorine or phosphorus, can drive a corrosion reaction, as shown in Figure 2. These reactions can occur at the leads of a package, the solder bumps, in the redistribution layer (if one exists), or on the die if metal is exposed. In general, plastic packages are more susceptible to these problems, as they have some permeability to moisture. The thinner the package, the faster moisture can penetrate to the die.

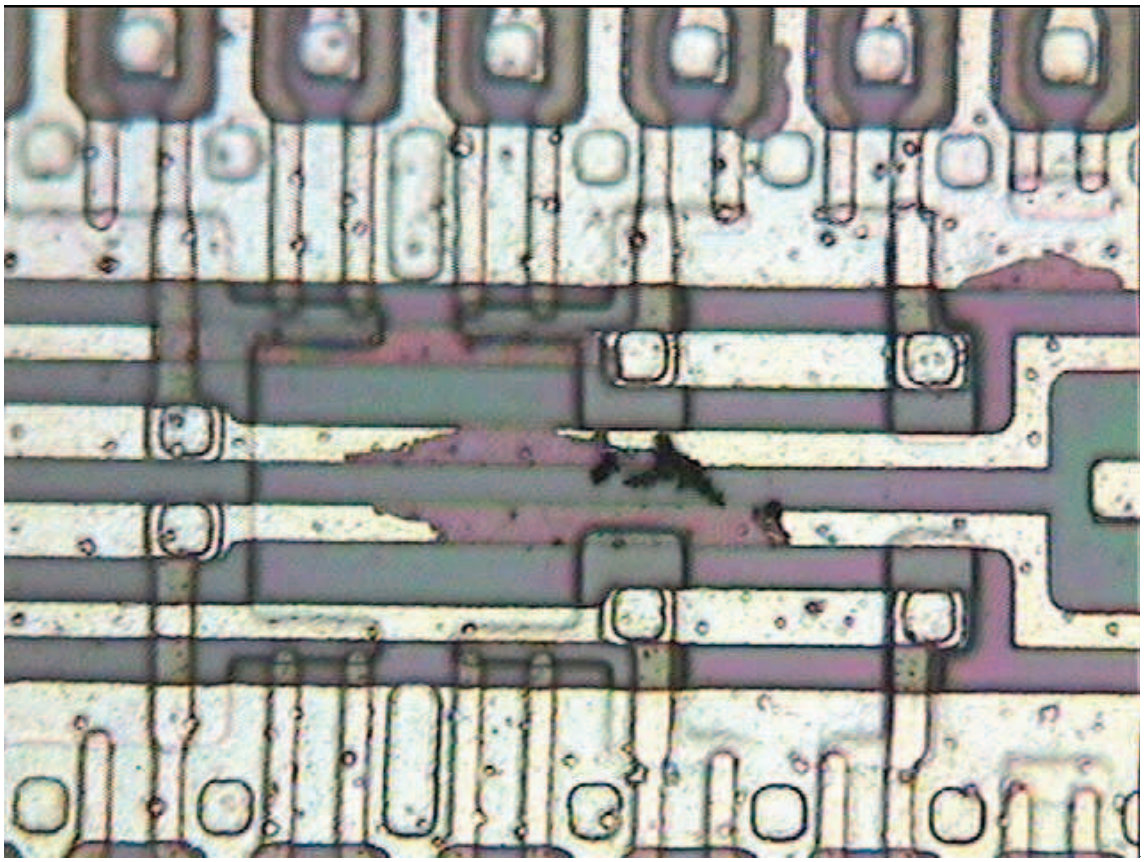

Figure 2. A metal corrosion reaction that dissolved the two horizontal aluminum interconnect lines in the center of the image, and damaged the thicker interconnect line in the upper-right hand portion of the image.

Thermomechanical Stress

Thermomechanical stress can lead to package cracking, die cracking, or other related problems like wire bond breakage or solder bump breakage. The coefficients of thermal expansion differ between the die, mold compound, and lead frame, setting up a condition where stress can occur. Thermal cycling exacerbates this stress; specifically, the lower temperature limit of the thermal cycling affects the extent of cracking. The lowest stress occurs at the same temperature as the epoxy cure temperature or close to the glass transition temperature of the epoxy.

One particular mechanism that involves both moisture and thermomechanical stress is popcorning. Moisture buildup at the die-mold compound or die paddle-mold compound interface can rapidly expand during solder reflow or burn-in, causing a delamination, as shown in Figure 3. The delamination can intersect with the bond wires or solder bumps, causing opens to occur. Popcorning is typically prevented by baking the component thoroughly prior to circuit board assembly.

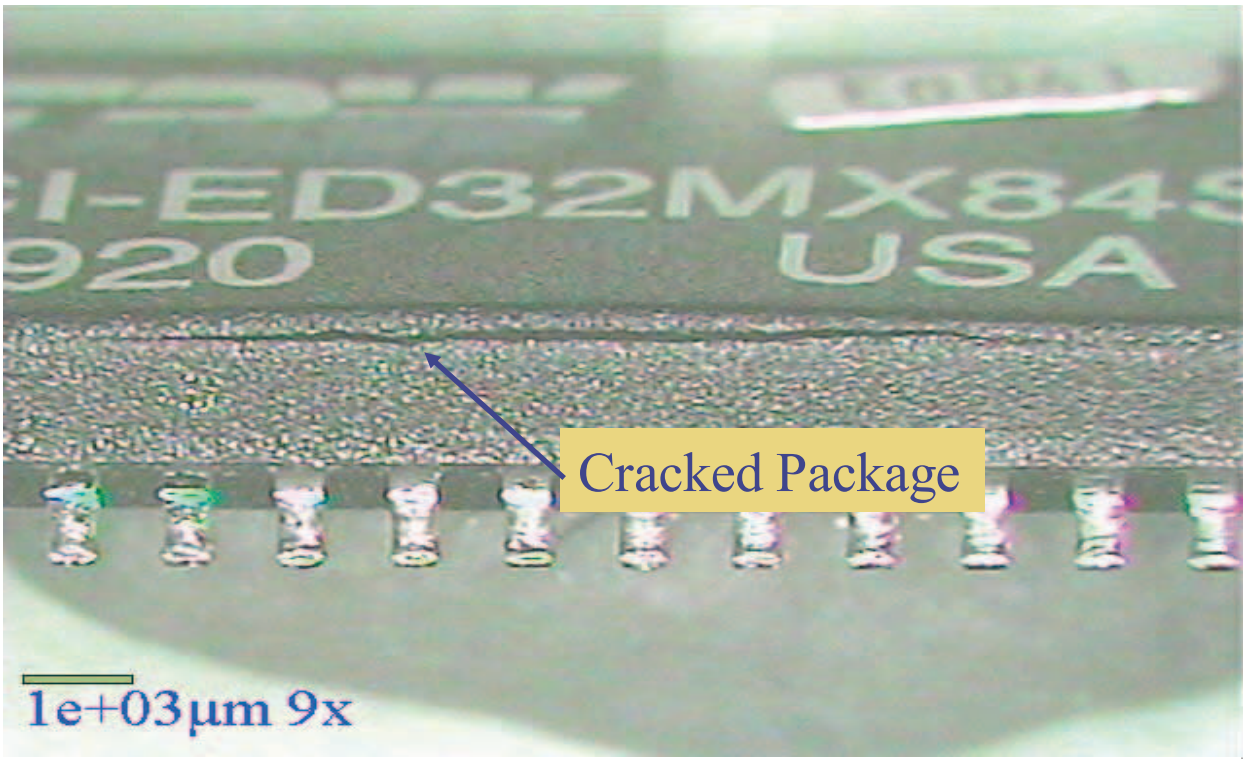

Figure 3. A cracked packaged caused by popcorning.

Thermal Degradation

Thermal degradation affects interfaces between materials systems. In particular, the aluminum-gold interface that occurs when gold wires are bonded to an aluminum bond pad is susceptible to thermal degradation. The gold diffuses more quickly into the aluminum than the aluminum diffuses into the gold, causing voids to occur, which can lead to wire bond failure. Another metal system susceptible to this degradation is the copper-tin system. The formation of copper-tin intermetallics can adversely affect the solderability of a component. These mechanisms are strongly accelerated by temperature, so avoiding high temperature bakes and prolonged baking times can mitigate the risk.

Tin Whiskers

Another common package-related failure mechanism is tin whiskers. As shown in Figure 4, tin whiskers result when leads plated with 100% tin are exposed to very high internal stress. Temperature cycling can cause additional stress on the package. To relieve the stress, a chemical reaction occurs, producing multiple single crystal "whiskers" from two to five millimeters long. The whiskers can cause pin-to-pin electrical shorts or break off inside the cavity of a device, causing intermittent electrical shorts.

Several methods to avoid tin whiskers include adding a small percentage of lead to the tin plating. Lead incorporated into the tin lattice reduces the stress and can prevent the mechanism. Alternatively, a hot oil bath can anneal the package, making it more resistant to stress.

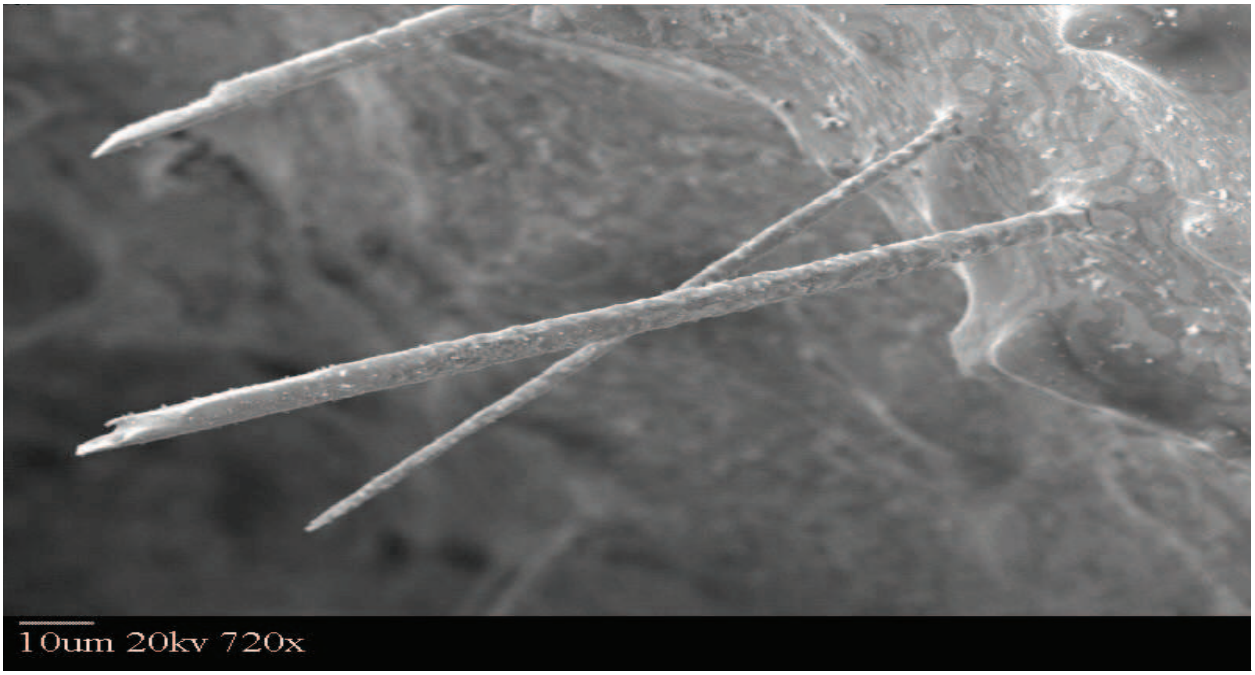

Figure 4. Tin whiskers caused by retained stress in a package with pins that are plated with 100% tin.

In next month's Feature Article, we will cover Use Condition Failure Mechanisms.

Technical Tidbit

Censored Data

This month's Technical Tidbit covers censored data. Engineers will sometimes obtain censored data when there is another effect overlapping the effect of interest one is trying to characterize.

Censoring is the convolution of results because of an unanticipated effect. This could be a second failure mechanism that interferes with the study of a failure mechanism of interest, or the inability to obtain correct data because of test length, equipment failure, or any one of a number of reasons. This Technical Tidbit will provide an awareness of the different types of lifetime data and how to deal with them.

Normally, when we determine the lifetime distribution through probability plotting, we assume that each failure is due to a single failure mode, and that we know the exact failure time. In many instances, however, this is not the case. We often encounter censoring, or a problem with our results. Sometimes the devices do not all fail during the test. Other times, we do not know the exact failure time, because it is impractical to monitor the devices in such a way as to obtain this information. Still other times we might encounter multi-censored data, where data exhibits different censoring times and readout intervals.

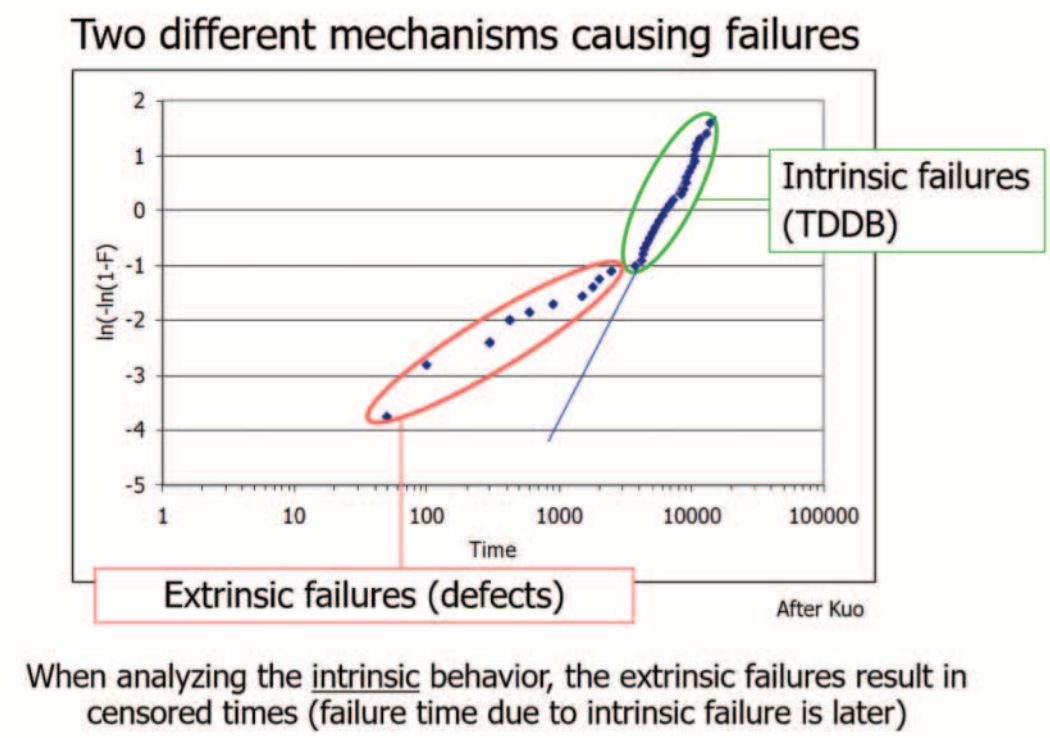

Figure 1. Graph showing a Weibull Probability Distribution of Failures after Reliability Stressing.

Figure 1 shows a classic example of censored data. In this probability plot we have a cluster of failures—circled in green—that falls along a Weibull slope associated with the intrinsic failure of an oxide due to time-dependent dielectric breakdown. Notice that we also have some failures—circled in red—that fail much earlier than the rest of the population. These are extrinsic failures due to defects in the oxide. When one attempts to analyze the intrinsic behavior, the extrinsic failures result in censored times. Notice that we can't draw a straight line through the extrinsic failure data points and have the intrinsic failures modeled correctly. These data points must be dealt with separately or they will convolute the main population results.

Ask the Experts

Q: Why is I_{eff} now used more than I_{dsat}?

A: I_{on} (or I_{dsat}) and I_{eff} are two different currents that reflect or represent the performance of a transistor. Generally, device physicists refer to I_{dsat} (which is I_{ds} at V_{DD} or the nominal supply voltage of the process node) when comparing transistor metrics. So, a transistor with I_{dsat} =1200 uA/um at 20nm is better than the one with I_{dsat} =1000 uA/um (assuming same leakage or I_{off}). However, this current is not useful to estimate circuit delay using the basic t_d=CV/I equation, where C= gate capacitance, V=supply voltage and I=current. This is because, in an inverter configuration, the current through the NMOS and PMOS never really reach I_{dsat}.

There was a very good paper from IBM that introduced this concept: http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=1175793.

The researchers estimated that the max current reached during inverter operation is the average of I_{high} and I_{low}, and using Ieff is a better metric to calculate inverter delay in a process node. Transistors with the same I_{dsat} can have different I_{eff}. For example, transistors with lower DIBL will have more I_{eff}, and the one with higher I_{eff} will result in lower delay/better performance. Hence I_{dsat} is not really the best metric, but I_{eff} is.

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Spotlight: Wafer Fab Processing

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. ***Wafer Fab Processing*** is a 4-day course that offers an in-depth look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we delve into the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the basics of each processing step and the issues surrounding them, participants will learn why certain techniques are preferred over others. Our instructors work hard to explain how semiconductor processing works without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Processing Steps.** Each processing step addresses a specific need in IC creation. Participants learn the fundamentals of each processing step and why they are used in the industry today.
2. **The Evolution of Each Processing Step.** It is important to understand how wafer fab processing came to the point where it is today. Participants learn how each technique has evolved for use in previous and current generation ICs.
3. **Current Issues in Wafer Fab Processing.** Participants learn how many processing steps are increasingly constrained by physics and materials science. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind the fundamental wafer fab processing steps.
3. The seminar will identify the key issues related to each of the processing techniques and their impact on the continued scaling of the semiconductor industry.
4. The seminar offers a wide variety of sample problems that participants work to help them gain knowledge of the fundamentals of wafer fab processing.
5. Participants will be able to identify the basic features and principles associated with each major processing step. These include processes like chemical vapor deposition, ion implantation, lithography, and etching.

6. Participants will understand how processing, reliability, power consumption and device performance are interrelated.
7. Participants will be able to make decisions about how to construct and evaluate processing steps for CMOS, BiCMOS, and bipolar technologies.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

COURSE OUTLINE

Day 1

1. Module 1: Basics & Fundamentals; Semiconductor Devices and ICs
    a. Acronyms
    b. Common Terminology
    c. Brief History
    d. Semiconductor Materials
    e. Electrical Conductivity
    f. Semiconductor Devices
    g. Classification of ICs & IC Processes
    h. Integrated Circuit Types
2. Module 2: Crystallinity, Crystal Defects, Crystal Growth
    a. Crystallinity
    b. Crystal Defects
    c. Crystal Growth
    d. Controlling Crystal Defects
3. Module 3: Basic CMOS Process Flow
    a. Transistors and Isolation
    b. Contacts/Vias Formation
    c. Interconnects
    d. Parametric Testing
4. Module 4: Ion Implantation 1 (The Science)
    a. Doping Basics
    b. Ion Implantation Basics
    c. Dopant Profiles
    d. Crystal Damage & Annealing

5. Module 5: Ion Implantation 2 (Equipment, Process Issues)
    a. Equipment
    b. Process Challenges
    c. Process Monitoring & Characterization
    d. New Techniques

Day 2

6. Module 6: Thermal Processing
    a. Overview of Thermal Processing
    b. Process Applications of SiO2
    c. Thermal Oxidation
    d. Thermal Oxidation Reaction Kinetics
    e. Oxide Quality
    f. Atomistic Models of Thermal Diffusion
    g. Thermal Diffusion Kinetics
    h. Thermal Annealing
    i. Thermal Processing Hardware
    j. Process Control
7. Module 7: Contamination Monitoring and Control
    a. Contamination Forms & Effects
    b. Contamination Sources & Control
    c. Contamination Characterization & Measurement
8. Module 8: Wafer Cleaning
    a. Wafer Cleaning Strategies
    b. Chemical Cleaning
    c. Mechanical Cleaning
9. Module 9: Vacuum, Thin Film, & Plasma Basics
    a. Vacuum Basics
    b. Thin Film Basics
    c. Plasma Basics
10. Module 10: CVD 1 (Basics, LPCVD, Epitaxy)
    a. CVD Basics
    b. LPCVD Films
    c. LPCVD Equipment
    d. Epi Basics
    e. Epi Process Applications
    f. Epi Deposition Process
    g. Epi Deposition Equipment

Day 3

11. Module 11: PVD
    a. PVD (Physical Vapor Deposition) Basics
    b. Sputter Deposition Process
    c. Sputter Deposition Equipment
    d. Al-Based Films
    e. Step Coverage and Contact/Via Hole Filling
    f. Metal Film Evaluation
12. Module 12: Lithography 1 (Photoresist Processing)
    a. Basic Lithography Process
    b. Photoresist Materials
    c. Photoresist Process Flow
    d. Photoresist Processing Systems
13. Module 13: Lithography 2 (Image Formation)
    a. Basic Optics
    b. Imaging
    c. Equipment Overview
    d. Actinic Illumination
    e. Exposure Tools
14. Module 14: Lithgroaphy 3 (Registration, Photomasks, RETs)
    a. Registration
    b. Photomasks
    c. Resolution Enhancement Techniques
    d. The Evolution of Optical Lithography
15. Module 15: Etch 1 (Basics, Wet Etch, Dry Etch)
    a. Etch Basics
    b. Etch Terminology
    c. Wet Etch Overview
    d. Wet Etch Chemistries
    e. Types of Dry Etch Processes
    f. Physics & Chemistry of Plasma Etching

Day 4

16. Module 16: Etch 2 (Dry Etch Applications and Equipment)
    a. Dry Etch Applications
    b. SiO2
    c. Polysilicon
    d. Al & Al Alloys
    e. Photoresist Strip
    f. Silicon Nitride
    g. Dry Etch Equipment
    h. Batch Etchers
    i. Single Wafer Etchers
    j. Endpoint Detection
    k. Wafer Chucks
17. Module 17: CVD 2 (PECVD)
    a. CVD Basics
    b. PECVD Equipment
    c. CVD Films
    d. Step Coverage
18. Module 18: Chemical Mechanical Polishing
    a. Planarization Basics
    b. CMP Basics
    c. CMP Processes
    d. Process Challenges
    e. Equipment
    f. Process Control
19. Module 19: Copper Interconnect, Low-k Dielectrics
    a. Limitations of "Conventional" Interconnect
    b. Copper Interconnect
    c. Cu Electroplating
    d. Damascene Structures
    e. Low-k IMDs
    f. Cleaning Cu and low-k IMDs

20. Module 20: Leading Edge Technologies & Techniques
    a. Process Evolution
    b. Atomic Layer Deposition (ALD)
    c. High-k Gate and Capacitor Dielectrics
    d. Ni Silicide Contacts
    e. Metal Gates
    f. Silicon on Insulator (SOI) Technology
    g. Strained Silicon
    h. Hard Mask Trim Etch
    i. New Doping Techniques
    j. New Annealing Techniques
    k. Other New Techniques
    l. Summary of Industry Trends

References:

Wolf, Microchip Manufacturing,
Doering & Nishi, Semiconductor Manufacturing Technology, 2nd ed.
Wolf, Silicon Processing, Vol. 4
Wolf, Silicon Processing, Vol. 1, 2nd ed.

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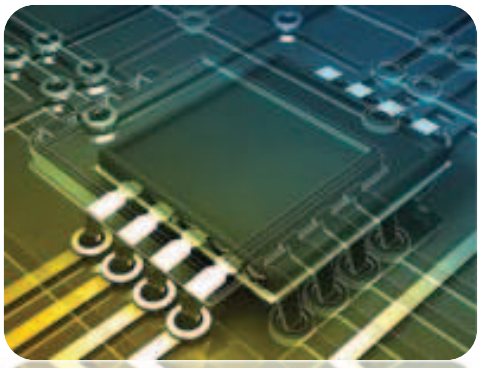

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4 sessions of 4 hours each
Europe: August 30 – September 2, 2021
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