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Reliability Test Equipment: Wafer Level, Part 3

By Christopher Henderson

In Part 3, we will conclude our discussion of reliability test equipment. The appropriate test equipment is essential for conducting reliability studies. In addition, one must know how to set up the equipment and understand issues related to cabling, noise, and long-term testing.

Figure 10. Illustrations of wafer probe systems.

Another major component of a reliability test system is the probe system. Probe systems fall loosely into two main categories: automated and semi-automated/manual systems. There are actually dozens of probe station manufacturers, but we don't have time to discuss each manufacturer in this section, so we'll discuss a few of the leading manufacturers. Several manufacturers make both automated and manual systems. Under the category of automated, we'll discuss

In this Issue:

Accretech, Electroglas, Tokyo Electron, and FormFactor. Under semi-automated and manual, we'll discuss Micromanipulator, Suss MicroTec, and Signatone.

Figure 11. Illustration of Accretech-TSK automated probe system.

Accretech-TSK is the leader in automated probe systems. Their systems, shown Figure 11, are used primarily for wafer-level testing for sort and automated test structure probing. Electroglas systems can handle 150, 200, and 300 mm wafers with stepping accuracies of 1.5 µm across a 300 mm wafer. The probe to pad accuracy is 1.5 µm. The system is computer-controlled. Systems can also be purchased with contamination free enclosures. This can be particularly useful for MEMS devices, as well as inline probing with the standard wafer process flow.

Figure 12. Illustration of Tokyo Electron automated probe system.

Tokyo Electron is another big supplier of probing systems. Figure 12 is an example of one of their setups. It can do ultra-high-speed testing, as well as DC and parametric testing.

Figure 13. Illustration of FormFactor automated probe system.

FormFactor is another leader in automated probing. Their systems can handle 75 to 300 mm wafers. The systems come with optional thermal chucks for probing at temperatures ranging from -55°C to +200°C. These systems can be docked with a wide variety of automated wafer-level reliability test systems, including Agilent 4060, 4070 and 4080 series systems, and Keithley S600, 4200, and ACS series systems. They can also be used in conjunction with custom systems, like the one shown here in Figure 13 based on the Agilent 4145 parametric analyzer.

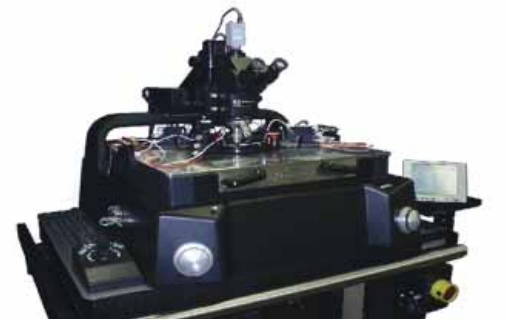
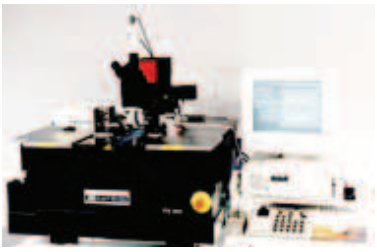


Figure 14. Illustration of Micromanipulator P300A semi-automatic probe system.

In the semiautomatic and manual arena, Micromanipulator is a leader. Micromanipulator sells a variety of manuals that can handle 150, 200, and 300 mm wafers. Some systems can be controlled via a PC. The 300 mm semi-automatic system shown here in Figure 14 has integrated vibration isolation for stable, long-term measurements. It has an integrated dark and dry environment for protection against the effects of stray light during probe and moisture when probing at cold temperatures. It has a high precision, high resolution drive for accurate probe placement. It also has an open platen to allow for flexibility when setting up probes or probe cards. Micromanipulator offers other systems that can be manually positioned. Manual positioning tends to be useful for failure analysis applications, or one-off reliability measurements.

Karl Suss Model PA-300



Signatone Model CM-100

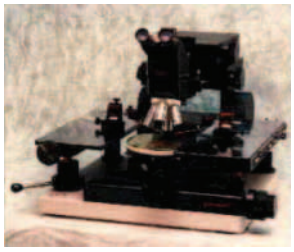


Figure 15. Illustrations of Suss MicroTec and Signatone probe systems.

Other players in the semi-automated and manual market include Suss MicroTec, and Signatone. Both of these companies, like Micromanipulator, offer a variety of models (as shown in Figure 15) that can handle wafer sizes up to 300 millimeters.

Figure 16. Illustrations of other manufacturers' probe stations.

There are other manufacturers in this area, including Probing Solutions, Wentworth, Alessi, Rucker & Kolls, Gigatest Labs, and many more. See Figure 16 for examples.

When choosing a probe station or prober, one must consider the application. There are several key factors of which one should be aware. The first is mechanical precision. This requires both accuracy and repeatability of probe placement. The next is mechanical stability. The system should have sufficient mass to help prevent shifting, and should be designed in such a way to reduce internal vibrations and prevent the coupling of mechanical vibrations from the outside environment. The system should exhibit thermal stability. There should be no movement of the wafer relative to the probes during operation. Finally, the probe station should exhibit good electrical performance. The two main concerns with the station itself are the isolation of the chuck from the station and resistance to noise coupling.

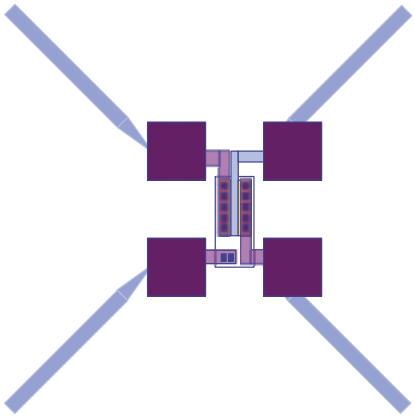


Figure 17. Mechanical precision.

Let's discuss mechanical precision in more detail. If one plans to perform automated measurements across multiple die sites or wafers, the system must be able to accurately place the probes on the pads. Most bond pads are 20 × 20 μm^2 or larger, but may be smaller in certain applications. This means that one would like the probe station to exhibit better than 5 µm accuracy across the wafer. Larger errors can result in a lack of contact to the structure and potential damage. This capability is more important for large wafers, where the errors are likely to be larger. Included in mechanical precision is the error generated by loading and unloading wafers from the chuck. Significant errors, like the one shown here in Figure 17, can result in a lack of contact and potential damage also.

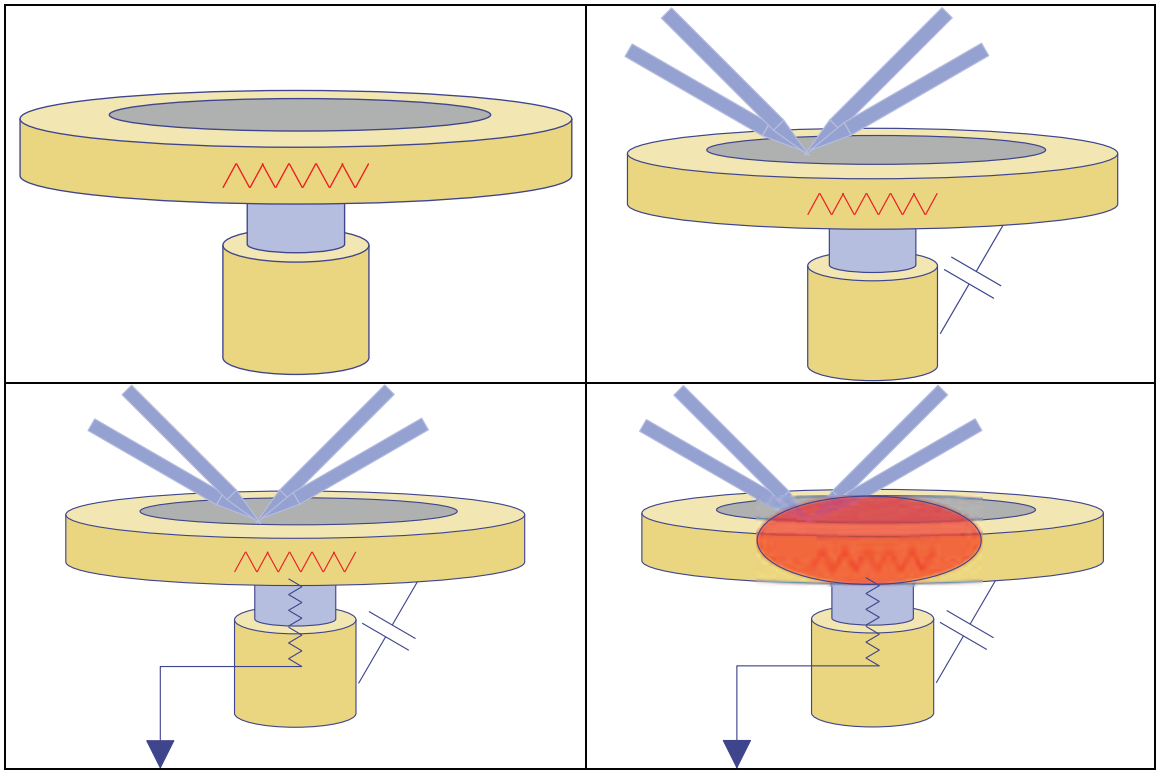


Figure 18. Illustration of electrical performance.

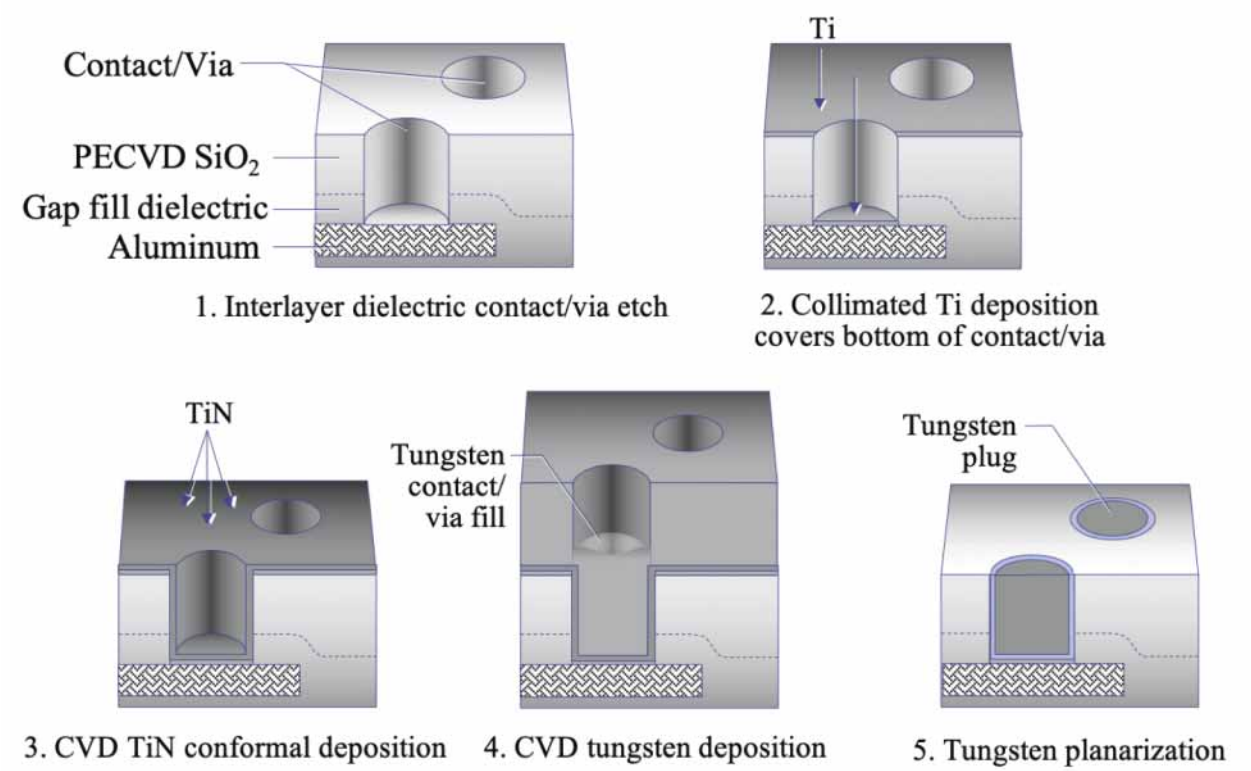
Electrical performance is another key aspect of a probe station. There should be good isolation between the chuck and the probe station body (Figure 18, top left). There should not be any capacitive coupling of signals from the station into the chuck (Figure 18, top right). If the chuck is grounded, then there should be a solid, low resistance connection to ground (Figure 18, bottom left). If one is using a thermal chuck, the heating elements should not generate electrical signals that can couple to the wafer and into the measurement (Figure 18, bottom right).

This concludes our discussion of reliability test equipment. For more information on this subject, you may want to consider subscribing to our Online Training System.

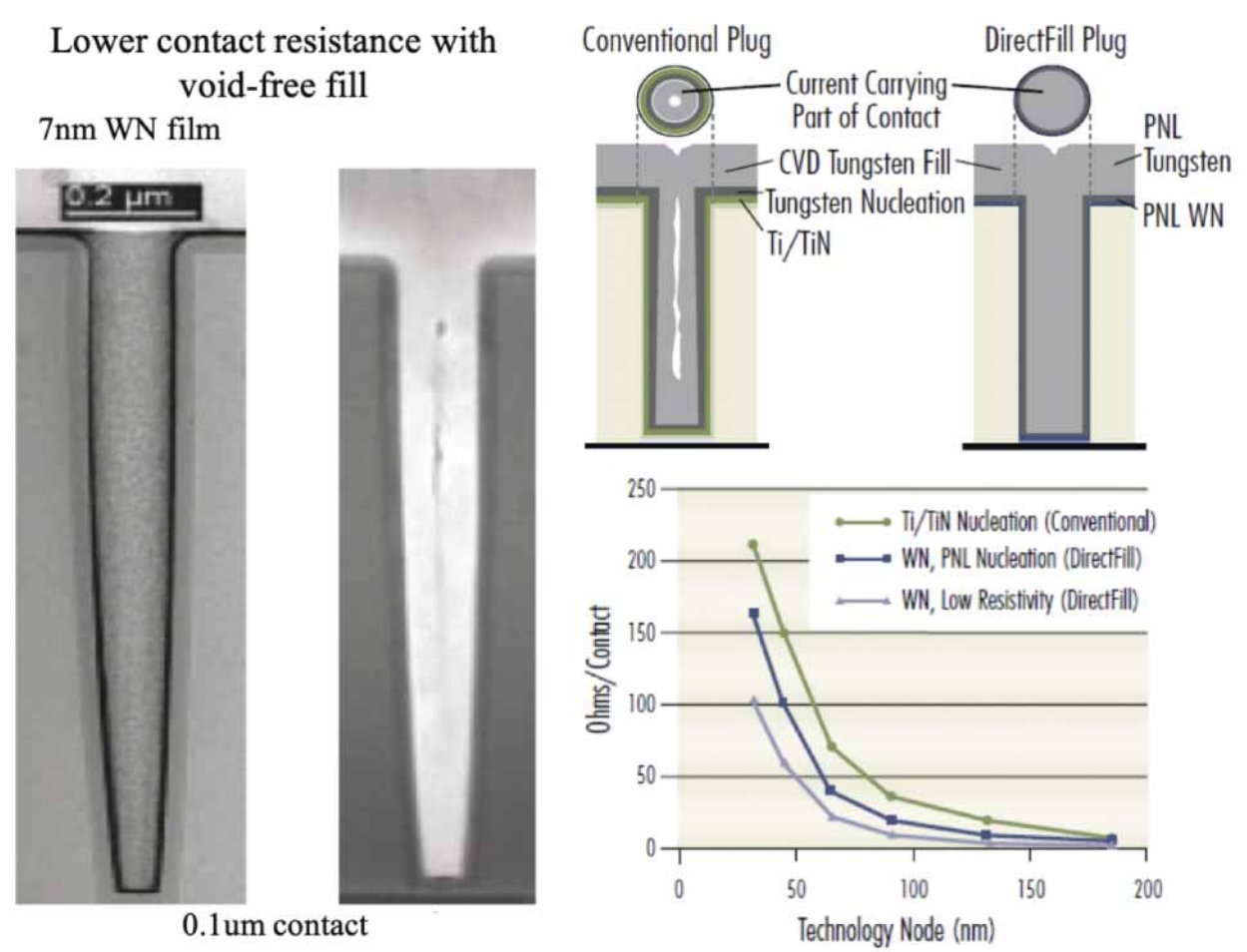
Technical Tidbit

Contact and Via Process

In this month's technical tidbit, we will review the basic process for creating contacts and vias.



For the purpose of this article, we will focus on the tungsten contact/via process more closely. With tungsten, the contact and via processes are quite similar, so we'll discuss them as one process. First, we etch through the dielectric layer, either pre-metal dielectric directly on the silicon surface, or the plasma-enhanced (PECVD) dielectric that separates metal layers. We use a reactive ion etch for this process. Next, we deposit titanium using a collimated physical vapor deposition process that covers the bottom of the contact or via. Next, we use physical vapor deposition to conformally deposit titanium-nitride on the sidewalls and bottom of the contacts or vias. We then use chemical vapor deposition to deposit tungsten into the contacts or vias. Finally, we use chemical mechanical planarization to remove the overlying tungsten and titanium-nitride layers, leaving the metals only in the contacts or vias.



Tungsten is a commonly used material for making contacts. Tungsten and tungsten-nitride films can be conformally deposited, even in high-aspect ratio vias and contacts. This leads to better fill characteristics and lower resistances like we show in the TEM images on the left, and the diagrams on the right. One method for lowering the resistance is a technique called Pulse Nucleation Layer, or PNL, deposition. This creates a lower resistance connection, like we see in the graph at the lower right. However, there are still concerns about contacts and vias. As we scale feature sizes down, there is more barrier layer, more grain boundary scattering, and more voiding. The aspect ratio of the vias or contacts also plays an important role in the development of voids. Voids are more likely to form the higher the aspect ratio is. Variations in critical dimensions would impact void formation as well.

Ask the Experts

Q: I am having problems with voiding in my tungsten contacts. What might be causing this, and what can I do to stop them?

A: Sometimes, cleaning steps can create this problem indirectly. Voids sometimes appear after an ammonium hydroxide cleaning step, just after CMP. Additional cleaning steps, sometimes used to better remove particles and debris from the CMP process, actually make the voiding problem worse in some instances. Also, using an ionized physical vapor deposition process creates a thick titanium liner, which creates poor tungsten fill properties, but using an RF physical vapor deposition process, the titanium liner is thinner, leading to better tungsten fill properties. Another step that can reduce the tungsten voiding process is an oxygen plasma ashing step to oxidize the surface of the tungsten. This protects the remaining tungsten during the wet clean process associated with the contact etches to the drain/source regions, as well as to the gates.

Spotlight: IC Packaging Technology

OVERVIEW

Overview: Integrated Circuit packaging has always been integral to IC performance and functionality. An IC package serves many purposes: (1) pitch conversion between the fine features of the IC die and the system level interconnection, (2) chemical, environmental and mechanical protection, (3) heat transfer, (4) power, ground and signal distribution between the die and system, (5) handling robustness, and (6) die identification among many others. Numerous critical technologies have been developed to serve these functions, technologies that continue to advance with each new requirement for cost reduction, space savings, higher speed electrical performance, finer pitch, die surface fragility, new reliability requirements, and new applications. Packaging engineers must fully understand these technologies to design and fabricate future high-performance packages with high yields at exceptional low-costs to give their company a critical competitive advantage.

This two-day class will detail the vital technologies required to construct IC packages in a reliable, cost effective, and quick time to market fashion. When completed, the participant will understand the wide array of technologies available, how technologies interact, what choices must be made for a high-performance product vs. a consumer device, and how such choices impact the manufacturability, functionality, and reliability of the finished product. An emphasis will be given to manufacturing, processes and materials selection tailoring and development. Each fundamental package family will be discussed, including flip chip area array technologies, Wafer Level Packaging (WLP), Fan-Out Wafer Level Packaging (FO-WLP), and the latest Through Silicon Via (TSV) developments. Additionally, future directions for each package technology will be highlighted, along with challenges that must be surmounted to succeed.

WHAT WILL I LEARN BY TAKING THIS CLASS?

1. **Molded Package Technologies.** Participants learn the fundamentals of molding critical to leaded, leadless, and area array packaging, enabling them to eliminate problems such as flash, incomplete fill, and wire sweep.
2. **Flip Chip Technologies.** Participants learn the fundamentals of plating, bumping, reflow, underfill, and substrate technologies that are required for both high performance and portable products.
3. **Wafer Level Packages.** Participants learn the newest technologies that enable the increasingly popular Wafer Chip Scale Level Packages (WCSPs) and Fan-Out Wafer Level Packages (FO-WLPs).
4. **Through Silicon Via Packages and Future Directions.** Participants will know the latest advances in the recently productized TSV technology, as well as future directions that will lead to the products of tomorrow.

COURSE OBJECTIVES

1. The course will supply participants with an in-depth understanding of package technologies current and future.
2. Potential defects associated with each package technology will be highlighted to enable the student to identify and eliminate such issues in product from both internal assembly and OSAT houses.

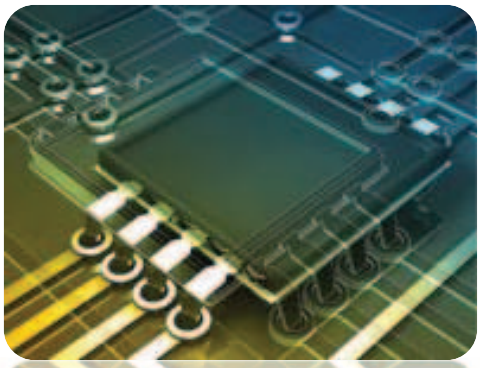
3. Cu and solder plating technologies will be described with special emphasis on package applications in TSVs and Cu pillars for FO-WLPs. Emphasis will be placed on eliminating issues such as reliability, non-uniformity, void free thermal aging performance, and contamination free interfaces.
4. New package processes employed in Through Silicon Via production will be described, along with current cost reduction thrusts, to enable the student to understand the advantages and limits of the technologies.
5. Temporary bonding and wafer thinning processes will be highlighted, as well as the cost reduction approaches currently being pursued to enable wider adoption of TSV packages.
6. The trade-offs between silicon, glass, and organic interposers will be highlighted, along with the processes used for each.
7. Participants will gain an understanding of the surface mount technologies that enable today's fine pitch products.
8. The class will provide detailed references for participants to study and further deepen their understanding.

COURSE OUTLINE

1. The Package Development Process as a Package Technology:
   a. Materials and Process Co-Design
2. Molded Package Technologies:
   a. Die Attach
      i. Plasma Cleans
   b. Wire Bonding
      i. Au vs. Cu vs. Ag
      ii. Die Design for Wire Bonding
   c. Lead Frames
   d. Transfer and Liquid Molding
      i. Flash
      ii. Incomplete Fill
      iii. Wire Sweep
      iv. Green Materials
   e. Pre- vs. Post-Mold Plating
   f. Trim Form
   g. Saw Singulation
   h. High Temperature and High Voltage Materials
3. Flip Chip and Ball Grid Array Technologies:
   a. Wafer Bumping Processing
      i. Cu and Solder Plating
      ii. Cu Pillar Processing
   b. Die Design for Wafer Bumping
   c. Flip Chip Joining
   d. Underfills
   e. Substrate Technologies
      i. Surface Finish Trade-Offs
      ii. Core, Build-up, and Coreless

f. Thermal Interface Materials (TIMs) and Lids
g. Fine Pitch Warpage Reduction
h. Stacked Die and Stacked Packages
i. Material Selection for Board Level Temperature Cycling and Drop Reliability

4. Wafer Chip Scale Packages:
   a. Redistribution Layer Processing
   b. Packing and Handling
   c. Underfill vs. No-Underfill
5. Fan-Out Wafer Level Packages:
   a. Chip First vs. Chip Last Technologies
   b. Redistribution Layer Processing
   c. Through Mold Vias
6. Through Silicon Via Technologies:
   a. Current Examples
   b. Fundamental TSV Process Steps
      i. TSV Etching
      ii. Cu Deep Via Plating
      iii. Temporary Carrier Attach
      iv. Wafer Thinning
   c. Die Stacking and Reflow
   d. Underfills
   e. Interposer Technologies: Silicon, Glass, Organic
7. Surface Mount Technologies:
   a. PCB Types
   b. Solder Pastes
   c. Solder Stencils
   d. Solder Reflow



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Upcoming Courses

(Click on each item for details)

Semiconductor Reliability / Product Qualification
April 6 – 9, 2021 (Tue – Fri)
Munich, Germany

Wafer Fab Processing
April 6 – 9, 2021 (Tue – Fri)
Munich, Germany

Failure and Yield Analysis
April 12 – 15, 2021 (Mon – Thur)
Munich, Germany

IC Packaging Technology
April 19 – 20, 2021 (Mon – Tue)
Munich, Germany

Advanced CMOS/FinFET Fabrication
April 22, 2021 (Thur)
Munich, Germany