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Semitracks Monthly Newsletter

Random Diffusion Masking Defect

By Christopher Henderson

In this article we will discuss a failure mechanism that has been around for as long as the semiconductor lithography process – the mask defect. To focus our discussion, let's take a specific type of masking defect, the diffusion masking defect. A random diffusion defect can cause areas of extra diffusion or missed diffusion, associated with the photo masking process. It often results in a wide range of device level problems including leakages between diffusions, open resistors, and faulty transistors, which cause functional and parametric defects. Any defect on the mask or pellicle, which alters the pattern, such as a scratch or contaminant, can cause these issues. It may also be caused by a defect in the patterned photoresist from scratches, or particles in, on, or under the resist.

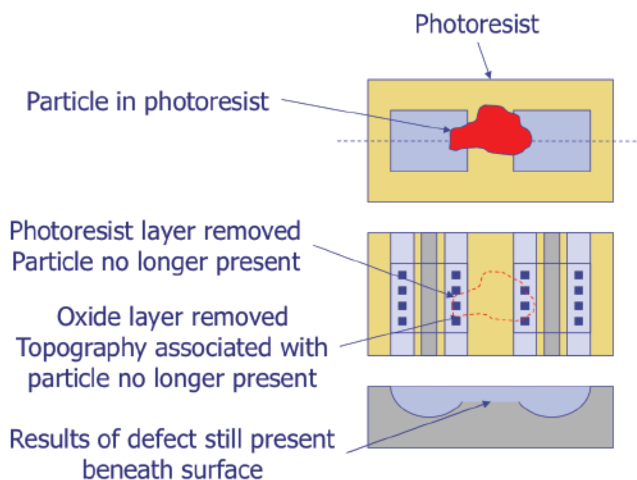

Figure 1. Cross section of particle effects.

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The anomalous pattern may or may not be apparent from visual inspection. In many semiconductor technologies, diffusion and implant defects are normally not visible because photoresist, rather than oxide, serves as the mask. Therefore, there is no imprint of the mask after the resist is removed. Almost all CMOS and many junction isolated bipolar processes strip and regrow the oxide layers after the isolation or base implant or diffusion steps and obscure defects at prior masks. However, when viewed in cross-section, the effects of the particle are still present. The defect may still be detected by a slight depression in the silicon (from silicon consumed during oxide growth) or a slightly different oxide thickness (from oxide growing faster over more heavily doped regions). Similarly, the mask which opens oxide holes for the source, drain, or emitter implant or diffusion will obscure base masking defects that might be present under the emitter. For instance, a pinhole defect in a negative resist base photo mask will leave a spot of oxide inside the base diffusion opening and will create a location where base dopant is blocked. If this defect is in an area designated to be an emitter, the subsequent emitter oxide opening step will remove the residual base oxide and make it difficult to spot the defect visually.

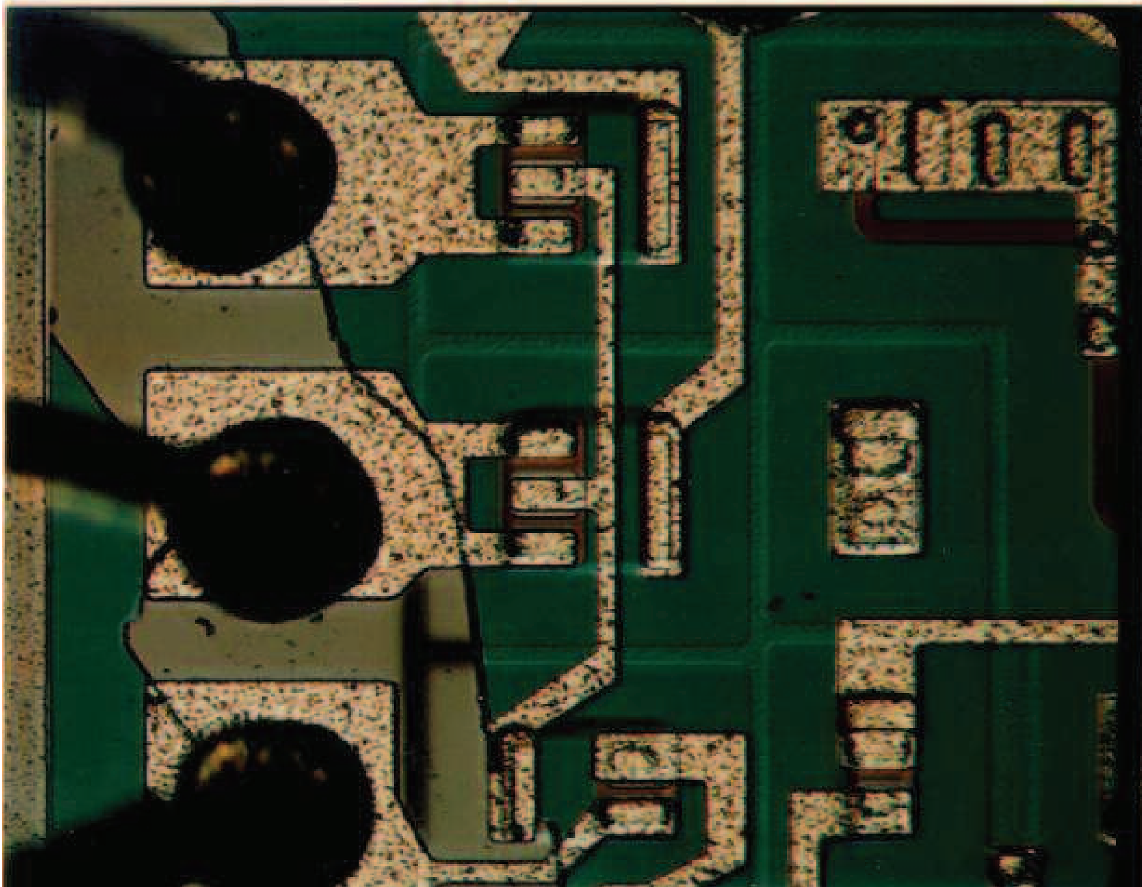


Figure 2. Random diffusion masking defect failure mechanism.

Figure 2 shows the random diffusion masking defect failure mechanism. A random diffusion-masking defect can cause areas of extra diffusion or missed diffusion associated with the photo masking process. It can result in a wide range of device level problems, including leakages between diffusions, open resistors, faulty transistors, causing functional and parametric defects. It can be caused by any defect on the mask or pellicle which alters the pattern, such as a scratch or contaminant. It may also be caused by a defect in the patterned photoresist from scratches, or particles in, on, or under the resist.

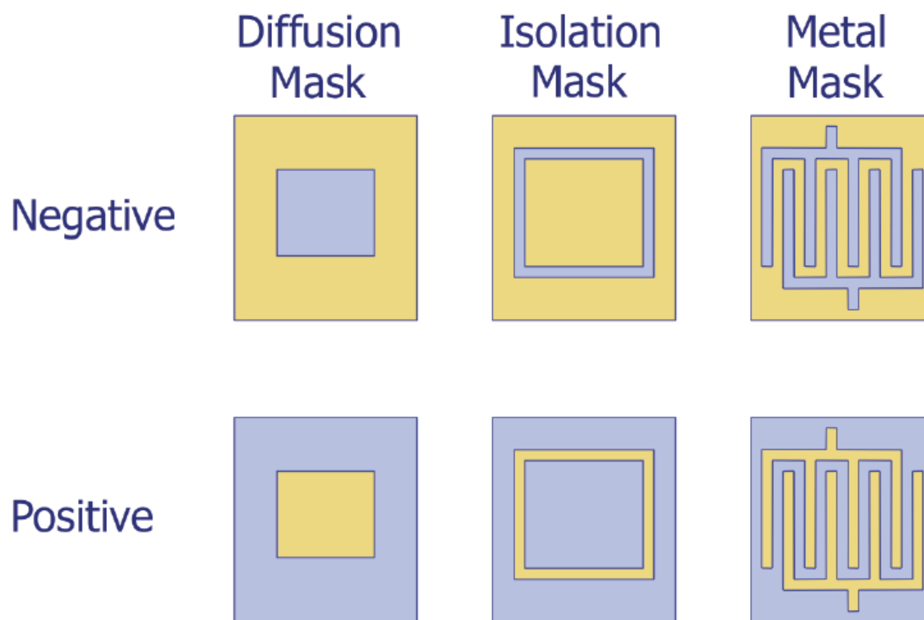


Figure 3. IC defects.

The figure is helpful in establishing the effect of different defects on the finished IC. Emitter, base and contact masks (negative resist) tend to be mostly transparent with dark rectangles where the dopants or contacts are to go. With positive resist there are clear boxes on an opaque background. The isolation mask for negative resist resembles a web of connected black lines separating the clear epi tubs. For positive resist the opposite is true, clear isolation diffusions surrounding opaque epi tubs. The metal mask for negative resist is clear where metal belongs. For positive resist the metal pattern is opaque on a clear background.

For each of these types of layers it is possible to create a table which will reveal the likely effect on the circuit of a wide range of defects. We show some typical results in the table below (Table 1).

Process Step	Problem	Result (Neg. Resist)	Result (positive Resist)
Emitter (Source/ drain)	Dust on mask	Extra diffused area-short adjacent n+ resistors	Hole in diffused area, Missing emitter-contact shorts to base, Open resistor
	Scratch in mask	Missing diffused area	Extra diffused area
	Scratched resist	Extra diffused area	Extra diffused area
Base	Dust on mask	Extra diffused area P resistor short to base or iso	Hole in diffused area
	Scratch in mask	Missing diffused area	Extra diffused area
	Scratched resist	Extra diffused area	Extra diffused area
Isolation	Dust on mask	Dots of extra p (shorts)	Missing isolation
	Scratch in mask	missing iso (tub to tub lkg.)	extra iso, p to p short
	Scratch in resist	extra isolation	extra iso, p to p short
Contact	Dust	Extra contact opening	Partial contact
	Scratch in mask	Partial/missing contact	Extra contacts, oxide short
	Scratch in resist	partial/missing contact	Extra contact, oxide short
Metal	Dust on mask	Break in metal, open	Extra metal remains, shorts
	Scratch in mask	Bridge, metal to metal short	Extra metal etch, open trace
	Scratch in resist	Bridge, metal to metal short	Extra metal etch, open trace
Via	Same as contacts	Same as contacts	Same as contacts

Table 1. Results of various types of photomask defects.

Diffusion masking defects are as stable as the intended diffusions and do not normally pose a reliability risk. The primary risk is that, by putting random elements into the circuit, they alter the circuit operation in ways which may or may not be caught by the outgoing ATE test equipment. The vast majority of diffusion masking defects are weeded out at wafer probe or sort. Particles in, on, or under the resist can interfere with its exposure or development leading to extra or missing resist on the wafer and subsequent additional or missing diffused areas. Scratches or smearing of resist similarly add diffusion where none was intended or block it where it was. Missing or extra opaque areas on the photo mask have similar effects. Early technology required the photo mask to physically contact the resist coated wafer. Crystal defects, such as epi spikes, created high spots on the wafer, which damaged the photo mask at that location and caused subsequent prints from that mask to replicate the same defect on each subsequent

wafer, causing "repetitive masking defects". As the technology progressed to projection alignment, the mask never comes into contact with the wafer, and is typically encased in a plastic shroud called a pellicle, which protects the mask surface from dust and damage. Any dust landing on the plastic surface is several mm away from the mask pattern and is so out of focus during the printing process that it will not be replicated on the wafer resist pattern. Because projection masks are so well protected they have an unlimited lifetime and great expense can be taken making them perfect using e-beam lithography, defect inspection and correction using Focused Ion Beam tools. As device dimensions shrunk and wafer diameter increased it was increasingly difficult to print the whole wafer in one exposure. Reducing steppers have a 4-5x larger pattern on the mask, which is optically reduced and stepped across the wafer in several exposures. If the reticle did have a masking defect that defect would be repeated in each field printed. Also, because each field is separately aligned the alignment may vary from field to field. Fields are generally a few cm on a side.

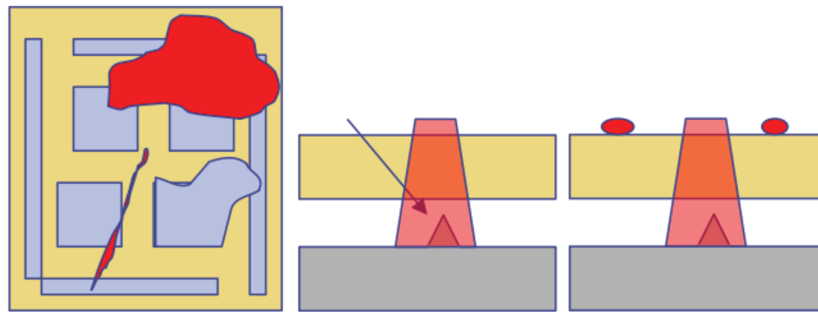


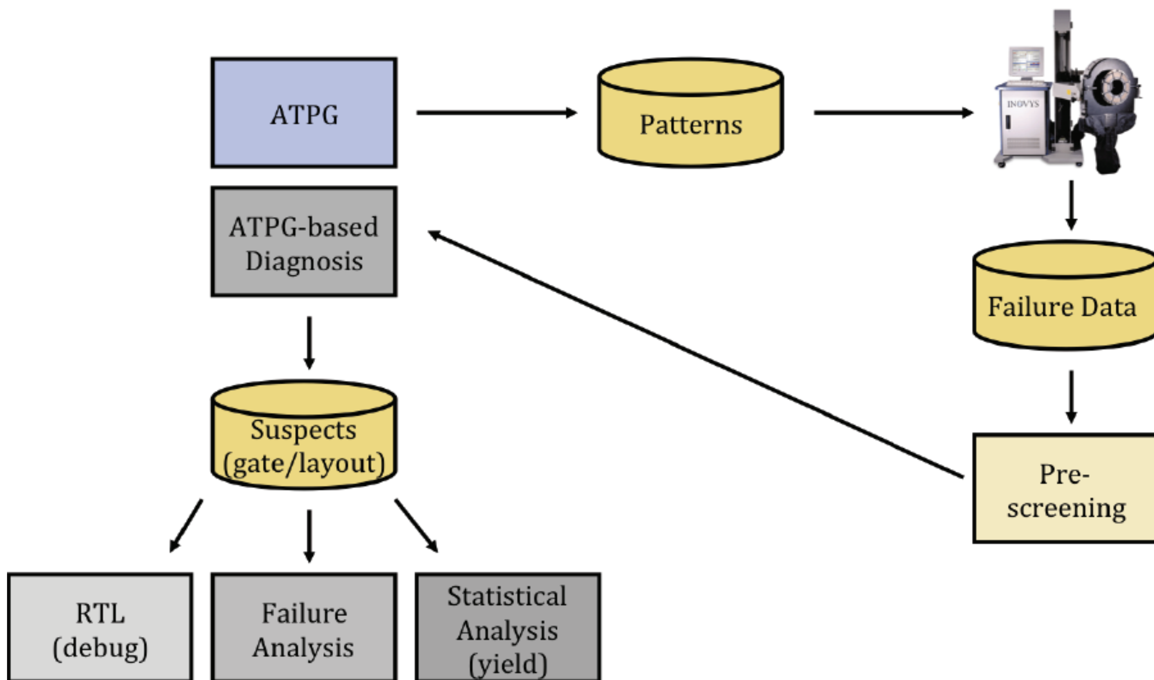
Figure 4. Example of resultant problem due to patterning and alignment.

Technical Tidbit

Basic ATPG Diagnosis

This technical tidbit helps explain the difference between ATPG and ATPG Diagnosis. ATPG Diagnosis uses the ATPG circuitry, tester, and test results to help isolate the location of a failure on a complex chip.

It is important to differentiate between "ATPG" and "ATPG diagnosis". Not just because the actual pattern generation and the diagnosis of ATPG patterns may be performed with different tools/products, but because there are some subtle, but important differences. For instance, during pattern generation, you may, for instance, only target stuck-at faults, since a pattern targeting stuck-at faults will typically detect bridge and open defects. For diagnosis, however, you would typically also have models for bridges and opens, even though these models weren't needed for pattern generation. Therefore, ATPG diagnosis typically involves additional test engineering effort after the failure is discovered by testing.



Here's how the process works. During the design phase, design and test engineers run automatic test pattern generation software to generate test vectors that will theoretically exercise the majority of the nodes within the circuit. These patterns can be input into a tester. The tests can be run on a part or group of parts to identify failures. These failures can then be analyzed for trends or severity. If the production contract or other issues dictate that the parts should be analyzed, they can be run through an ATPG-based diagnosis process. With models for opens and bridges, one can use ATPG-based diagnosis to identify suspect nodes based on the layout and failing vectors. One can make further use of the data for debug, failure analysis, and statistical analysis. Although this process can require more test engineering effort, ultimately it takes less effort than the requisite detailed failure isolation effort that is often required for analysis of complex ICs with subtle functional failure modes.

Ask the Experts

Q: Why do we typically use a lightly doped epi layer on top of heavily doped substrate?

A: There are several important reasons why p- epi/p+ substrate works well. One is to reduce the MOS leakage current. If we were to simply fabricate transistors in a p- substrate with no epi, there would be a higher concentration of minority carriers. As such, the carriers should diffuse for hundreds of microns to space charge regions and be collected as a reverse bias leakage current. This is particularly a problem at higher operating temperatures. However, if one uses a p- epi layer on top of a p+ substrate, the p+ substrate has few minority carriers, so the minority carriers would only be generated in the epi. This has the effect of suppressing the diffusion current and lowering the leakage (important for low power applications). In addition, the p- epi/p+ substrate reduces the possibility of latch-up; it helps getter or trap oxygen precipitates, and finally, the p- epi layer is more free of oxygen, so that helps prevent the formation of defects.

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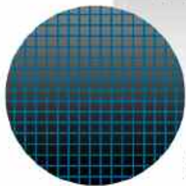

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Spotlight: Semiconductor Reliability and Qualification

OVERVIEW

Package reliability and qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. in particular, the proliferation of new package types. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. While customers expect high reliability levels, incorrect testing, calculations, and qualification procedures can severely impact reliability. Your company needs competent engineers and scientists to help solve these problems. ***Semiconductor Reliability and Qualification*** is a four-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability and qualification. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

What Will I Learn By Taking This Class?

Participants learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions and their parameters.
2. **Failure Mechanisms.** Participants learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die and at the package level. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, etc.
3. **Qualification Principles.** Participants learn how test structures can be designed to help test for a particular failure mechanism.
4. **Test Strategies.** Participants learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.
2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.
3. The seminar will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.
4. The seminar offers a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.

6. Participants will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

COURSE OUTLINE

Day 1 (Lecture Time 8 Hours)

1. Introduction to Reliability
    1. Basic Concepts
    2. Definitions
    3. Historical Information
2. Statistics and Distributions
    1. Basic Statistics
    2. Distributions (Normal, Lognormal, Exponent, Weibull)
    3. Which Distribution Should I Use?
    4. Acceleration
    5. Number of Failures

Day 2 (Lecture Time 8 Hours)

1. Overview of Die-Level Failure Mechanisms
    1. Time Dependent Dielectric Breakdown
    2. Hot Carrier Damage
    3. Negative Bias Temperature Instability
    4. Electromigration
    5. Stress Induced Voiding
2. Package Level Mechanisms
    1. Ionic Contamination
    2. Moisture/Corrosion
        1. Failure Mechanisms
        2. Models for Humidity
        3. Tja Considerations
        4. Static and Periodic stresses
        5. Exercises
    3. Thermo-Mechanical Stress
        1. Models
        2. Failure Mechanisms
    4. Interfacial Fatigue
        1. Low-K fracture
    5. Thermal Degradation/Oxidation

Day 3 (Lecture Time 8 Hours)

1. Package Attach (Solder) Reliability
    1. Creep/Sheer/Strain
    2. Lead-Free Issues

        3. Electromigration/Thermomigration
        4. MSL Testing
        5. Exercises
    2. TSV Reliability Overview
    3. Board Level Reliability Mechanisms
        1. Interposer
        2. Substrate
    4. Electrical Overstress/ESD
    5. Test Structures and Test Equipment
    6. Developing Screens, Stress Tests, and Life Tests
        1. Burn-In
        2. Life Testing
        3. HAST
        4. JEDEC-based Tests
        5. Exercises

Day 4 (Lecture Time 8 Hours)
1. Calculating Chip and System Level Reliability
2. Developing a Qualification Program
    1. Process
    2. Standards-Based Qualification
    3. Knowledge-Based Qualification
    4. MIL-STD Qualification
    5. JEDEC Documents (JESD47H, JESD94, JEP148)
    6. AEC-Q100 Qualification
    7. When do I deviate? How do I handle additional requirements?
    8. Exercises and Discussion

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

The Semitracks Analysis Instructional Videos™

One unique feature of this workshop is the video segments used to help train the students. Reliability Analysis is a visual discipline. The ability to identify nuances and subtleties in graphical data is critical to locating and understanding the defect. Some tools output video images that must be interpreted by engineers and scientists. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

2016 IPFA
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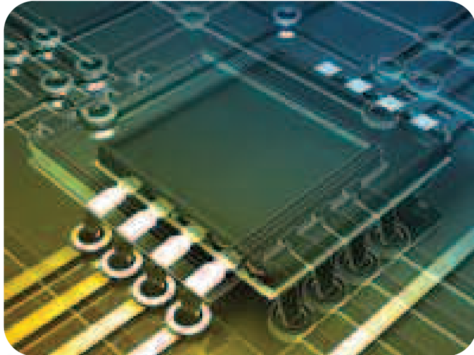
10 Bayfront Avenue, Singapore

Registration is available at
http://ieee-ipfa.org/

Chris Henderson will be attending and will be available for meetings. Please contact us at info@semitracks.com to schedule a meeting.



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Upcoming Courses

(Click on each item for details)

EOS, ESD and How to Differentiate
July 25 – 26, 2016 (Mon – Tue)
Manila, Phillippines

Semiconductor Reliability / Product Qualification
September 12 – 15, 2016 (Mon – Thur)
San Jose, California

Introduction to Processing
January 5 – 6, 2017 (Thur – Fri)
Shanghai, China