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Hot Carrier Degradation—Physics

By Christopher Henderson

It has been known for some time that as V_{GS} approaches V_{DS}, hot carrier degradation increases in n-channel transistors with sufficiently short channel lengths, which is the case for most state-of-the-art ICs. The exact cause is uncertain, and can be attributed to various causes. One is the oxide field dependence of hydrogen bond breaking. A second is the increase in electron-electron scattering, and shift of the potential minimum to the silicon dioxide interface. A third is multi-vibrational excitation effects, which become important at high drain currents. And a fourth is localized self-heating in the drain region. Let's assume electron-electron scattering dominates as an effect. The Damage Rate Is proportional to the difference between the drain current and the critical current, I_{CR} raised to the power M times the interface trap density times the mass of the electron times the effective voltage. I_{CR} is a critical or threshold current for the high V_G effect, given by the equation in Figure 10.

In this Issue:

Page 1	Hot Carrier Degradation—Physics
Page 6	Technical Tidbit
Page 7	Ask the Experts
Page 8	Spotlight
Page 13	Upcoming Courses

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$$I_{CR} \equiv I_D @ V_{GS} = \beta V_{DS} \qquad \beta \approx 0.6 - 0.8$$

$$I_{CR} \approx I_D F_{VV} \qquad F_{VV} \equiv \left(\frac{1 - (\beta V_{DS} - V_T)}{V_{GS} - V_T} \right) \qquad V_{GS} > \beta V_{DS}$$

Figure 10. High V_G Effect in n-Channel Transistors.

This can be seen more clearly in graphical format. There is a peak that corresponds to the midpoint of the drain-to-source voltage as shown in Figure 11, predicted by the linear model. Notice the secondary peak at higher gate-to-source voltages that is predicted by the high V sub G model. Actually, the data indicate that both models play a role in the hot carrier behavior.

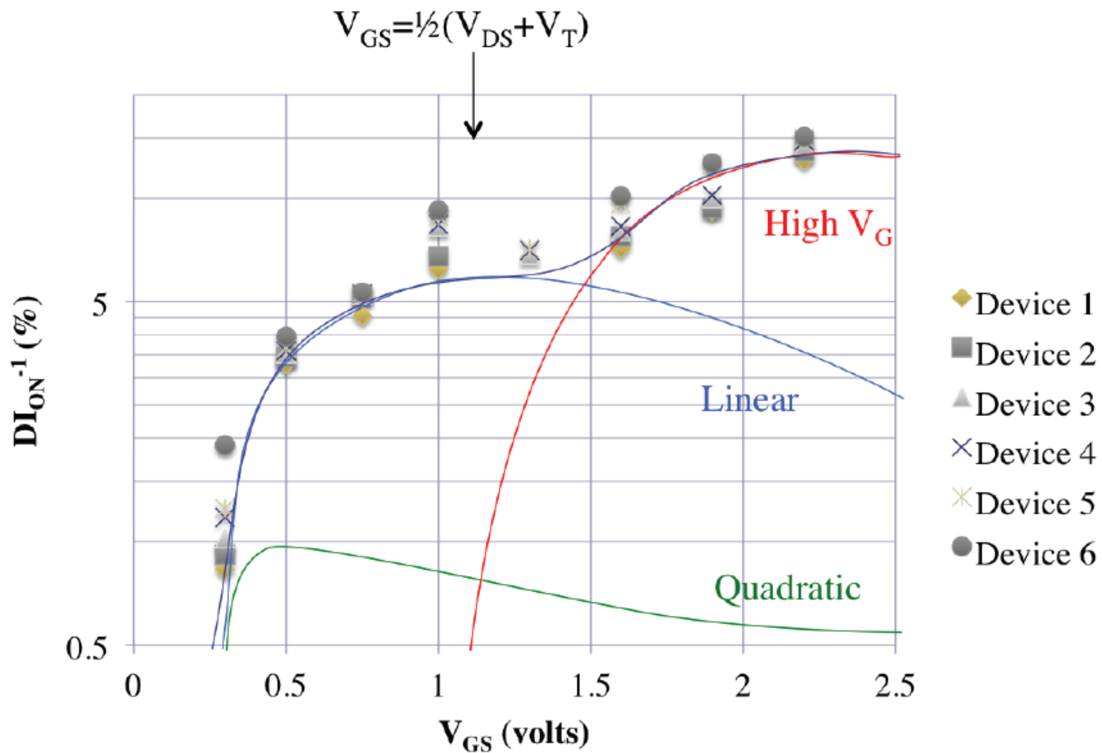


Figure 11. High V_G Effect Graph.

This leads to a unified model that can be used in the three regimes: low, medium and high gate-to-source voltages. Here we show the equations for each:

Low V_G: $R_0 = a_0 I_D S_{IT}(qV_{EFF})$

Mid V_G: $R_1 = a_1 I_D^2 S_{IT}(qm_{EE}V_{EFF})$

High V_G: $R_2 = a_2 I_D^4 F_{VV}^4 S_{IT}(qm_{EE}V_{EFF})$

Total $DR \propto R_{TOT} = R_0 + R_1 + R_2$

Then total DI_{ON}^{-1} is: $DI_{ON}^{-1} = \alpha(L, V_T)[(R_0 + R_1 + R_2)t]^n$

The total damage rate DR is then equal to the sum of the three individual regimes, and the change in current is also a function of the three changes in the resistance. IBM researchers call this the physical energy driven hot carrier model. It can be used in situations where more accuracy is required.

With scaling, the p-channel FET hot carrier behavior has evolved as well. It has gone from strong electron trapping over the low to mid V_g range and interface state generation at the higher V_g range, to weak electron trapping at the low V_g range, weak interface state generation at mid V_g, and a dominant high V_g mechanism. This high V_g mechanism has these characteristics. One, the time slope n is approximately 0.2 – 0.25 with slow measurements. Second, it is more dependent on VGS than VDS. And three, it is positively thermally activated. Interestingly, these are all characteristics of NBTI. We feel that this is no coincidence.

The graph in Figure 12 shows classical p-channel transistor behavior in older devices after hot carrier stressing. Notice that at low voltages electron trapping results in an increase in current, whereas at high voltages interface state generation and hole trapping result in a decrease in current.

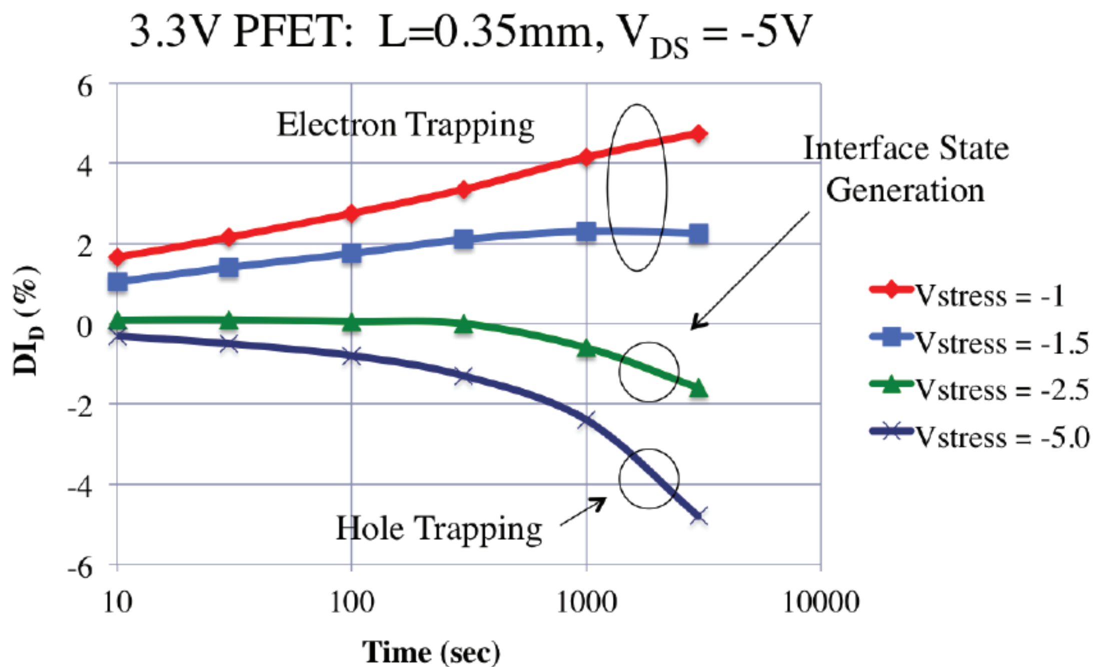


Figure 12. Older Technology PFET HC Effects.

In newer technologies, the effects are somewhat different. There is typically no increase in drain current at low stress voltages—indicating weak effects—but there is a more pronounced decrease in drain current due to some type of high gate voltage mechanism, as shown in Figure 13.

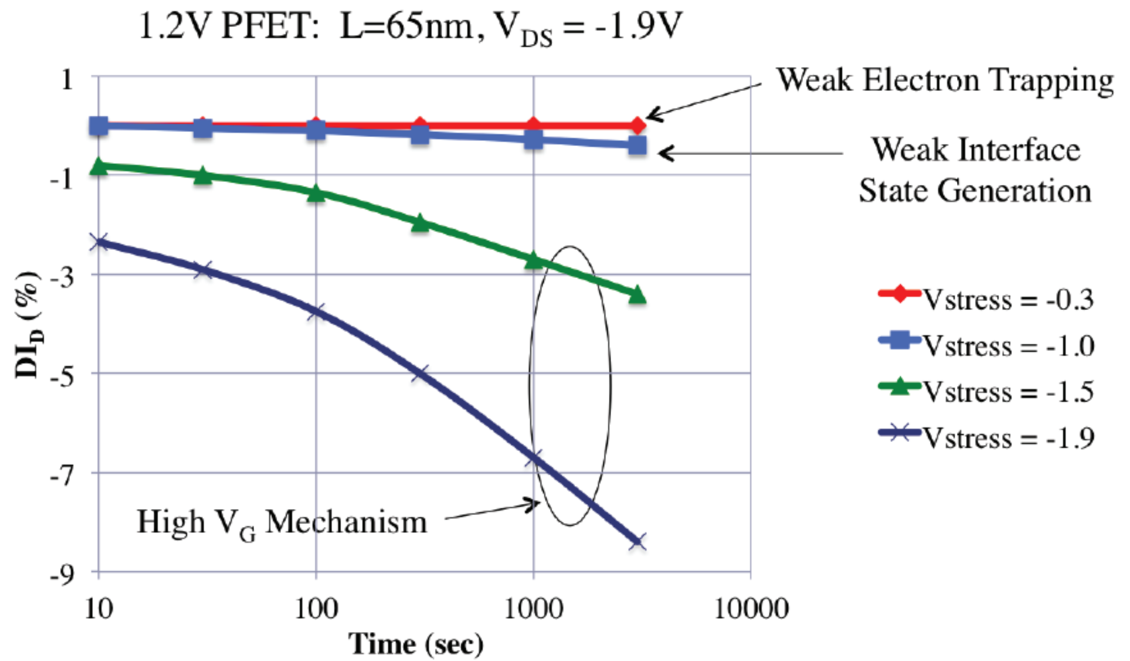


Figure 13. Newer Technology PFET HC Effects.

What exactly is the high gate voltage mechanism? It is thought to be an NBTI-enhanced effect by localized self heating. This is based on the idea that the effective temperature for NBTI is increased on the drain side of the channel due to carriers releasing energy there. Hot electrons generate acoustic phonons—or lattice vibrations— which is in essence, heat generation. Also, hot electrons will generate optical phonons which in turn generate acoustic phonons or heat.

This is a model that captures this line of thinking. We start with the basic NBTI model:

$$\Delta I_{ON}^{-1} = AV_{GS}^{p} exp\left(-\frac{\Delta H}{kT}\right) t^{n}.$$

The model is then generalized to the case of asymmetric, localized self heating by introducing an L term, and replacing T with T_{EFF}. The parameters P, ΔH, and n remain the same. For the bulk region beneath the transistor, the self heating mechanism should contribute a ΔT proportional to P_D, the local drain power dissipation. The Localized Self Heating Enhanced NBTI Model is then given by the expression:

$$\Delta I_{ON}^{-1} = AL^{-m} V_{GS}^{p} exp\left(-\frac{\Delta H}{k(T_{AMB}+\theta_{SH} I_D V_{EFF})}\right) t^{n}$$

with the parameters $m \sim 1$, $\theta_{SH} \sim 100 - 150$ K/mW/µm. The parameter m is approximately equal to 1, and θ_{SH}, or the thermal diffusivity, is between 100 and 150 Kelvin per milliwatt per micron.

As we discussed previously, a major impact of hot electrons is the generation of interface states. The energetic electrons break the silicon-hydrogen bond, leaving a dangling silicon bond while the hydrogen diffuses away. This dangling bond will trap charge and also scatter charge carriers in the channel, affecting both the threshold voltage and the mobility of the transistor.

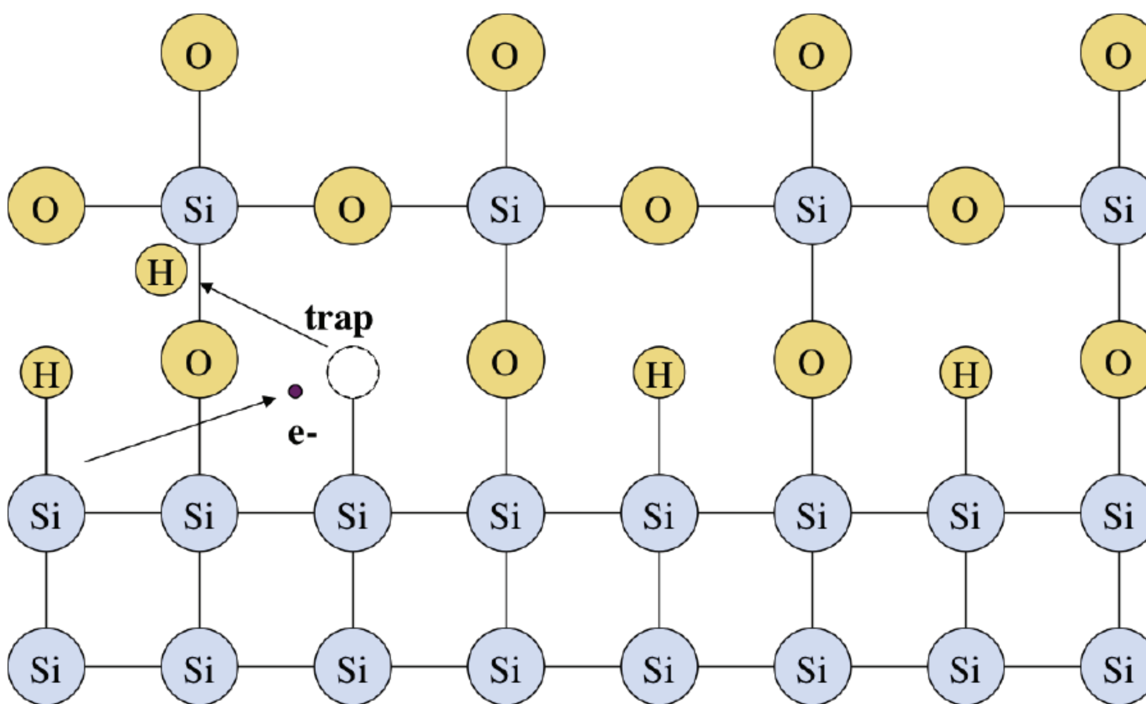


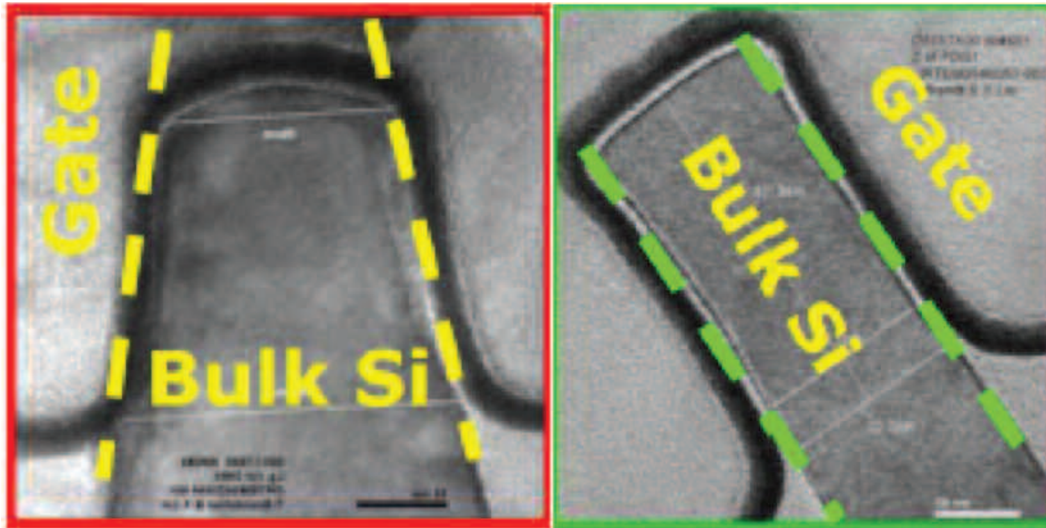
Figure 14. Interface State Generation.

We want to leave you with these main ideas. Scaling associated and its effect on hot carriers is driven by energy, not electric field. The mid gate voltage regime—rather than the high gate voltage regime—is most representative of hot carrier behavior in typical CMOS switching applications for both n-channel and p-channel transistors. For a realistic assessment of product impact and the required timing margins, hot carrier effects should be characterized by the amount of parametric shift, not as an ambiguous lifetime parameter. The dominant device mechanism is typically hot carrier degradation for n-channel transistors, and NBTI for p-channel transistors. This may change with hi-K due to the effects of positive bias temperature instability or PBTI.

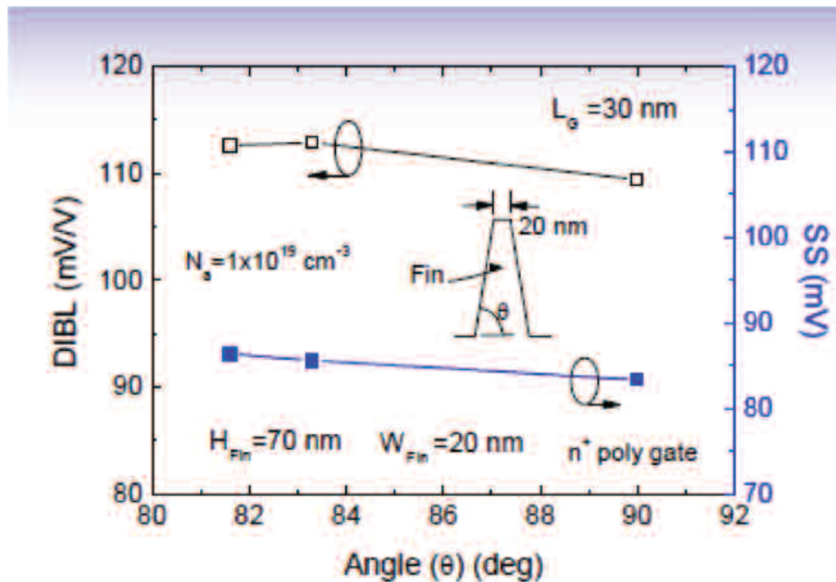
Technical Tidbit

FinFET Taper Angle

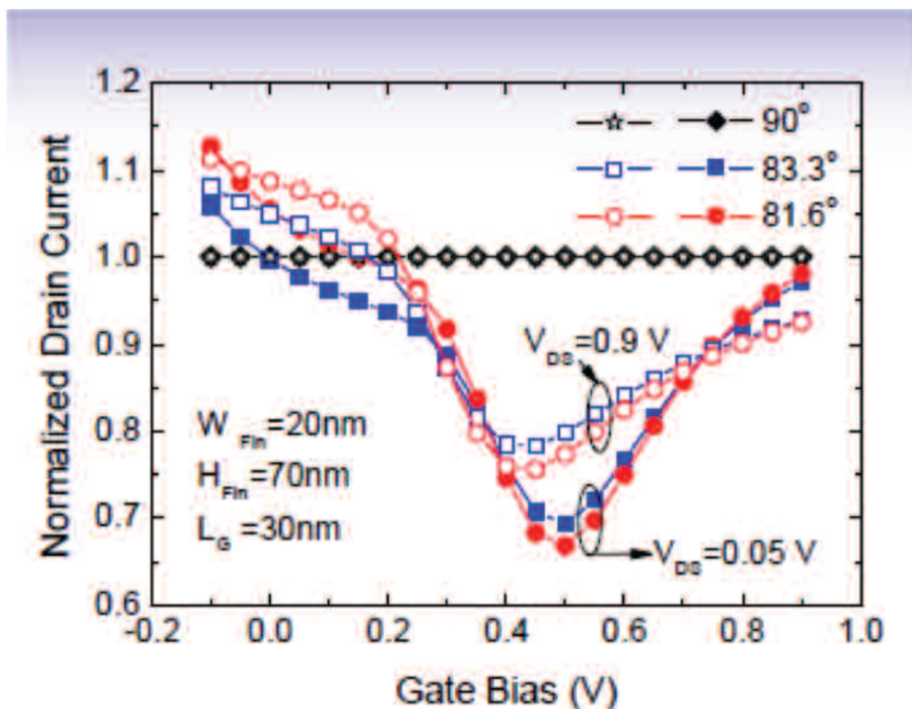
FinFET structures are quickly becoming common in advanced technologies. One important aspect of the fin is the taper angle. In general, process engineers try to design the fin with a taper angle as close to 90 degrees as possible. The image on the left shows a fin with a taper angle significantly less than 90 degrees, while the image on the right shows a structure with a taper angle close to 90 degrees.



A fin taper angle significantly less than 90 degrees leads to degraded short channel effects. The graph nearby shows the effect of fin taper angle on Drain Induced Barrier Lowering (DIBL) and Subthreshold Slope (SS). Notice that when the fin angle is less than 90 degrees, DIBL and SS increase. While these changes look fairly minor, they actually create more significant effects on transistor performance.



When we looks at the normalized drain current as a function of the gate bias, we see more pronounced effects. Notice that at moderate gate bias voltages of 0.4 – 0.6 volts, the normalized drain current is significantly less than 1.0. This effects the transistor not only at low V_{DS} values, but also at higher V_{DS} values.



Ask the Experts

Q: How does current-carrying-capability between Gold and Copper wire compare?

A: Both resistivity and melting temperature play a role in current-carrying-capability. Gold and Copper have somewhat different resistivities. Gold is 2.44e-6 ohm-cm, while Copper is 1.68e-6 ohm-cm. This means that Copper has about 1.4 times the current-carrying-capability of Gold. Gold and Copper have fairly similar melting temperatures, so melting temperature is not an important difference between the two metals.

Spotlight: MEMS Packaging

OVERVIEW

Microelectromechanical Systems (MEMS) have captured the interest of the public with their promise to miniaturize existing systems. Although much of the excitement surrounding MEMS has died down, real applications are beginning to emerge. MEMS accelerometers for games, automotive, and wireless applications have emerged. MEMS inkjet chips are now ubiquitous, and new applications for RF and sensors are in development. One of the most challenging aspects of MEMS is packaging. Forces that normally do not affect meso-scale objects must be understood and controlled at the micro-scale. This has created a number of challenges related to the packaging of these components. ***MEMS Packaging*** is a comprehensive 2-day course that offers detailed instruction on the design and modeling of MEMS packages. We place special emphasis on surface-to-volume ratio issues, electrostatics, liquid wetting, inertia, and other parameters. This course is a must for every manager, engineer, and technician working in semiconductor packaging, using MEMS components in high performance applications or new packaging configurations, or supplying packaging tools to the industry.

WHAT WILL I LEARN BY TAKING THIS CLASS?

By focusing on the fundamentals of MEMS packaging, participants will learn why advances in the industry are occurring along certain lines and not others. Our instructor works hard to explain MEMS packaging without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants learn basic but powerful aspects about semiconductor packaging. This skill-building series is divided into four segments:

1. **MEMS Market Overview.** Participants understand the driving market forces behind MEMS packaging. They review the technology trends, the market segments, and the major manufacturers and suppliers.
2. **MEMS Technical Basics.** Participants review the basic wafer processing steps for MEMS devices, including deep reactive ion etching, wet etching, patterning, CMP, and more. They also discuss the major research activities occurring in the MEMS area.
3. **MEMS Assembly, Testing, and Packaging.** Participants learn the fundamentals of packaging concepts for MEMS devices. They learn about bonding, printing, backgrinding, structural release, wirebonding, flip chip attach, cleaning, encapsulation, and basic testing. They discuss the challenges and tradeoffs associated with each topics.
4. **MEMS Reliability.** Participants learn MEMS reliability issues and associated analysis and simulation techniques. They also learn about the physics and mechanics issues involved in reliability degradation of MEMS devices.

COURSE OBJECTIVES

1. At the end of the course, participants will understand the major issues associated with MEMS Packaging.
2. They will also know how MEMS devices are fabricated and packaged.
3. Participants should be able to identify areas within MEMS Packaging where development is occurring.
4. The attendees will gain an understanding of process activities like backgrinding, structural release, clean, and encapsulation.
5. Participants will gain a basic understanding of testing MEMS devices.
6. The participants will learn about reliability aspects of MEMS devices, in particular, reliability issues associated with the packaging process.
7. Finally, the participants can interact with the instructor to discuss specific items and directions of interest at Kulicke and Soffa regarding MEMS assembly and test.

COURSE OUTLINE

1. MEMS Market Overview (downplay this activity, but do enough to get everyone on the same page)
   - 1.1. Types of devices, applications, volumes, growth rates
   - 1.2. Technology trends
   - 1.3. Major device manufacturers
   - 1.4. Major assembly and test equipment manufacturers
2. MEMS Technical Basics
   - 2.1. Overview of Device Processing and Manufacturing Techniques
     - 2.1.1. Summary of MEMS fabrication processes
     - 2.1.2. Overview of what's going on at R&D Centers in MEMS
     - 2.1.3. Major equipment suppliers by process step
     - 2.1.4. Backend/packaging level – who is doing what?
     - 2.1.5. Environmental considerations in MEMS fabrication and assembly processes
   - 2.2. The Impact of Packages and Assembly Processes in MEMS Device Operation
   - 2.3. High-level method of operation of device types and the role of packaging for each
     - 2.3.1. Pressure Sensors and microphones
     - 2.3.2. Inertial sensors: accelerometers and gyroscopes
     - 2.3.3. Magnetic sensors: compasses and Hall sensors
     - 2.3.4. Optical MEMS: displays and imagers
     - 2.3.5. RF MEMS: switches, time bases, and relays
     - 2.3.6. Fluidic MEMS: ink jets, Lab on a chip, DNA analysis

3. Assembly, Packaging and Testing Processes (this should be the major portion of the course)
    3.1. Material topics for MEMS packaging
        3.1.1. Classes of materials used in MEMS packaging
        3.1.2. Critical material parameters for MEMS packages
    3.2. Bonding, Joints and Adhesion Processes
        3.2.1. Theory of bonding and adhesion
        3.2.2. Wafer bonding
        3.2.3. Thermocompression bonding and welding
        3.2.4. Soldering and brazing
        3.2.5. Sealing glasses and frit bonding
        3.2.6. Polymer bonding processes
    3.3. Printing, Plating and Dispensing
        3.3.1. Screen and stencil printing
        3.3.2. Metallic plating
        3.3.3. Dispensing processes
    3.4. Wafer Backgrind, Singulation and MEMS Release
        3.4.1. MEMS structural release
        3.4.2. Wafer backgrinding processes
        3.4.3. Wafer singulation (dicing) topics
        3.4.4. Interaction and tradeoffs between release and singulation
    3.5. Considerations in MEMS Die Attach
        3.5.1. Die attach process overview
        3.5.2. Unique factors in MEMS die attach
        3.5.3. Interaction between MEMS types/structure and process requirements
        3.5.4. MEMS die attach materials and processes
    3.6. Wirebonding MEMS devices
        3.6.1. Wirebond process overview
        3.6.2. Unique factors in MEMS wirebonding
        3.6.3. Interaction between MEMS types/structure and process requirements
        3.6.4. MEMS wirebonding materials and processes
    3.7. Flip Chip technologies as applied to MEMS
        3.7.1. Flip Chip process overview
        3.7.2. Unique factors in MEMS Flip Chip
        3.7.3. Flip chip materials and processes for MEMS
    3.8. Hermetic package assembly
        3.8.1. Principles of hermeticity, permeability and outgassing
        3.8.2. Vacuum and specialty gas sealing and gettering
        3.8.3. Hermetic packages styles
    3.9. Non-Hermetic Package Assembly
        3.9.1. Molding and encapsulation
        3.9.2. Plastic and substrate package styles

3.10. Chip Scale and Wafer Scale Packages
- 3.10.1. Wafer-level packaging process overview
- 3.10.2. Types of wafer-level packages
- 3.10.3. Thru-Silicon Vias (TSVs)

3.11. Tradeoffs in MEMS Packaging and Assembly Processes
- 3.11.1. Hermetic vs. non-hermetic packages
- 3.11.2. Wirebond vs. flip chip vs. TSV
- 3.11.3. Integration of MEMS release in the assembly process
- 3.11.4. Wafer-scale vs. component scale packaging
- 3.11.5. One chip vs. two chip solutions – what are the drivers?

3.12. MEMS Inspection
- 3.12.1. Special Cleaning Requirements

3.13. MEMS Test Considerations
- 3.13.1. Wafer-level MEMS testing considerations
- 3.13.2. MEMS testing during product development
- 3.13.3. End of Line MEMS testing

3.14. Throughput requirements per process step
- 3.14.1. Handling formats and systems
- 3.14.2. Handoffs between steps

4. MEMS Reliability

4.1. Overview of reliability and qualification test types

4.2. Typical failure mechanisms

4.3. Materials related issues

4.4. Process related issues

4.5. Assembly equipment features that improve reliability

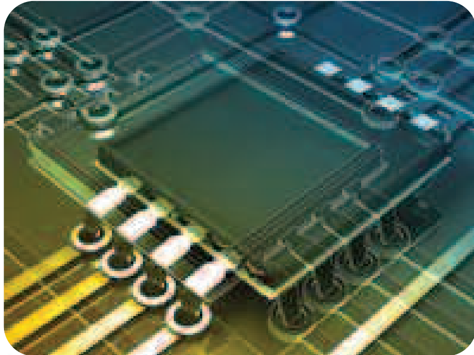
International Symposium for Testing and Failure Analysis

ISTFA 2015
International Symposium for Testing and Failure Analysis

November 1-5, 2015
Oregon Convention Center
Portland, OR, USA

Registration is available at
http://www.asminternational.org/web/istfa-2015

Semitracks plans to attend and is available for meetings. Please contact us at info@semitracks.com to schedule a meeting.



Upcoming Courses

(Click on each item for details)

Failure and Yield Analysis

August 10 – 13, 2015 (Mon – Thur)
San Jose, California, USA

Semiconductor Reliability

September 2 – 4, 2015 (Wed – Fri)
Munich, Germany

EOS, ESD and How to Differentiate

September 7 – 8, 2015 (Mon – Tue)
Munich, Germany

Product Qualification

September 9 – 10, 2015 (Wed – Thur)
Munich, Germany

MEMS Packaging and Reliability

September 14 – 15, 2015 (Mon – Tues)
Boston, Massachusetts

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).
To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.

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To post, read, or answer a question, visit our forums.
We look forward to hearing from you!